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A Novel approach of identifying uninitialized register in SOC designs

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Abstract: As we know that today's'SoC designs comprise of IP blocks from different design team and vendors. Integrating and verifying them is a challenge for design teams. Verification happens mainly in two stages RTL and Gate level simulation. One of the key challenges in gate level simulation of a ASIC/SoC is X (unknown) propagation debug. X propagation happens due to many reasons such as uninitialized memory, timing violations and due to non-resettable flops. X propagation due to non resettable flops are very difficult to debug and consumes enormous time, challenge further increases due to presence of hundreds/thousands of such non resettable flops which needs to be traced separately for every X propagation, To avoid these X propagation, such flops should be initialized with random value 0 or 1 in the beginning (at 0 time) to mimic silicon behavior but the problem is list of such non resettable flops is not available to the soc team and there are no efficient & reliable techniques present to identify such flops.
The proposed paper explains a methodology which can generate a list of non resettable flops required to avoid 'X' propagation in gate simulation. This uses formal tools and gate level VCD of the physical design.

Keywords: Non resettable flop, Gate level Simulation, Uninitialized register

I. INTRODUCTION

Gate level simulation now a day is almost mandatory for every complex SoC. As design complexity, number of asynchronous clock domain and size of the design increases, gate level verification becomes very challenging and time consuming task. Basic question arises in minds of many "why do we need gate level simulation when STA (static timing analysis) and formal verification is done". There are multiple reasons for this.

- STA may set false and multi cycle paths where they don't belong – wrong understanding of the design may lead to wrong false path definition.
- Validate asynchronous flop to flop paths which STA doesn't cover.
- Validate constrains defined during formal verification while DFT logic is inserted after synthesis.
- BCS/WCS Timing simulation with back annotated SDF to validate dynamic switching.
- ATE tester pattern generation from SDF simulation.
- Identify any faulty initial condition of the flop – X/Z, RTL simulation is normally optimistic and may initialize a flop with 0 or 1 which may not match with silicon behavior while gate level simulation is quite close to silicon.

Gate level simulation is verified with ZD (zero delay) to validate if the design has come out of reset, scan insertion is proper. Fully SDF back annotated gate level simulation is done to validate CDC (clock domain crossing), STA timings and dynamic switching. SDF based simulation may also be used for ATE pattern generation.
One of the key challenges of gate level simulation is identification of X propagation which may happen due to un-initialized memory, uninitialized flop, timing violation etc.. With multimillion gates design and multiple clock domains, significant amount of time is spent in debugging source of X and fixing the X propagation.

II. EXISTING APPROACHES

Gate level simulation is a very painful and time consuming task. Traditionally it is done using VCS simulator or any other industry standard simulator tool. Most of the time is spent in debugging X (unknown) propagation in the simulation. This debug of tracing X is manual effort which is dependent on person's experience and design knowledge. Practically it is not possible to run 100% test cases at gate level. So a subset of total verification suite is run on gate level. This limits number of issues that can be un-covered.

There are several causes for X propagation in GLS. Most complex one to debug being non-resettable or un-initialized flops. This paper presents an innovative flow of finding all non-resettable flops which causes X propagation if not initialized. This uses gate level VCD along with cadence formal verification tool, LEC verify. VCD is a dump in standard format. We can also replace cadence formal tool with any other EDA formal tool in this flow. These flops are re-viewed with designer and forced to random value (0 or 1) during simulation. Using random initialization of the non resettable flops increases the probability of identifying the design and initialization issues.

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III. SOURCES OF X PROPAGATION IN GATE LEVEL SIMULATION

X propagation can happen due to

1. Uninitialized memory array in the simulation.

Read transaction from a memory array which is not initialized causes X propagation in the design. All memories must be initialized during simulation. This can be easily done with compilation switch or doing out a back door loading of memory with all 0"s. For e.g. following compare is from VCS to initialize all memory arrays with 0's.

+VCs+initmem+0|1

2. Setup and hold violation

Setup and hold violation in SDF simulation may cause X propagation. This needs to be analyzed on a case by case basis and cross checked with STA reports if it is found in the same clock domain. Timing clean SDF should not have any setup or hold time violation for any flops in the same clock domain. If the violation appears on a flop which has a different clock domain as compare to originating flop then it should be checked if the violation is present on 1st flop of the two stage synchronizer, if yes, it can be ignored and Filter should be applied to mask such violation else synchronizer is required in such paths.
+notimingcheck or +no specify statements can be used to avoid X propagation from a known timing violation.

3. Un-initialized flops in the design

When hard reset of the design is asserted, all flops are supposed to have valid 0 or 1 value. Flop can be initialized by asynchronous set/clear pins or by synchronous reset circuit. Figure 1 shows asynchronous resettable flop.

Asynchronous reset flops gets initialized to 0 or 1 as and when reset signal is asserted.

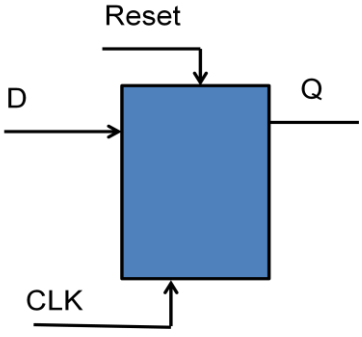

Figure 1: Asynchronous Resettable flop

In case of synchronous resettable flops – Figure 2, synchronous reset is applied to D input through combinational logic. It is ensured in design that before hard reset is removed, the flop gets initialized to valid value.

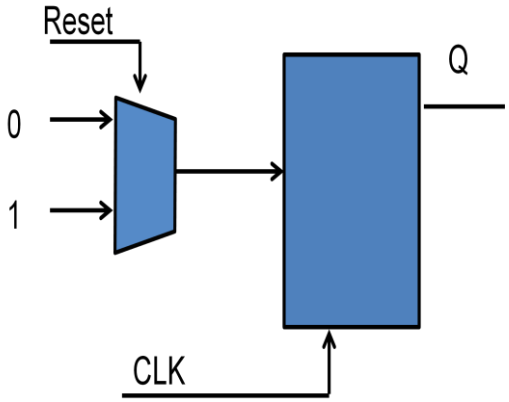

Figure 2: Synchronous Resettable flop

3.1 Un-initialized flops in the design

Non-resettable flops are the ones which do not have valid 0 or 1 value on Q of the flop during device reset assertion. These are the flops which cause 'X' propagation. These flops neither have set/clear pin nor synchronous reset provided. Identification of these flops is a critical task in GLS.
Unlike memories there is no simulator option which initializes all flops in the design. Simulator options are not effective in initializing UDPs in the design.

3.2 Synchronous reset flop without clock toggle during reset phase

These are valid synchronous resettable flops. Reset is provided as combinatorial input to D. Clock to flop is disabled during reset assertion and no clock toggle happens during reset state. Though D input has valid 0 or 1 upon reset, Q will still hold value of 'X' after coming out of reset; clock may be enabled to this flop. By that time 'X' propagation happens to next flop in the design.

3.3 Flop with Combo loop back

As shown in Figure 3 and 4, these flops are mostly the flops whose D input is having a feedback path from the same non resettable flop or some other non resettable flop. These flops can never recover from 'X' after reset is removed.

Here NR stands for Non Resettable flop

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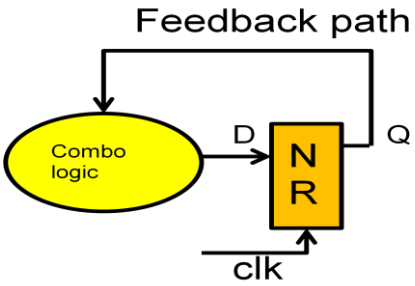

Figure 3: Non Resettable flop having feedback path from itself

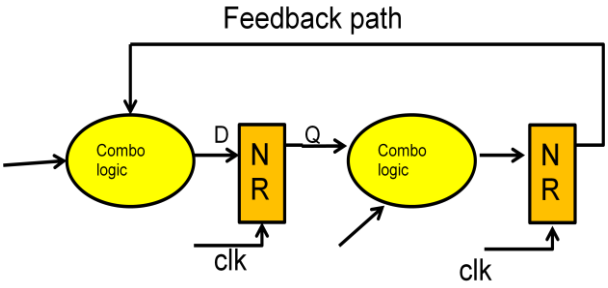

Figure 4: Non Resettable flop having feedback path from some other non resettable flop

During simulation any of the above 3 conditions originate 'X' and these 'X's are propagated through design'

IV. PROPOSED METHODOLOGY

We have developed a standard automated flow which identifies all the required non resettable flops in the design which is must to initialize. This uses gate level VCD and a formal tool which first reads gate level net list and subsequently initializes its flop states from VCD at a given time point which is calculated from VCD at reset removal. Formal tool used here is cadence LEC verify. This flow is completed in 5 steps

1. Generate VCD of the fill design using zero delay or SDF release and identify time point when reset is removed. This time point is T_RR.

2. Invoke LEC verify

3. Read the same ZD/SDF design. LEC command used to read the design is "read design"

4. Initialize state of all the flops using VCD generated in 1st step, we need to specify the time at which states has to be initialized. This time point is T_RR.

5. Issue the command "report rule check INIT3" which list down all the flops with design hierarchy which is uninitialized.

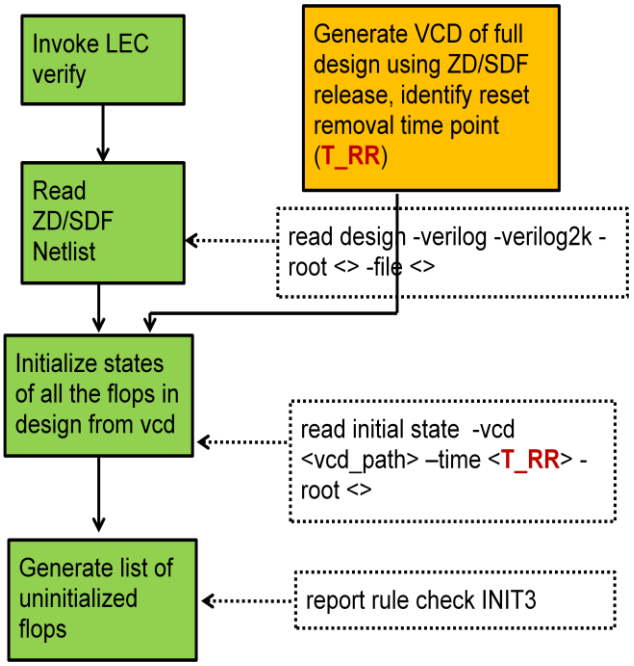

Figure 5: flow diagram of the proposed methodology

Uninitialized flops listed in the last step are the flops which remains unknown at the time of reset removal and these are mainly the

1. Non resettable flops who is propagating 'X' due to its D input is driven from feedback path from itself or some other non resettable path
2. Non resettable flop with valid D input but dead or unknown clock.
3. Non resettable flops without set/clear pin and without any synchronous reset.

Generate flop list can be reviewed with designer and initialized in gate level simulation with random values of 0 and 1 so that possible issues due to a particular initialization of these flop can be generated in GLS itself.

V. RESULTS

The proposed scheme was successfully tested and proven on two SoC. We used Conformal LEC from Cadence Inc as formal tool and VCS as simulator to generate gate level VCD. Below table reports results from design 1 and design 2. As we can see that it finds 2464 number of non resettable flops from design 1 and 1548 number of non resettable flops from design 2 which needs to be initialized in GLS. Time required for running this flow is manageable.

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Table 1

Item	Design 1	Design 2
Gate count	~ 180000000	~ 220000000
Flop count	967534	1276390
Gate level VCD generation	8 hours (including compile time)	10 hours(including compile time)
Time taken be LEC in reading net list	~3 hours	~4 hours
Time taken in initializing states from VCD	~35 minutes	~40 minutes
Time taken in reporting uninitialized flops	~15 minutes	~15 minutes
Non Resettable flops reported	2464	1548

VI. CONCLUSION

The proposed flow to generate list of un-initialized flops is very simple and fast. This can be used for fast gate level simulation bring up and to detect silicon bugs which remains undetected due to improper verification of non resettable flops.

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BIOGRAPHIES

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