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System-on-Chip (SoC) for Telecommand System Design

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Abstract: The emerging developments in semiconductor technology have made possible to design entire system onto a single chip, commonly known as System-On-Chip (SoC). The incresase in Space System's capabilities kindled by the On-board data processing capabilities can be overcome by optimizing the SoCs to provide cost effective, high performance, and reliable data. This is achieved by embedding pre-designed functions into a single SoC, which utilizes specialized reusable core (IP cores) architecture into complex chip.This paper is concerned with the design of telecommand system for transfer of signals from ground station to space station by the integration of SRAM(Static Random Access Memory), ARM (Advanced RISC Machine) Processor, EDAC unit (Error Detection And Correction)and CCSDS (Consultative Committee for Space Data System) decoder system.In this paper we designed the Telecommand SoC by using VHDL code.The implementations have been done using XILINX FPGA platform and the functionality of the system is verified using Modelsim simulation. The presented SoC design operates with the frequency of 143.74 MHz and it consumes 2056 mw power .

Keywords:ARM Processor, EDAC unit, SRAM, telecommand, IP cores,CCSDS decoder.

I. INTRODUCTION

A system on a chip or system on chip (SoC or SOC) is an Integrated Circuit (IC) that integrates all components of a computer or other electronic system into a single chip. It is a collection of all components and subcomponents of a system on to a single chip. SoC design allows high performance, good process technology, miniaturization, efficient battery life time and cost sensitivities. This revolution in design had been used by many designers of complex chips, as the performance, power consumption, cost, and size advantages of using the highest level of integration made available have proven to be extremely important for many designs .

The emerging technologies in the field of semiconductors, along with the use of the System-on-Chip (SoC) design, have made this possible. System development based on the use of a core-based architecture, where the reusable cores are interconnected by means of a standard on-chip bus, which is the most common way to integrate the cores into the SoC[7] .This design methodology has been proven to be very effective in terms of development time and productivity since it reuses existing Intellectual Property (IP) cores. In a SoC design which uses multi-million gates the design and test engineers face various problems such as signal integrity problems, heavy power consumption concerns and increase in testability challenges.

The semiconductor industry has continued to make impressive improvements in the achievable density of very large-scale integrated circuits .In order to keep pace with the levels of integration available ,design engineers have developed new methodologies and techniques to manage the increased complexity inherent in these large chips .One such emerging methodology is system-on-chip design, wherein predesigned blocks called Intellectual Property(IP) blocks, IP cores or virtual components are obtained from internal sources or third parties and combined into a single chip.These reusable IP cores may include embedded processors ,memory blocks, interface blocks, analog blocks and components that handle application specific processing functions[2]. The corresponding software components are also provided in a reusable form which include real time operating systems, kernels, library functions and device drivers .

II. SoC DESIGN METHODOLOGY

Every technological improvements in the integrated circuit industry is followed by the development of new design technology.The design methodologies can be grouped into the following categories:

(i)Area-Driven Design
(ii) Timing –Driven Design
(iii)Block-Based Design
(iv)IP- Core Based Design
(v) Platform –Based Design.

In this paper ,the IP –core Based Design Methodology is used. Since each and every component is being checked by itself it is easy to integrate them.It facilitates

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timing closure and functional correctness and also it meets the need of many different designs thereby enhancing the configurability.

III. DESIGN ARCHITCTURE

In this paper an On-Board System (OBS) of a small Satellite is implemented in the form of a telecommand System-on-a-Chip (SoC). Soft intellectual property (IP) cores written in the hardware description language VHDL are used to build the system on-a-chip. The resulting subsystem is the integration of SRAM, ARM PROCESSOR, EDAC Unit and CCSDS Decoder was designed. The Block Diagram of the design is shown in Fig. 1.

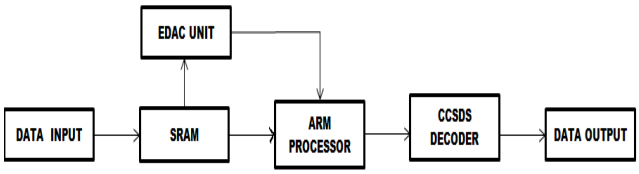

Fig. 1 Block diagram of SoC design

The telecommand input data is send from ground station to the space station it is given as input to the SRAM . In space applications it is well known that in Low Earth Orbit (LEO) stored digital data suffers from SEUs. These upsets are induced naturally by radiation. Bit-flips caused by SEUs are a well-known problem in memory chips and error detection and correction techniques have been an effective solution to this problem[3]. For the secure transaction of data between the CPU of the on board computer and its local RAM, the program memory has generally been designed by applying the Hamming code in the error detection and correction unit so that the errors can be detected and corrected and the resultant output will be a error free data.The resultant error free data is fed to the processor ,so that it will process the error free data and also it will collect all the on –board data signals and produce the resultant data output.

A. Design of SRAM

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The Dynamic RAM memory can be deleted and refreshed while running the program ,whereas Static RAM is not possible to refresh the programs. It but is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

The basic architecture of a static RAM includes one or more rectangular arrays of memory cells with support circuitry to decode addresses, and implement the required read and write operations[13].The block diagram of 2k x 32 bit SRAM is shown in Fig.2. SRAM memory arrays are arranged in rows and columns of memory cells called wordlines and bitlines, respectively. Each memory cell has a unique location or address defined by the intersection of a row and column,which is linked to a particular data input/output pin. The total size of the memory, the speed at which the memory must operate, layout and testing requirements, and the number of data inputs and outputs on the chip determines the number of arrays on a memory chip. Memory arrays are an essential building block in any digital system.The aspects of designing an SRAM are very vital to designing other digital circuits.The majority of space taken in an integrated circuit is the memory. Consider an Nxn SRAM array where 'N' indicates the number of bytes and 'n' indicates the byte size. The size of an SRAM with m address lines and n data lines is 2^m words, or 2^ m x n bits.

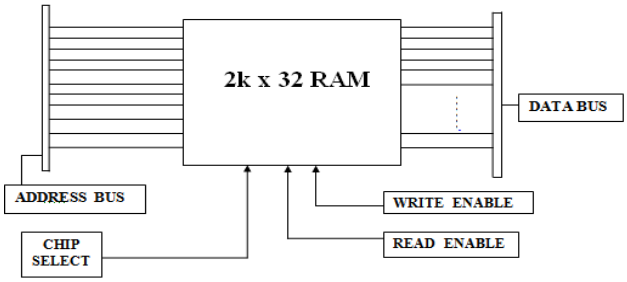

Fig. 2 Block diagram of 2K x32 bit SRAM

B. *Design of EDAC Unit*

Error Correction Codes (ECC) and error detection and correction (EDAC) schemes have been implemented in memory designs to tolerate faults and enhance reliability. Extra check bits (parity bits) have to be stored along with the information bits, so the hardware overhead includes the encoding/decoding circuit and the memory space for check bits. ECC can protect the memory from attacks of hard and soft errors. The modified Hamming Code and Hsiao Code are the most widely used Single-Error Correctable and Double-Error Detectable (SEC-DED) codes.The code word format is shown in Fig. 3.

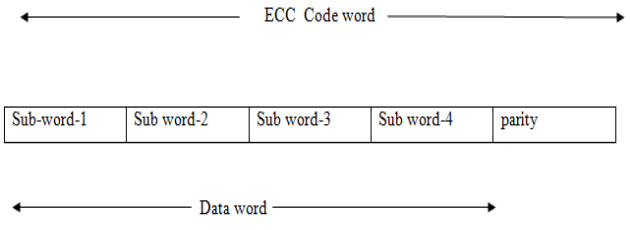

Fig. 3 ECC Code word format.

1) Hamming Code: Hamming code error detection and correction methodology is used for error free communication in communication system[11]. The transmitted and received data between source and destination may be corrupted due to any type of noise. In order to find the original transmitted data we use Hamming code error detection and correction technique. In hamming code error detection and correction technique

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to get error free data at destination, we encrypt information data according to even and odd parity method before transmission of information at source end. Hamming codes are still widely used in computing telecommunication and other applications[10]. It is also applied in data compression and block turbo codes. Because of the simplicity of Hamming codes they are widely used in computer memory. The hamming code representation of various data bits are shown in Table 1.It belongs to the family of (n,k)linear block codes where

Block length (n)=2^m - 1

Number of message bits (k)=2^m-m-1

Number of parity bits (m) = n-k

TABLE I
HAMMING CODE BITS REPRESENTATION

DATA BITS	CHECK BITS	TOTAL BITS
1	2	3
4	3	7
8	4	12
32	6	38
64	7	71

2) *Calculating the Hamming Code:*The key to the Hamming Code is the use of extra parity bits to allow the identification of a single error. Create the code word as follows:

- Mark all bit positions that are powers of two as parity bits. (positions 1, 2, 4, 8, 16, 32, 64, etc.).

- All other bit positions are for the data to be encoded. (positions 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, 17, etc.)

- Each parity bit calculates the parity for some of the bits in the code word. The position of the parity bit determines the sequence of bits that it alternately checks and skips. Position 1 will check 1 bit and skip1 bit,Position 2 will check 2 bits and skip 2 bits,Position 4 will check 4 bits and skip 4 bits, Position 8 will check 8 bits and skip 8 bits, Position 16 will check 16 bits and skip 16 bits, Position 32 will check 32 bits and skip 32 bits.

- Set the desired parity bit to "1" if the total number of ones in the positions it checks is odd.

Set the parity bit to "0" if the total number of ones in the positions it checks is even.

3) Integration of SRAM with EDAC unit: In space applications it is well known that in Low Earth Orbit (LEO) stored digital data suffers from SEU's caused by radiations. These radiations may be ultraviolet radiation,infrared radiation and gamma radiation. This change in data caused by SEUs are a well-known problem in memory chips and error detection and correction techniques have been an effective solution to this problem. For the secure transaction of data between the CPU of the on board computer and its local RAM, the program memory has generally been designed by applying the Hamming code.

In order to have the secure transmission of data between a central processing unit (CPU) and its local random access memory (RAM) the traditional means of error detection and correction (EDAC) is a Hamming code. In the theory of error control the designation (n, k) denotes a block code that takes a k-bit data word and maps it to an n-bit code word. For computers on board a satellite, and using the latest high density byte-wide RAMs, there is however a definite risk of two error bits occurring within one byte of stored data; either from the impact of a particularly energetic Single Event Upset (SEU), or from a second SEU creating a second error, and before the computer has had time to wash the first error.

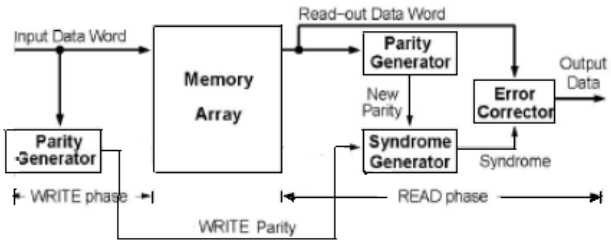

Fig. 4 Integration of SRAM with EDAC unit

In the EDAC scheme, shown in Fig.4 the Parity Generator generates the parity from the input data word. The entire codeword, which includes the data word and parity word is written into the memory when we perform the WRITE operation. In a READ operation, the data word to be read is used to generate the parity again. The Syndrome Generator compares the newly generated parity with the read-out parity to produce the syndrome that contains the information for error bits[3]. The Error Corrector corrects the error in the read-out data word if necessary, based on the Syndrome.

IV. DESIGN OF ARM PROCESSOR

As the high capacity, low cost FPGA devices train continues its revolutionary journey through the electronics design. Creation of soft processor based systems, destined to run within a chosen Target FPGA device, nowadays utilize one of the many supported flavors of 32–bit RISC(Reduced Instruction Set Computer) processor, wired up to access peripheral I/O and memory over a standard bus interface.Soft core processors are processors that are defined as part of the FPGA design that is programmed into the physical FPGA device[1], rather

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than physical, discrete devices connected to the FPGA, or processors that are immersed as part of the physical FPGA's makeup. Such processors are typically 32-bit and have simple, RISC architectures.

The ARM (Advanced RISC Machine) processor uses load-store architecture[1,5,8,14.There are no data processing instructions that directly manipulate data in memory. Thus, data processing is carried out solely in registers. The data register file consists of 32 registers, whereof 16 are accessible at one time (depending on the current operating mode). The operand unit performs the operand fetch for the three operand-slots. Also the data conflict detector and the forwarding system are placed here. The Barrel Shifter **unit** performs the arm-compatible barrel-shifting of the data in ALU data path B.The shift value can either be an immediate from the opcode, or a register value, which is loaded in the same cycle, no additional data load cycle is needed.

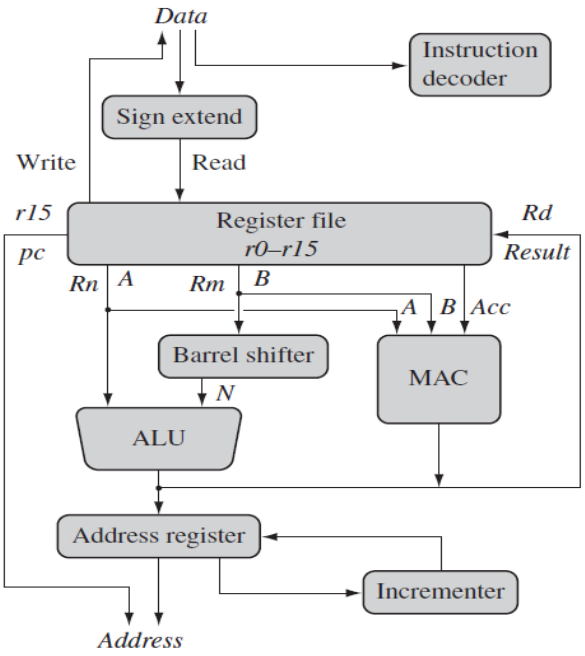

Fig. 5 ARM Core Architecture flow

The multiply unit calculates a 32x32 bit operation and outputs the lower 32 bit to the ALU data path B.The ALU holds the primary data operation units. All address-operations are done here (except for the program counter increment). Furthermore it handles the manual read/write access to the different machine status registers. The arithmetical unit performs the dedicated arithmetical add & sub operations and also the "arithmetical compares".i.e., CMP, CMN.

The logical unit performs the dedicated logical operations like "BIC" and "OR" and also the "logical compares" (TST, TEQ).The load-store unit outputs the correct address (instruction address or data address) to the memory address bus and also sends the write data and the control signals to the external memory interface[14]. The write-back unit performs the data write back to the register file and also accepts the read data from the memory. The MCR system (Machine Control Register) holds the machine control registers (program counter, all the saved machine status registers and the current machine status register) as well as the interrupt/context change system. The flow control generates the control signals for each stage and every module. The decoded instruction data is brought to this unit where it triggers all internal operations. The Opcode Decoder unit decodes the ARM-compatible opcode into processor control signals.

Data items are placed in the register file—a storage bank made up of 32-bit registers. Since the ARM core is a 32-bit processor, most instructions treat the registers as holding signed or unsigned 32-bit values. The sign extend hardware converts signed 8-bit and 16-bit numbers to 32-bit values as they are read from memory and placed in a register. ARM instructions typically have two source registers, Rn and Rm, and a single result or destination register, Rd. Source operands are read from the register file using the internal buses A and B, respectively. The ALU (Arithmetic Logic Unit) or MAC (Multiply-Accumulate Unit) takes the register values Rn and Rm from the A and B buses and computes a result. Data processing instructions write the result in Rd directly to the register file. Load and store instructions use the ALU to generate an address to be held in the address register and broadcast on the Address bus.

One important feature of the ARM is that register Rm alternatively can be preprocessed in the barrel shifter before it enters the ALU[8]. Together the barrel shifter and ALU can calculate a wide range of expressions and addresses. After passing through the functional units, the result in Rd is written back to the register file using the Result bus. For load and store instructions the incrementer updates the address register before the core reads or writes the next register value from or to the next sequential memory location. The processor continues executing instructions until an exception or interrupt changes the normal execution flow.

V. CCSDS TELECOMMAND DECODER

A telecommand system must reliably and transperantly convey control information from an the originating source to a remotely located physical device or process.The CCSDS telecommand system architecture defines a comprehensive set of layered ,standardised command servies that are applicable to a very wide range of mission needs .

In this paper,CCSDS telecommand decoder is designed. The Telecommand Channel enables an secure data path to be established for the transfer of telecommands to the spacecraft. The service contains two distinct layers of data handling operations:(i) CODING LAYER, which

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permits telecommand information bits to be more reliably transmitted through the noisy physical data channel using standard channel coding techniques. The Coding layer also provides information about the beginning of the contents of valid codeblocks and the continuity of the data stream, and it delivers the contents of those codeblocks to the layer above.(ii) PHYSICAL LAYER, which contains the radio frequency and modulation capabilities that may be invoked to establish the physical data channel.

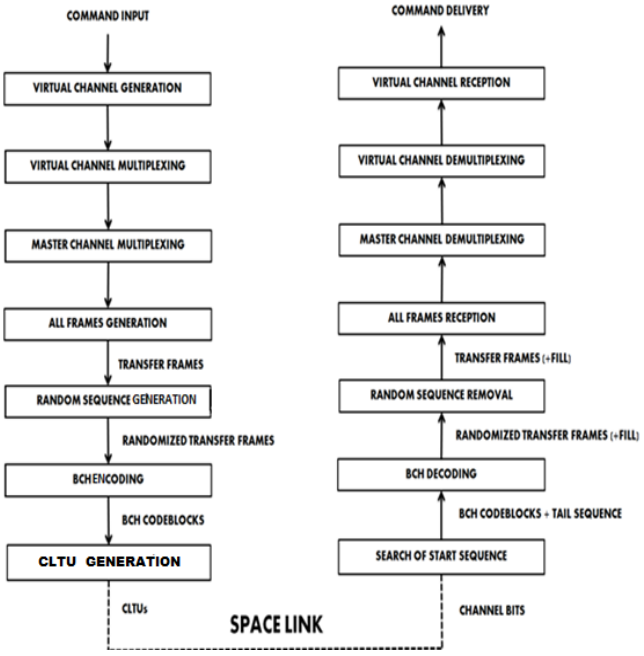

Fig.6 TC decoder implementation model

The Coding layer establishes the reliable, error-controlled data channel through which user telecommand data bits may be transferred. The data are encoded to reduce the effects of noise in the Physical layer channel on the user data. A block code has been chosen to provide this protection. Synchronization for the codeblock and delimiting of the beginning of user data are provided by the Command Link Transmission Unit (CLTU) data structure. Resolution of data ambiguity (sense of "1" and "0") when receiving the symbol stream shall be a service of the Coding layer.

VI. Results and Discussions

Table II shows synthesis report which gives information of the cell usage, device utilization constraint, timing summary. The device utilization gives information of the total hardware utilized. In this the integration of SRAM, EDAC unit, ARM processor and CCSDS Decoder is done so the data input is fed to the SRAM ,due to some radiations in the space the data stored in the SRAM gets flipped .It is passed to the EDAC unit in order to detect and correct the errors. From EDAC unit it is passed to the processor and it will process the data and it is send to the CCSDS Decoder unit to provides the desired output.

TABLE II
Xilinx Device Utilization Summaries

Logic Utilization	Available	Used	Utilization (%)
Number.of.Slice Registers	301440	2232	1%
Number.of.Slice LUT's	150720	3962	2%
Number.of fully used LUT-FF pairs	4838	1356	28%
Number of Bonded IOB's	600	318	53%
Number.of Block RAM/FIFO	416	6	1%

TABLE III
Xilinx Device PARAMETERS ANALYSIS

Maximum Operating Frequency	143.74 MHz
Area	2232 slices
Time Delay	6.831 ns
Power Consumed	2056 mw

VII. Conclusions

The primary focus in SoC verification is on checking the integration between the various components. Rather than implementing each of these components separately, the role of the SoC designer is to integrate them onto a chip to implement complex functions in a relatively short time. Since IP cores are pre-designed and pre–verified, the designer can concentrate on the complete system without having to worry about the correctness or performance of the individual components. The conventional telecommand system is designed with SRAM,EDAC unit,ARM Processor and CCSDS Decoder and they are integrated to form a SoC design. The simulation of each system is done separately and then integrated to produce final output. Future work includes the ASIC implementation of the entire design.

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BIOGRAPHY

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