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Study the characteristics of 65nm PMOS transistor incorporating the SILVACO TCAD TOOLS

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Abstract: This paper explains about the characteristics of 65 nm PMOS technology with strained silicon in terms of electrical parameters like drain current, gate voltage etc.. Fabrication processes of transistor were performed by the ATHENA fabrication simulator while electrical characterisation of device was performed by ATLAS simulator. The comparison of the performance of conventional 65 nm PMOS and strained silicon 65nm PMOS was done by $\mathbf{I_D}$-$\mathbf{V_G}$ characteristic. Comparison result represents the strained silicon PMOS had lesser power consumption in comparison to conventional PMOS.

Keywords:PMOS, strained silicon, threshold voltage, simulation process

I. INTRODUCTION

IN recent years, strained silicon has been focus of research for better performance of PMOS. Strain silicon is most suitable material for performance enhancement. This enhances the transport properties of electrons and holes and delivers transistor speed enhancement and low power consumption.

Fast scaling of MOSFETs drives increasing microprocessors performance and rapid growth of the information technology revolution. The reason behind this revolution is Moore's law. In 1965, Gordon Moore observed that the number of transistors in a chip increased exponentially over time [1]-[3]. This is due to transistor size decreased exponentially over time. When Moore made his prediction in 1965, the size of transistor was 100µm.During last three decades, transistor size exponentially decreased from micrometers to nanometers.In 2003, 45 nm transistor was fabricated and Moore's law is found valid in nanotechnology era. Presently we introduce the 65nm PMOS with strain silicon. Strained silicon is one of new technologies that enables a fairly dramatic increase in performance with a relatively simple change in starting materials [4]-[5].In 1980, researcher was demonstrated that PMOS with strained silicon were faster due to increased electron mobility and velocity. Furthermore in 1998, researchers showed it would work with leading-edge, sub-100 nm short-channel transistors. Today, companies such as Intel, IBM, Hitachi, AMD and UMC have reported success with strained silicon.

In this paper, firstly PMOS is fabricated. Furthermore strain silicon is added in the fabrication process of PMOS.Electrical characterisation of devices was done and we compared the simulation result of each device. Comparison result represents the strained silicon PMOS had lesser power consumption in comparison to conventional PMOS.The analysis of PMOS is focused on strain silicon. In this paper, we described a 65-nm PMOS transistor designed for high speed and low power operation. Section II describes strained silicon technology. SectionIII–VI represents the methodology used in 65-nm PMOS transistor and section VII gives the idea about its I_D-V_G characteristics.

II. STRAINED SILICON

The strained silicon is formed by depositing a thin layer of Silicon on a silicon germanium layer onto a Si substrate. Figure 1 represents strain silicon in which the silicon atoms are stretched beyond their normal interatomic distance. This is performed by putting the layer of silicon over a substrate of silicon germanium (SiGe). Strained Si is a technology that involves physically stretching or compressing the silicon crystal lattice via various means, which in turn increases carrier mobility and enhances the performance of the transistors without having to make them smaller. There are two major types of induced strain which are biaxial and uniaxial strain which are used to increase the carrier mobility in CMOS technologies. Longitudinal tensile strain (strain along the channel, making it longer) allows holes to move more quickly and smoothly. In biaxial tensile strain, the interatomic distances in the silicon crystal are stretched, generally

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increasing the mobility of holes making p-type transistors faster.

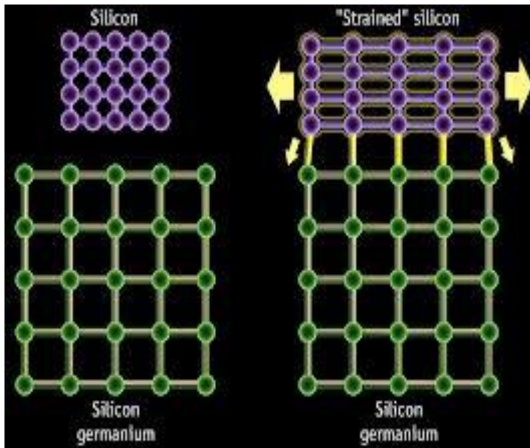

Fig. 1: strained silicon

The strong enhancement of hole and electron mobility via uniaxial stress has been known for 50 years. The difficulty in using uniaxial stress to improve the performance of complementary MOSFETs arises since it is difficult to improve both n- and pMOSFETs simultaneously [7] - [8].

The majority of the strained-Si work to date in the literature has focused on biaxial tensile stress introduced using a thick relaxed Si Ge substrate since this approach can potentially introduce advantageous strain for both n- and pMOSFETs [9], [10]. Biaxial strain using Si Ge has received much focus in recent years [11], [14] but has yet to be introduced into a CMOS logic technology for microprocessors due to process integration challenges; and most work showing near zero hole mobility improvement at large vertical electric fields [10]-[13] (typical operating region for high-performance nanoscale MOSFETs). Types of stress needed for enhanced carrier mobility is represented in table 1.

Types of stress needed for enhanced carrier mobility		
Direction	NMOS	PMOS
Longitudinal (along length of channel)	Tension	Compression
Transverse (along width of channel)	Tension	Tension
Out of Plane	Compression	Tension

Table 1: The effect of various stress on electron and holeMobility[6]

A. Mobility Enhancement With Strained-Si

A key scaling problem in nanoscale transistors is the mobility degradation caused by the large vertical electric fields. Fig. 2 represents the mobility versus technology scaling trend for various Intel process technologies. Mobility has decreased from 400 to 120 cm^2 /Vs during the last decade is also depicted in fig.2. It is becoming increasingly important to incorporate mobility enhancing process features in nanometer logic technology to counteract this undesirable mobility trend [9],[11]

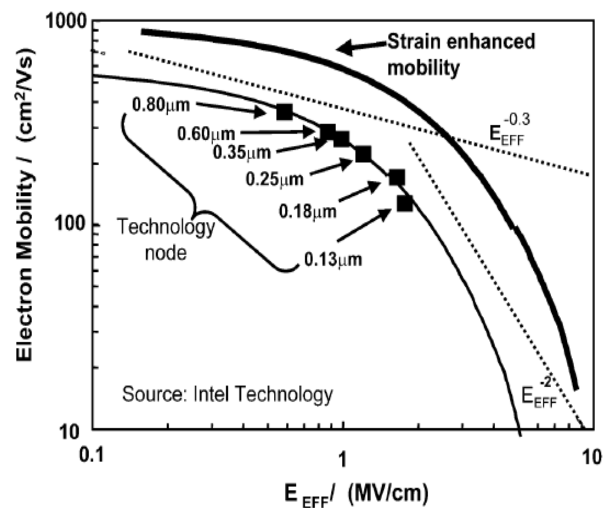

Fig. 2.Mobility versus technology scaling trend for Intel process technologies [2]

The mobility is extracted from the improvement in the linear current for the short channel device [1] using:

$$I_D = k(V_{GS} - V_T)(V_{DS} - I_D R_{SD})(V_{DS} = 50mV),$$

Where R_{SD} is measured independently. The field dependence of the mobility is also extracted using conventional techniques on a long channel transistor [1]. The physical mechanism for the large hole mobility enhancement at low stress and large vertical field has not been emphasised but can be inferred from the data using

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previous experimental and theoretical work [15]-[21].Summarizing references [15]–[21], the strain enhanced hole mobility understanding has lagged behindElectron [19], [22]. Fig. 3 reviews what is known about the hole band structure for unstrained and strained Si. The valence bands are plotted for the in-plane direction of the MOSFET. In the valence band, both uniaxial and biaxial stress lifts the degeneracy and causes shift and warping of the bands as depicted in Fig.3.

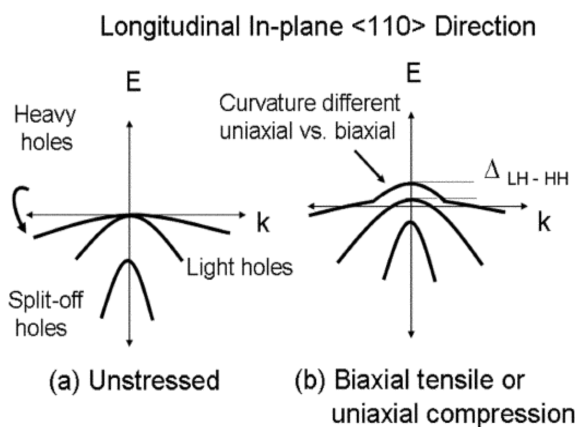

Fig. 3: Hole mobility for uniaxial strained-Si introduced Si Ge in the source and drain [12].

III. DEVICE STRUCTURE

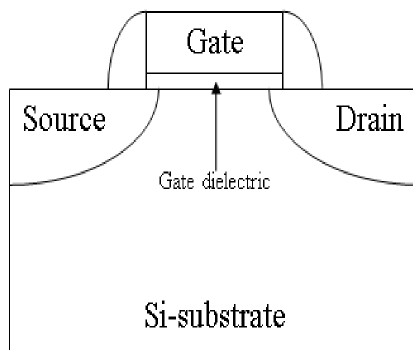

Fig. 4: Basic MOS transistor structure

The basic structure of MOS transistor is shown in fig.4. It is four terminal device which are gate, source, drain and substrate or body.NMOS transistor consists of a p-type silicon substrate into which two n^+regions, the source and the drain, are formed while PMOS transistor consists of a n-type silicon substrate into which two p^+regions, the source and the drain, are formed. Thegate electrode is usually made of metal or heavily doped polysilicon and is separated from by a thin SiO_2 film.

IV. FLOW CHART

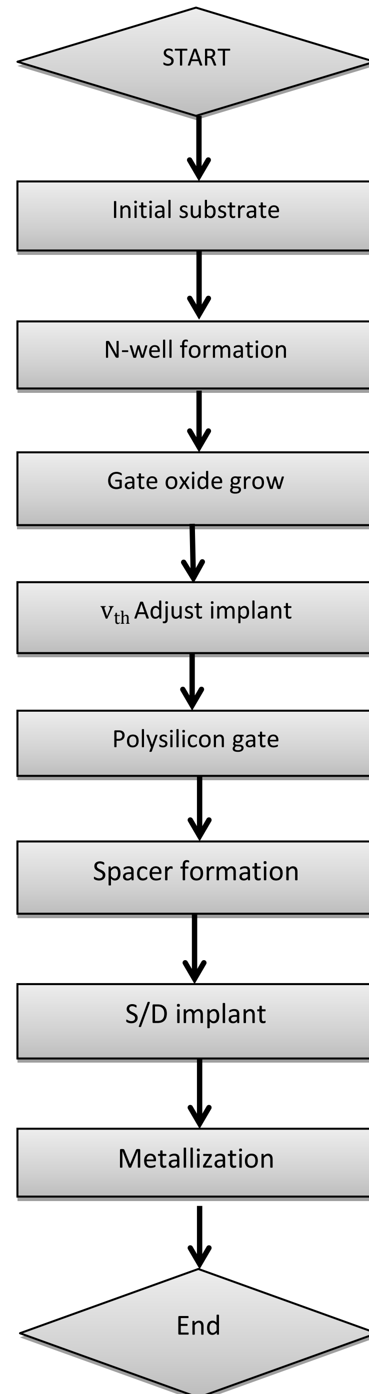

Fig.5: Flow chart for PMOS

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V. SIMULATION PROCESS

Process simulation of conventional PMOS and PMOS with SiGe layers were carried out by Athena simulator. Process of both strain silicon and conventional PMOS is almost same, only SiGe is deposited after n-well formation in the strained silicon PMOS. The fabrication of conventional 65nm PMOS device starts by forming initial silicon substrate p-type with phosphorus doping of 2 $x10^{15}cm^{-3}$. Then, we perform diffuse process to grow oxide. The process continues with the implantation of Boron 1 $x10^{15}cm^{-3}$ for adjust threshold voltage. After that polysilicon is deposited to form the gate. Finally, the final structure of the conventional 65nm PMOS is shown in Fig. 6.

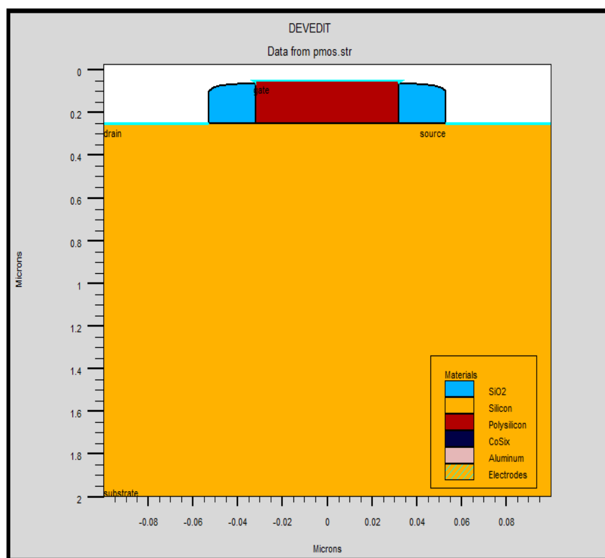

Fig. 6: Conventional 65nm PMOS

PMOS with strained silicon is formed by deposition of SiGe layer of thickness 0.015µm on silicon layer with thickness 0.010µm followed by another silicon layer of thickness 0.007µm.In SiGe layer, germanium concentration is taken as 0.35 which means SiGe layer consists of 35% Ge part. Finally, the final structure of the 65nm strained silicon PMOS is shown in Fig. 7.

Device simulation was performed by ATLAS simulator to find the I_D-V_G characteristic of each device. ForI_D-$V_G$characteristicV_G was varying from 0 to -2.0 V in each case. These two devices simulated with the same condition to compare and observe electrical characteristics between them.

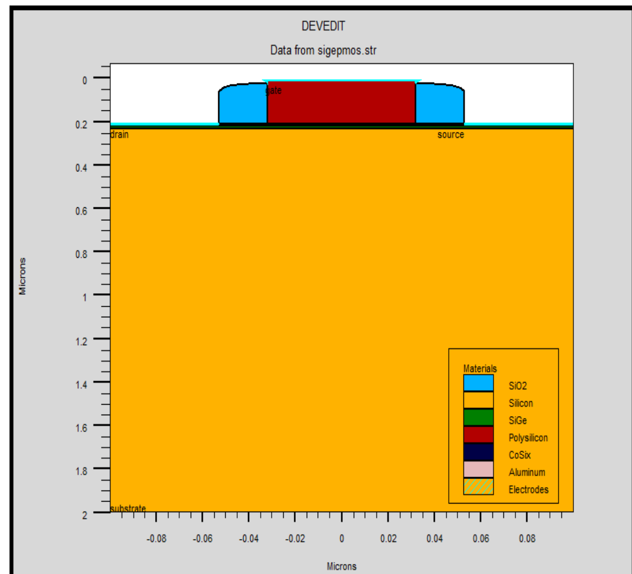

Fig.7: 65nm strained silicon PMOS

VI. SIMULATION METHOD

ATHENA is comprehensive simulation tool for modelling semiconductor fabrication processes.it provides facilities to perform efficient simulation analysis that substitute for costly real world experimentation. ATLAS is a physically-based two dimensional device simulator. It predicts the electrical behaviour of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation. ATHENA is frequently used in conjunction with the atlas device simulator. ATHENA predicts the physical structures that result from processing. These physical structures are used as input by ATLAS, which then predicts the electrical characteristics associated with specified bias conditions [23].

Tonyplot is a visualisation tool which gives the output window. Fig. 8 shows the process flow for simulation.

Fig.8: Simulation Flow

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VII. RESULTS AND DISCUSSION

The graph ofI_D-V_G is obtained through ATLAS simulator after the process simulation which is shown in following figure 9 and 10. I_D-V_G Curve for conventional PMOS and strained silicon PMOS is depicted in figure 9 and 10 respectively.

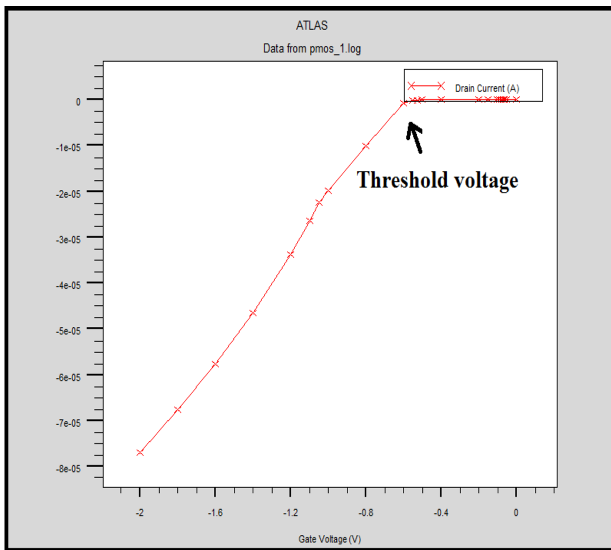

Fig.9: I_D-$V_G$curve for Conventional 65nm PMOS

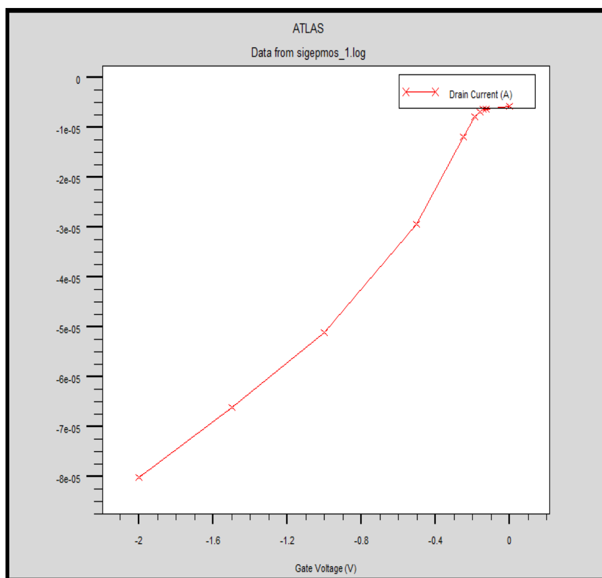

Fig.10: I_D-$V_G$curve for 65nm PMOS with strained silicon

The measured threshold voltage was -0.598 V with optimized threshold adjust of 1 x10^{15}atoms/$cm^{-3}$for PMOS transistor. From Fig.10, measured threshold voltage was -0.249V.It is clear that the strained PMOS has lower voltage threshold than the conventional PMOS which translates to lower power consumption.Fig.11 represents overlay plot of Fig.9 and Fig.10.

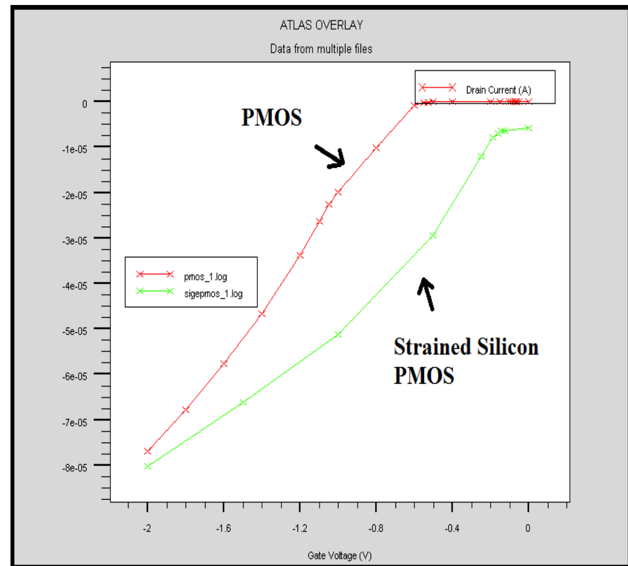

Fig.11: Overlay Plot

This result states that the silicon beneath the gate experience compressive stress during ion implantation process forming source and drain.

VIII. CONCLUSION

In this paper, we described a 65-nm PMOS transistor designed for high speed and low power operation. Strained silicon is added to enhance the performance of PMOS. Strained-Si channel transistors are added to continue Moore's law in the nanotechnology era. This article has mainly focused on the performance enhancement by channel strained silicon in PMOS Technology.

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BIOGRAPHY

Anil Kumar is Asst. Prof. at SHIATS-DU Allahabad. He obtained B.E (MMMEC,Gorkhpur) in ECE & M.Tech. (IIT BHU Formerly IT B.H.U.) in Microelectronics Engg. and presently pursuing Ph.D. He guided various projects & research at undergraduate & postgraduate level. He published many research paper in different journals. He has more than 10 years teaching. experience and actively involved in research and publications. His area of interest includes Antenna, microwave, artificial neural network and VLSI.

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