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A Roadmap on Very Long Instruction Word CPUs Family

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Abstract: Very long instruction word or VLIW refers to a processor architecture designed to take advantage of instruction set parallelism. This paper describes and compares the micro-architectural aspects and ISA rationale of TriMedia, C6000, SODA, EVP processors. This paper is useful which describes process specification of the 4 processors. The processors performances are discussed.

Keywords: VLIW, TriMedia, C6000, SODA, EVP

I. INTRODUCTION

Very long instruction word or VLIW refers to a processor architecture designed to take advantage of instruction level parallelism (IPL). Whereas conventional processors mostly allow programs that specify instructions to be executed at the same time (i.e. in parallel). This type of processor architecture is intended to allow higher performance without the inherent complexity of some other approaches. A processor that executes every instruction one after the other (i.e. a non-pipelined scalar architecture) use processor resources inefficient, potentially leading to poor performance. The performance can be improved by executing different sub-steps of sequential instructions simultaneously (this is pipelining), or even executing multiple instructions entirely simultaneously as in superscalar architectures. Further improvement can be achieved by executing instructions in an order different from the order they appear in the program, this is called out-of-order execution.

VLIW CPUs are usually constructed of multiple RISC-like functional units that operate independently. Contemporary VLIWs typically have four to eight main functional units. Compliers generate initial instruction sequences for the VlIW CPU in roughly the same manner that they do for traditional CPUs, generating a sequence of RISC-like instructions. The compiler analyzes this code for dependence relationships and resource requirements. It then schedules the instructions according to those constraints. In this process, independent instructions can be scheduled in parallel. Because VLIWs typically represent instructions scheduled in parallel with a longer instruction word that incorporates the individual instructions, this results in a much longer opcode (thus the term "very long") to specify what executes on given cycle.

This paper describes and compares the micro-architectural aspects and ISA rationale of 4 processors:

- the **TriMedia** mediaprocessor (NXP, formerly Philips Semiconductor),
- the **C6000** platform(Texas Instruments),
- the **SODA** architecture (University of Michigan)
- and the **EVP** (NXP).

These 4 processors can all be broadly categorized as application specific digital signal processors (DSPs). The first two processors (Trimedia and TI's C6000) are targeted as **media processors,** the latter two (SODA and EVP) are processors developed almost exclusively for **Software Defined Radio** (SDR).

II. GENERAL COMPARISION OF SDR PROCESSOR

2.1 Multimedia Processing

Multimedia processing is the handling of video and audio data in electronic devices. This is sometimes accomplished by specific purpose integrated circuits, but the lack of flexibility and high cost of this approach had led to the development of multimedia processors, programmable processors specially designed to efficiently execute all tasks related to multimedia processing.[5]

Multimedia processors achieve these goals by optimizing the execution of the multimedia tasks mentioned above. This implies:

- *High level of parallelism*: VLIW, SIMD to boost performance and to allow for a low cost silicon implementation.

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- *Large cache memories:* To accommodate typically large images and video frames close to the processor saving costly memory access and bandwidth.

- *Penalty free un-aligned memory access*: Processing algorithms typically access image blocks in an un-aligned manner.

- Data pre-fetching: Multimedia processing algorithms access memory locations in predictable strides and blocks.

- Large register files: Large data working sets can be kept in registers, preventing costly load and store operations.

- DMA-style memory transfers: Increases overall system performance.

- Application specific instructions: Typical multimedia operations can be done in one or a few clock cycles, saving energy and gaining performance.

- Small data words: 8 and 16-bit data words are typically sufficient for most multimedia processing tasks. Limiting the size of data words allows for higher memory density and parallelism.

TriMedia and TI C6000 are two competing families of multimedia microprocessors that is one way or another implement the architectural design choices listed above.

2.2Software–defined radio (SDR)

The physical layer of most wireless protocols is traditionally implemented in custom hardware to satisfy the heavy computational requirements while keeping power consumption to a minimum. These implementations are time consuming to design and difficult to verify. A programmable hardware platform capable of supporting software implementations of the physical layer, or **Software-define radio** (SDR), has a number of advantages: support for multiple protocols (i.e, multimode operation), faster time-to-market, higher chip volumes, and support for late implementation changes. SDR can be considered as a high-end digital processing (DSP) application[13].
The main design goals of these SDR processors are typically high performance (imposed by the high throughput requirements of current wireless protocols), energy efficiency (battery operated devices) and programmability (multi-protocol support, higher chip volumes).

III. MULTIMEDIA PROCESSOR

TriMedia is a family of microprocessors developed by NXP. The main application of the TriMedia microprocessors is multimedia data processing in embedded systems. This particular application domain shapes the TriMedia microprocessor design, diverging drastically from general purpose processors.
TriMedia processors are deployed on consumer devices as a System On Chip solution. TriMedia processors employ VLIW architecture.. VLIW and SIMD provide a high degree of instruction parallelism, optimizing the overall performance of the system.
The **TMS320 family** consists of 16-bit and 32-bit fixed- and floating-point DSPs. There are three main platforms, including the TMS320C2000 (control applications), the TMS320C5000 (power efficient applications), and the **TMS320C600** (high – performance applications). These processors are used in cell phones, digital cameras, modems etc.

3.1 Comparing TriMedia and TI C6000

TriMedia and TIC6000 achieve high performance, low power consumption and low unit cost by implementing the architectural features described in section 2.1. However, the details of how they accomplish each feature may differ between them. Each architectural feature implies design compromises that were sometimes solved differently in each processor.

3.1.1 High performance Parallelism on TriMedia

The algorithms required to implement video processing codecs are suitable for parallelization using VLIW and SIMD. They typically requires similar independent operations on multiple small data words. TriMedia processors provide instructions and super instructions that accomplish typical tasks in these codecs in few cycles and with minimum memory bandwidth consumptions. The VLIW in TriMedia is implemented with 5 issue slots and compressed with a 10-bit template field.
Parallelism on TIC6000 –VLIW and SIMD provide instruction and data level parallelism in the TI C6000. In addition, **compression** through stop bits is supported: parallelism of instructions in the fetched 256-bit VLIW can be controlled by using a stop bit, when setting the least significant bit (LSB) of the eight contained individual instructions to either 0 or 1. When set to 1, the individual instruction will be executed in parallel with the subsequent individual instruction. This allows eight instructions to be executed fully serial, partially serial or fully parallel.

Large register file on TriMedia –Video processing requires working with a large data set ; a large register file prevents overuse of expensive load and store instructions. TriMedia processor TMS3270 has a unified register file with 128 32-bit registers.

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Specific domain ISA instructions – Not all tasks found in video processing codecs are parallelizable, for example in H.264 Context-Based Adaptive Binary Arithmetic Coding (CABAC) intrinsic sequential behavior cannot be properly optimized with SIMD. The TriMedia ISA is equipped with several native instructions to simplify CABAC programming to compensate for this disadvantage and minimize sequential execution. TI C6000 provides also specific domain instructions designed to optimize the execution of image processing kernels.

Fixed-point arithmetic – On the TIC6000 processors fixed-point arithmetic is less computationally demanding than floating-point arithmetic, and thus a suitable design choice to increase arithmetic processing speed.

Prediction – Both families of processors allow instructions to be executed conditionally (prediction), thus reducing costly branching.

Delay slots- On the TIC6000, for fixed-point instructions, a number of delay slots are available. The number of delay slots is equivalent to the number of additional cycles required after the source operands are read for read for the result to be available for reading : for a multiply instruction this is 1, for a load this is 4, and for a branch this is 5.

3.1.2 Low power consumption Clock gating and frequency scaling on TriMedia – TriMedia applies two main power saving techniques: clock gating and voltage-frequency scaling. The latest TriMedia implements 70 clock domains, for example all stages of all functional units are gated. The normal supply voltage is 1.2V but the TriMedia guarantees normal operations at 0.8V at a lower frequency. The maximum operating frequency for the TM3270 is 350MHz, ample room for scaling down its frequency when processing typical tasks such as MP3 decoding (only 8 MHz needed).

Clustering on TI C6000- On the other hand, the TI C6000 family, to avoid a slow and power-hungry register file (read / write ports from each register to each of the 8 FUs) and a large forwarding network, two data paths (i.e. clusters) are available. This allows higher frequencies and lower power consumption.

TriMedia's register file is twice the size of the TI C60000 and is unified. In this way TriMedia designers choose to save memory bandwidth with a large register file and TI C6000 designers choose to save on power consumption and to reach higher frequencies with a smaller divided register file.

Memory access- On TI C6000, 4 interleaved single-ported memory banks assure lower power consumption. This however can lead to reduced performance in VLIW architecture. Only one access to each bank is allowed per cycle; if two parallel load instructions are both trying to access the same bank, one load must wait, resulting in a memory stall.

IV. SDR PROCESSORS: SODA AND EVP

SODA (Signal-processing On-Demand Architecture) is a (proposed) SDR processor architecture developed at the University of Michigan. The design goals are: high performance, energy efficiency, and programmability through a combination of features that include single-instruction multiple-data (SIMD) parallelism, and hardware optimized for 16-bit computations.The proposed programmable architecture has been implemented on 180 nm process technologies, and it is projected to meet the throughput and power requirements of current wireless protocols when implemented on 65 nm.

Embedded Vector Processor (EVP) is an application specific processor developed by NXP.EVP accomplishes this data and instruction level parallelism (vector processing and VLIW) and by providing application specific instructions.

Comparing SODA and EVP

High performance	**Energy efficiency**	**Programmability**
Multiple parallelism • VLIW • SIMD • Multiple cores (SODA only)	No branch prediction	VLIW/SIMD
Hardware optimized for 16-bit fixed-point operations	Fixed-point operations	
Scratchpad memory	No cache	
Special DSP instructions	Special DSP instructions	
	Separated SIMD memory	

Fig : Comparision of SODA and EVP

4.1 Wireless protocol characteristics

Wireless protocols are characterized by a number of specific properties, which have an important impact on the design of a DSP system.

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- **High Data-Level Parallelism** – Most of the computationally intensive DSP algorithms have abundant data level parallelism (for example the "searcher" in a W-CDMA protocol, can be represented by 320-wide vectors), much more than instruction level parallelism.[13]

- **8 to 16-bit data width –** Most algorithms operate on variables with small values. Analysis of two typical wireless protocols shows that there should be strong support for 8 and 16-bit fixed-point operations. 32-bit fixed-point operations and floating –point support is not necessary.[13].

- **Real –time requirements** – Strict real-time requirement in wireless protocols requires deterministic architectural behavior. Therefore features such as **caching, multi-threading** and **prediction** are not well suited.[13]

- **Vector operations –**Intravector operations (vector reductions) and shuffling of data within a vector is key to a number of common algorithms (e.g. FFT). Therefore specific, power and performance optimal, support for these operations should be provided.[16]

V. CONCLUSION

In this paper, we discuss the comparison of 4 processors such as TriMedia, C6000, SODA, EVP. The architecture and their performance are discussed as well. Each of the processor has advantage and disadvantage. The brief description of each architecture and their applications are mentioned.

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