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Low Power Op-Amp Design with Current Compensation Technique

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Abstract: The trends in electronic design field are growing day by day towards the low power chip design system. The need of smaller size chips with very small power dissipation increases the demand of low power designs. The supply voltage must be reduced to lower the overall power consumption of the system. In this paper ,we are presented a low power single output two stage CMOS operational amplifier (Op-Amp) with current buffer compensation technique operates in weak inversion region with a 1.8 V supply voltage. The two stage CMOS Op-Amp is designed in UMC 0.18µm CMOS technology. Since MOS transistor in sub-threshold region allows to work at low input bias current and low voltage, so the presented Op-Amp has very low power consumption with a high driving capabilities. The proposed Op-Amp has open loop gain =73.57db, the gain bandwidth product (GBW) 1.094 and 4.35µW power consumption.

Keywords: Two Stage CMOS Operational Amplifier (Op-Amp), Current Buffer Compensation, Power Dissipation, Low-Power, Low-Voltage, Power Consumption.

I. INTRODUCTION

The Operational Amplifier (Op-Amp) is undoubtedly one of the most useful devices in analog electronic circuitry.In designing an op-amp, various electrical characteristics, e.g. gain bandwidth, slew rate, common mode range, output swing, offset, power dissipation, all have to be taken into consideration. Op-Amps are designed with vastly different levels of complexity to be used to realise functions ranging from a simple dc bias generation to high speed amplifications or filtering. Power dissipation can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As we decrease input current, though power dissipation is reduced, but the dynamic range is degraded. As we decrease the supply voltage, it also becomes increasingly difficult to keep transistors in saturation condition. In order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology .[1]

CMOS Op-amp can be used very efficiently for practical consequences e.g designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op amps are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance, etc.[3]

II. OPERATIONAL AMPLIFIER (OP-AMP)

An operational amplifier (Op-Amp) is a DC coupled input voltage amplifier with high gain. It produces an output voltage a million times greater than the voltage difference across its two input terminals.

The general structure of op-amp is as shown in figure 1 below:-

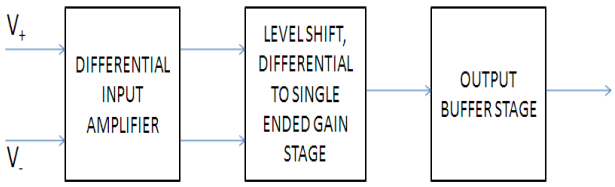

Fig.1. General Structure of Op-Amp

1. The first block is input differential amplifier, that provides very high input impedance, a large CMRR and PSRR, high gain, a low offset voltage, and low noise.

2. The second stage performs Level shifting, added gain and differential to single ended converter.

3. The third block is the output buffer. The output buffer sometimes may be replaced form a high output resistance un-buffered op-amp often referred to as Operational trans-conductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).

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III. APPLICATIONS OF LOW POWER OP-AMP

Low power op-amp circuits are required in battery operated devices. Low power Op-Amp can be used as a bio-potential amplifier. The main purpose of bio-potential amplifier is to amplify and filter extremely weak bio-potential signals.

The main areas to ponder while designing a bio-potential amplifier can be summarized as follows:

- High CMRR
- Low-noise for high signal quality.
- Ultra-low power dissipation for long-term power autonomy.
- Configurable gain and filter characteristics that suits the need of different bio-potential signals and different applications.

The best example of this is one of the most important electrophysiological measurements in medical diagnosis and patient care is that of the electrocardiogram (ECG or EKG).

IV. OP-AMP DESIGN WITH CURRENT BUFFER COMPENSATION TECHNIQUE

In the current buffer compensation technique, we remove the feed forward path from the output of the first stage to the output of Op-Amp. Circuit diagram for two stage op-amp with compensation block is shown below:-

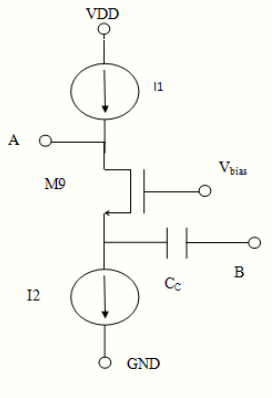

Fig.2. Current Buffer Compensation Block

The main criterion of this paper is to operate with lower power supply and achieving less power consumption by the op-amp design.

The main schematic of two stage op-amp with common gate current buffer compensation technique is shown below:-

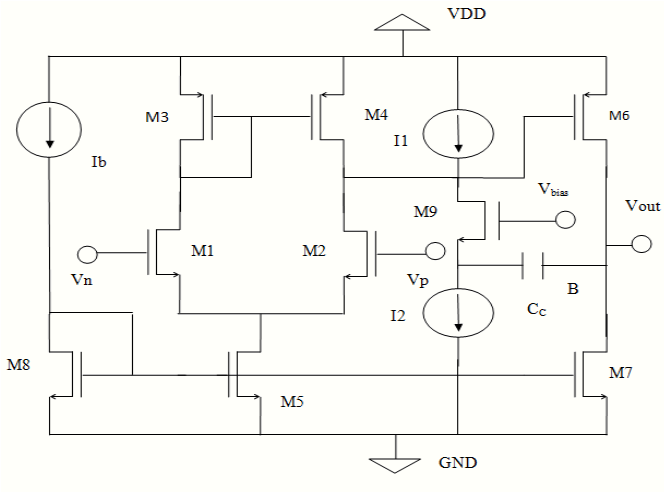

Fig.3. Schematic of Two Stage Op-Amp with Current Buffer Compensation Technique

The presented circuit consists of a cascode of Voltage to Current and Current to voltage stages.
First stage had a differential amplifier of NMOS transistor (M1,M2) converting the differential input voltage to differential currents. Which is then applied to a current mirror load of PMOS transistor (M3,M4) recovering the voltage. [9]

The second stage had common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. C_C is the compensation capacitor, required for the stability.

TABLE I
Sizes and Regions of Transistors Used

TRANSISTOR	SIZE	TYPE	REGION
M1.2	18.2/2	NMOS	SUB-TRESSHOLD
M5,8	0.336/2	NMOS	SATURATION
M7	1.68/2	NMOS	SATURATION
M9	0.388/2	NMOS	SATURATION
M3,4	0.252/2	PMOS	SATURATION
M6	2.526	PMOS	SATURATION
C_C	0.390pF	COMPENSAT-ION CAPACITOR	

V. RESULTS

The CMOS operational amplifier is simulated on Tanner EDA T-spice software for 0.18µm Technology to obtain the different parameter such as UGB (Unit gain bandwidth), gain, phase margin, CMRR, PSRR etc.

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TABLE II

PARAMETERS OBTAINED

PARAMETERS	VALUES
SUPPLY	1.8 V
CMOS TECHNOLOGY	0.18µm
GAIN	73.57 dB
UGB	1.094MHz
PHASE MARGIN	65.86º
CMRR	147.9dB
PSRR	88.84dB
POWER DISSIPATION	4.35µW

VI. CONCLUSION

Designing of low power low voltage op-amp with Current buffer compensated technique there is improvement of gain, bandwidth, phase margin CMRR, slew rate but power dissipation increases and PSRR decreases. Also, area requirement for current buffer compensation technique is very less as compared to RC compensation technique.

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