ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 12, December 2014

Implementation of reversible vedic multiplier for low latency and reduced resources utilization applications

K.SRINIVASA RAO[1], G.SANKARA RAO[2]

M.Tech Scholar [VLSI&ES], Swamy Vivekananda Engineering College, Bobbili, AP, India [1]

Sr. Assistant Professor, Swamy Vivekananda Engineering College, Bobbili, AP, India [2]

Abstract: Reversible computation is an emerging area of research, having applications in nanotechnology, low power design and quantum computing. It is proved that reversible logic has zero internal power dissipation. Multiplication plays an important role in the processors. It is one of the basic arithmetic operations and it requires more hardware resources and processing time than the other arithmetic operations. Vedic mathematic is the ancient Indian system of mathematic. It has a unique technique of calculations based on 16 Sutras. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhyam sutra which means vertical and crosswise. In this paper it is used for designing a low latency and reduced resources 4*4 Vedic multiplier. The important parameters in designing reversible logic circuits like no of flipflops,no of LUT's , Total Equivalent gate count for design are estimated and reported for our proposed reversible Vedic multiplier.

Keywords: Include at least 4 keywords or phrases

I. INTRODUCTION

multiplication is of immense importance in Digital Signal Processing (DSP) and Image Processing (IP). To implement the hardware module of Discrete Fourier Transformation (DFT), Discrete Cosine Transformation (DCT), Discrete Sine Transformation (DST) and modem broadband communications; large numbers of complex multipliers are required. Complex number multiplication is performed using four real number multiplications and two additions/ subtractions. In real number processing, carry needs to be propagated from the least significant bit (LSB) to the most significant bit (MSB) when binary partial products are added [1]. Therefore, the addition and subtraction after binary multiplications limit the overall speed. Many alternative method had so far been proposed for complex number multiplication [2-7] like algebraic transformation based implementation[2], bit-serial multiplication using offset binary and distributed arithmetic [3], the CORDIC (coordinate rotation digital computer) algorithm [4], the quadratic residue number system (QRNS) [5], and recently, the redundant complex number system (RCNS) [6]. Blahut et. al [2] proposed a technique for complex number multiplication, where the algebraic transformation was used.

This algebraic transformation saves one real multiplication, at the expense of three additions as compared to the direct method implementation. A left to right array [7] for the fast multiplication has been reported in 2005, and the method is not further extended for complex multiplication. But, all the above techniques require either large overhead for pre/postprocessing or long latency. Further many design issues like as speed, accuracy, design overhead, power consumption etc., should not be addressed for fast multiplication [8].

In algorithmic and structural levels, a lot of multiplication techniques had been developed to enhance the efficiency of the multiplier; which encounters the reduction of the partial products and/or the methods for their partial products addition, but the principle behind multiplication was same in all cases. Vedic Mathematics is the ancient system of Indian mathematics which has a unique technique of calculations based on 16 Sutras (Formulae). "Urdhva-tiryakbyham" is a Sanskrit word means vertically and crosswise formula is used for smaller number multiplication. "Nikhilam Navatascaramam Dasatah" also a Sanskrit term indicating "all from 9 and last from 10", formula is used for large number multiplication and subtraction. All these formulas are adopted from ancient Indian Vedic Mathematics.

In this work we formulate this mathematics for designing the complex multiplier architecture in transistor level with two clear goals in mind such as: i) Simplicity and modularity multiplications for VLSI implementations and ii) The elimination of carry propagation for rapid additions and subtractions. Mehta et al. have been proposed a multiplier design using "Urdhva-tiryakbyham" sutras, which was adopted from the Vedas. The formulation using this sutra is similar to the modem array multiplication, which also indicating the carry propagation issues. A multiplier design using "Nikhilam Navatascaramam Dasatah" sutras has been reported by Tiwari et. al in 2009, but he has not implemented the hardware module for multiplication. Multiplier implementation in the gate level (FPGA) using Vedic Mathematics has already been reported but to the best of our knowledge till date there is no report on transistor level (ASIC) implementation of such complex multiplier. By employing the Vedic mathematics, an N bit complex number multiplication was

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 12, December 2014

transformed into four multiplications for real and imaginary terms of the final product. "Nikhilam Navatascaramam Dasatah" sutra is used for the multiplication purpose, with less number of partial products generation, in comparison with array based multiplication.

When compared with existing methods such as the direct method or the strength reduction technique, our approach resulted not only in simplified arithmetic operations, but also in a regular array like structure. The multiplier is fully parameterized, so any configuration of input and output word-lengths could be elaborated. Transistor level implementation for perfomance parameters such as propagation delay, dynamic leakage power and dynamic switching power consumption calculation of the proposed method was calculated by spice spectre using 90 nm standard CMOS technology and compared with the other design like distributed arithmetic[3], parallel adder based implementation [1] and algebraic transfomation[2] based implementation. The calculated results revealed (16,16) x(16,16) complex multiplier have propagation delay only 4ns with 6.5 mW dynamic switching power.

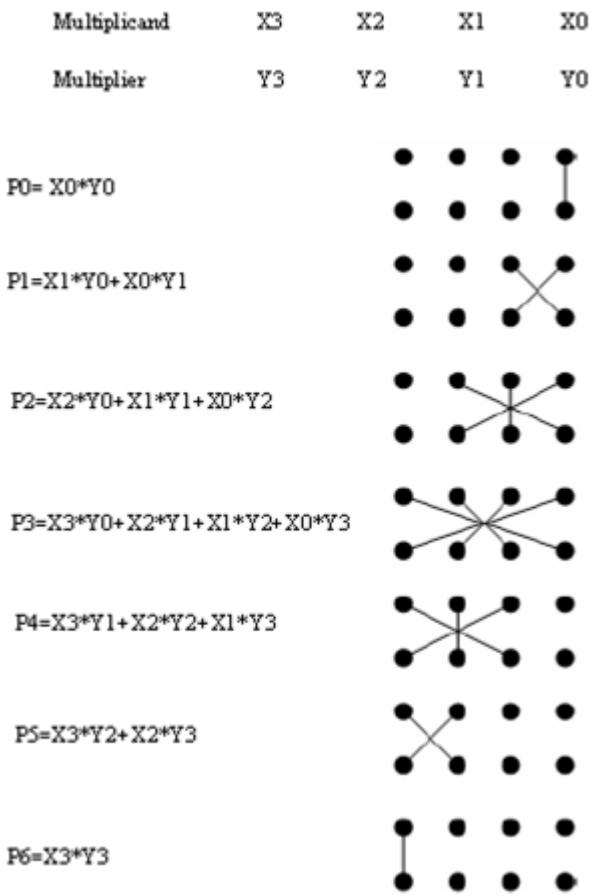
In this paper we report on a novel high speed complex multiplier design using ancient Indian Vedic mathematics. The paper is organized as follows; Mathematical fonnulation of the Vedic sutras and its application towards multiplier is described in below.

II. Description Of The Ancient Mathematical Technique

The description of the system study is given in this section The gifts of the ancient Indian mathematics in the world history of mathematical science are not well recognized. The contributions of saint and mathematician in the field of number theory, 'Sri Bharati Krsna Thirthaji Maharaja', in the form of Vedic Sutras (fomulas) [11] are significant for calculations. He had explored the mathematical potentials from Vedic primers and showed that the mathematical operations can be carried out mentally to produce fast answers using the Sutras.

In this paper we are concentrating on "Urdhva-tiryakbyham", and "Nikhilam Navatascaramam Dasatah" fonnulas and other fonnulas are beyond the scope of this paper. A. "Urdhva-tiryakbyham " Sutra The meaning of this sutra is "Vertically and crosswise" and it is applicable to all the multiplication operations. Fig. 1 represents the general multiplication procedure of the 4x4 multiplication. This procedure is simply known as array multiplication technique [12].

It is an efficient multiplication technique when the multiplier and multiplicand lengths are small, but for the larger length multiplication this technique is not suitable because a large amount of carry propagation delays are involved in these cases. To overcome this problem we are describing Nikhilam sutra for calculating the multiplication of two larger numbers.



Fig, I: Multiplication procedure using "Urdhva-tiryakbyham " sutra

B. "Nikhilam Navatascaramam Dasatah" Sutra Nikhilam sutra means "all from 9 and last from 10". Mathematical description of this sutra can be fonnulated as:

Assuming A and B are two n-bit numbers to be multiplied and their product is equals to P.

$$A = \sum_{i=0}^{n-1} A_i\, 10^i \quad \text{where } A_i \in \{0,1,\ldots\ldots 9\} \qquad (1)$$
$$B = \sum_{i=0}^{n-1} B_i\, 10^i \quad \text{where } B_i \in \{0,1,\ldots\ldots 9\} \qquad (2)$$

Multiplication Rule:

$$P = AB \qquad (3)$$

Equation (3) can be reformulated as by adding and subtracting the term $10^{2n}+10^n(A+B)$ in the right hand side

$$P = AB + 10^{2n} + 10^n(A+B) - 10^{2n} - 10^n(A+B) \qquad (4)$$
$$= \{10^n(A+B) - 10^{2n}\} + 10^{2n} - 10^n(A+B) + AB \qquad (5)$$

Equation no 5 can be derived for both the numbers if the number is greater than the base or less than the base.

If the number is greater than the base:

$$= 10^n\{(A+B) - 10^n\} + \{(10^n - A)(10^n - B)\} \qquad (6)$$

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 12, December 2014

f the number is less than the base:

$$= 10^n\{(A + B) - 10^n\} + \{(A - 10^n)(B - 10^n)\} \quad (7)$$

$$= 10^n\{A - (10^n - B)\} + \{(10^n - A)(10^n - B)\} \quad (8)$$

$$= 10^n(A - \bar{B}) + (\bar{A}\,\bar{B})\} \quad (9)$$

Where $\bar{A}$ and $\bar{B}$ are the 10^n's complement of A and B.

Subtraction Rule:

$$\bar{A} = 10^n - \sum_{i=0}^{n-1} A_i\, 10^i \quad (10)$$

$$= \sum_{i=1}^{n-1}(9 - A_i)10^i + (10 - A_0) \quad (11)$$

The serious drawback of Nikhilam sutra can be summarized as:

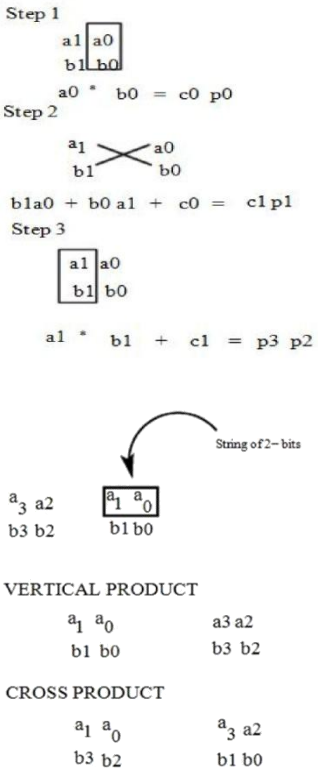
(i) Both the multiplier and multiplicand are less or greater than the base.

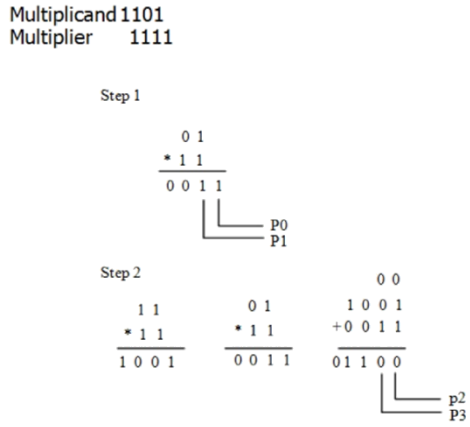
(ii) Multiplier and multiplicand are nearer to the base.

III. IMPLEMENTATION OF THE ALGORITHM

This section describes the steps to implement the ancient vedic technique in mathematics. As a first step Urdhva Tiryakbhyam technique is considered. It is the multiplication sutra (algorithm) in Vedic mathematics.Urdhva means vertical. Whereas Triyagbhyam means Crosswise. The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical and Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means vertically and crosswise. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number.

Steps of Urdhva Tiryakbhyam Sutra(Algorithm)





Extension of Vedic Multiplication Algorithm into Conventional Logic

Two Logic Blocks are needed to implement 4-bit multiplier. Four 2*2 Multiplier blocks and Three 4-bit Full Adder blocks are given in the Fig.1.

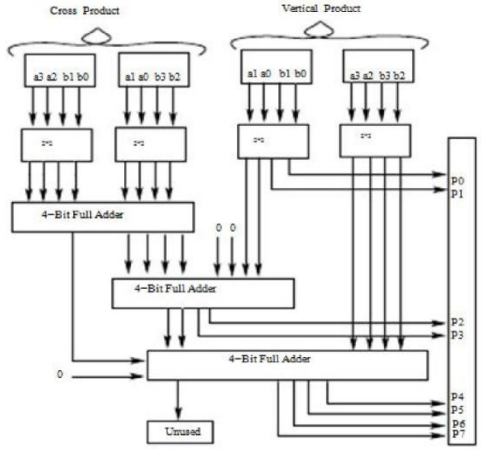


Fig.1: Architecture

IV. RESULTS

The results pertaining to the proposed technique are mentioned here in this sections. The schematic diagram followed by the output response for each model are presented subsequently here. Fig.2 presents the waveforms and Fig.3 and Fig.4 represents the Schematic output responses.

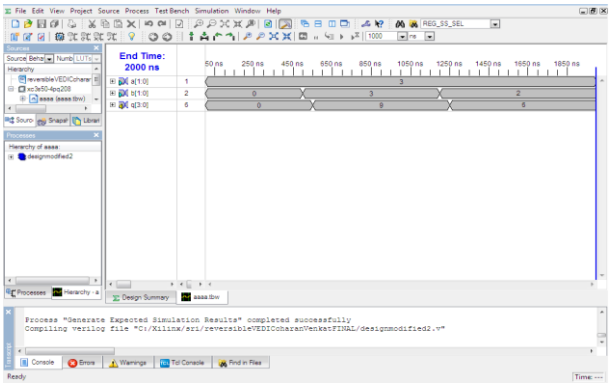


Fig.2: Waveform

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 12, December 2014

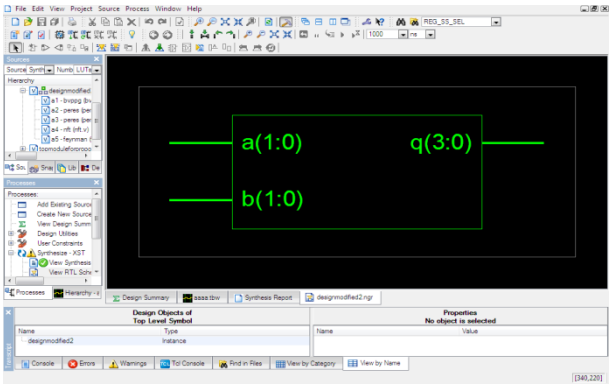


Fig.3: Schematic

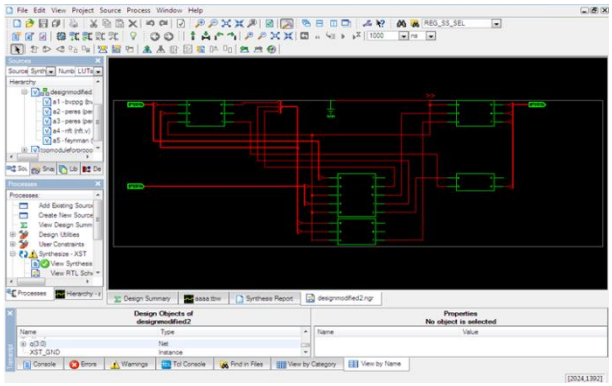


Fig.4: RTL Schematic

V. CONCLUSION

Simulation of the conventional model and the proposed vedic multiplier are presented in this paper. The proposed implementation of the vedic multiplier has shown. The implementation has paved a way to novel techinue of adopting ancient method.

REFERENCES

[1] Swami Bharati Krsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965
[2] Vedic Mathematics: http://www.hinduism.co.za/vedic.html.
R. Landauer,"Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.
[3] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
[4] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.
[5] A. Peres, Reversible logic and quantum computers, Phys. Rev. A 32 (1985) 3266–3276.
[6] E. Fredkin and T. Toffoli,"Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982.
[7] G Ganesh Kumarand V Charishma, Design of high speed vedic multiplier using vedic mathematics techniques, Itn'l J. of Scientific and Research Publications, Vol. 2 Issue 3 March 2012
[8] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.