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Efficient Fault–Handling of Reconfigurable Logic in SRAM using BIST and AGT

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Abstract: Fault tolerance is an important system metric for many operating environments. The conventional technique for improving system reliability is by replicating component, which uses the parameter such as cost, high design time, testing, consumption of power, volume. The proposed approach employs Adaptive group testing technique for stuck open fault and stuck short fault resolution. The Static Random Access Memory (SRAM) circuit is tested for its functionality. LFSR is used for generating the test patterns. These patterns are provided to circuit to check its functionality. A Group testing based fault resolution is incorporated into SRAM based reconfigurable Field Programmable Gate Array (FPGA) to provide an evolvable hardware system with self-organizing properties. This approach improves the performance of the system and develops new techniques for addressing BIST diagnosis method.

Key Words: SRAM, BIST, AGT, FPGA.

I. INTRODUCTION

Rapid advances in deep submicron and nanotechnologies are enabling engineers to design more complex integrated circuits (IC) and driving them toward new design paradigms like System-on-Chip (SOC) and Network-on-Chip (NOC). Such a design style allows reusing previous design and leading to shorter time to market and reduced cost. On the other side SOC designing makes external test increasingly difficult. Constantly increase in internal speed of SOC and the methods used in external testers is always one step behind. So Built-In Self-Test (BIST) has been the promising solution to the VLSI and SOC testing problem. BIST is used for detecting faulty components in a system by providing test logic on-chip.

Fault tolerant system is very important in system which requires high sustainability. Reconfigurable hardware builds an organic system to meet the principle of fault tolerant. FPGAs are the most widely used reconfigurable hardware in industries. FPGA uses Configurable Logic Blocks (CLBs) as flexible logics to implement large diverse applications. The reconfigurability of FPGAs provides a great level of freedom to realize the properties for fault-tolerant systems, which allows full adaptation to design failures and environmental change.

Since the transistor lines are very closely arranged to each other, so RAM circuits suffer from a very high average number of defects per unit chip area compared to other circuits. This motivated the research member to develop efficient RAM test sequences that provide good fault coverage.

A traditional algorithm takes very long test time for testing today's memory. For instance GALPAT and WALKING I/O require the test times of n^2 and $n^{3/2}$ order (where n is the number of bits in the chip). Zero-One and Checkerboard are older tests of order n, which have poor fault coverage. The memory testing time as a function of memory size is shown in table 1[10]

TABLE I
Testing time with memory size.

Size	Complexity			
n	n	$n \log n$	$n^{3/2}$	n^2
1K	0.0001s	0.001s	0.0033s	0.105s
4K	0.0004s	0.0048s	0.0262s	1.7s
16K	0.0016s	0.0224s	0.21s	27s
64K	0.0064s	0.1s	1.678s	7.17m
256K	0.0256s	0.46s	13.4s	1.9h
1M	0.102s	2.04s	1.83m	1.27d
4M	0.41s	9.02s	14.3m	20.39d
16M	1.64s	39.36s	1.9h	326d
64M	6.56s	2.843m	15.25h	14.3y
256M	26.24s	12.25m	5.1d	229y
1G	1.75m	52.48m	40.8d	3659y

II. RELATED WORK

The fault diagnosis methods based on previous approaches to test the memory include fault detection and isolation. Functional testing include coarse grained redundancy approaches such as Triple Modular Redundancy (TMR)[3], which rely on functional testing using a voting element. This supports the masking of a single faulty module for a given input vector. However, multiple faulty modules can leave the system unprotected as the quantity of spares in the system is fixed. TMR method is generated using the generic algorithm. In roving star approach latency is very high because of sequential nature. Iterative Logic Array and array based technique are put to test under serialized inputs.

Combinatorial group testing [2] has been done on BIST based diagnosis. The main problem of testing is to find the subset of defective member. Fault location can be done with high precision by using testing methods such as batching, digging, jumping and doubling on selected

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benchmark circuit. The drawback of this system it can be tested only when the FPGA is in offline.

This paper extends the technique to an automated diagnostic methodology which can be used for different cores, that takes into account the different operating modes. The method is scalable to different FPGA families. Further, these techniques can be readily adapted to provide test coverage of various faults. Using a single test pattern all the blocks can be tested at one time. Group testing techniques are used for generating a non-adaptive test that involves concurrent execution of a single group tests. The test provides the full coverage for all system of a type present in the chip by dividing the blocks. By generating, and comparing the outputs produced by the blocks in response to the test pattern, complete fault coverage is achieved under a single test.

III. PROPOSED WORK

The proposed work employs adaptive group testing to test the memory blocks. The memory blocks are divided into different small blocks which are applied for testing. The blocks which are tested is called block under test (BUT). If there are n blocks then it is divided into n/4=k blocks. These blocks are tested in single stage for isolating the faults. The comparator compares the output from the blocks provides the pass or fail signal based on the discrepancies as shown in figure 1.

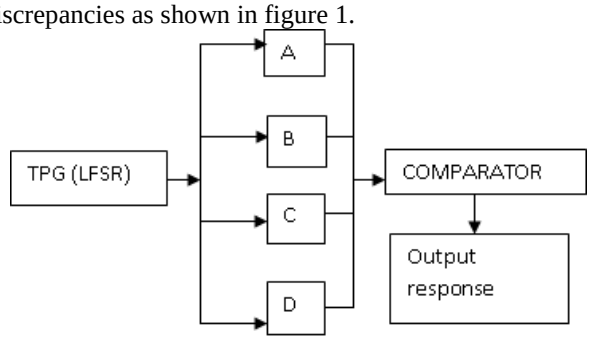

Fig 1 BIST structure for testing a group of 4 blocks

For a group of 4 BUTs, a total of six comparators are required to compare each BUT's output with that of all the other BUTs in the same group. For purposes of simplicity, BIST model in its smallest scale, considering one such group of 4 BUTs, named A, B, C, D. It is assumed that these blocks have been tested for correct functionality.

The test pattern generation is done using a LFSR for testing the memory blocks for different inputs. The technique uses TPG and the ORA for comparing the outputs of the 4 BUTs in group $\boldsymbol{k} = 1$. The test routine is used for testing the signal. Termination of the test is done followed by the propagation of the test results. At each clock cycle the results are compared and ensured that these defective blocks does not go undetected.

An LFSR is a shift registers that, when clocked, moves the signal from one bit to the next MSB. Some of the outputs are joined in exclusive-OR configuration to form a feedback mechanism. A LFSR can be designed by performing EX-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops. LFSR make extremely good pseudorandom pattern generators. The seed value is loaded and the LFSR is clocked, it will give a pseudorandom pattern of 1s and 0s. If the seed is all 0 states, then the LFSR will be stuck at all 0 states as the feedback logic is EXOR gate.

MEMORY FAULT MODEL

Classical faults are not enough to test the SRAM. Functional faults are used for testing the memory. Memory faults are classified as shown in figure 2.

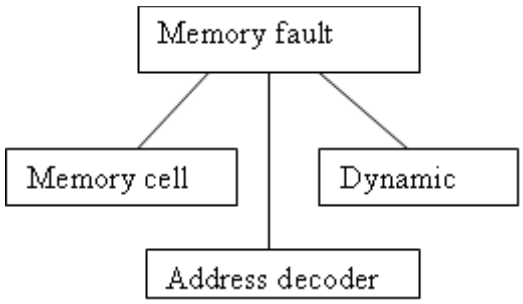

Fig 2 functional fault models classification

The fault models employed in SRAM testing are not sufficient to test the effect produced by some defects. Due to the improvement in the manufacturing process and memory architecture leads to new fault models. The presence of open and short fault is more due to ever-growing no of interconnection between the layers.it is reported that open/short via are the most common root causes for the faults occurring in the circuit

In these fault models memory cell fault model such as stuck open fault (SOF) and stuck short fault (SSF) are isolated.

- A short in a circuit is formed when two points are connected when it is not intended to be connected.
- An open result from the breaking of a connection.

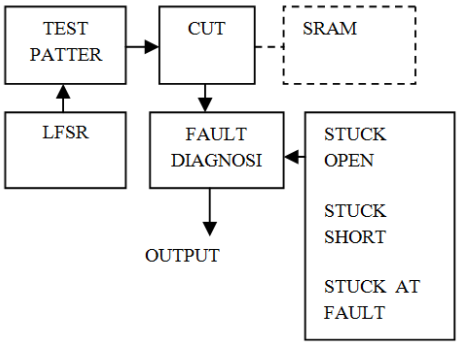

Fig 3 block diagram of fault diagnosis using BIST

A stuck-open fault (SOF) occurs when the cell cannot be accessed due to a broken word line. When a read operation is performed to this cell it will produce the previously read value. Stuck-On fault model is the Complement of the Stuck-Open fault model. The prediction of stuck on fault is difficult. Fault diagnosis using BIST is shown in figure 3

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ADAPTIVE GROUP TESTING

The clock and matrix m is initialized which keeps track of the discrepancy counts of the resources. As shown in figure 4 all elements in the matrix are initialized to zero. As a stage of tests proceeds the reset is initialized to zero now the configuration is selected at random and the test Patterns are applied to CUT.

The SRAM contain an array of cells where the data is stored. The data from the cell is retrieved

Over time, suspect resources are identified. Under a single-fault assumption, maximum no of faults is detected. if faulty resource is identified and fault is isolated the process is terminated else again test pattern is applied to test for the defect in the circuit. The AGT algorithm has three phases of fault isolation which is done after the fault detected. In the initialization phase, the elements are initialized to zero. In addition, since the isolation procedure is yet to begin, the set of suspect resources is equal to the set of resources under test. After initializing the configurations the first stage of test is created, and then the second phase of testing is done.

The third phase consists of performing tests on the configuration thus created. Repetition of phase two and phase three is done until the defective resource is isolated. During the fault isolation, random test vectors are applied to isolate the fault which emulates the data stream for the first test stage. This process is continued until static is attained. After the static is achieved new test stage is created.

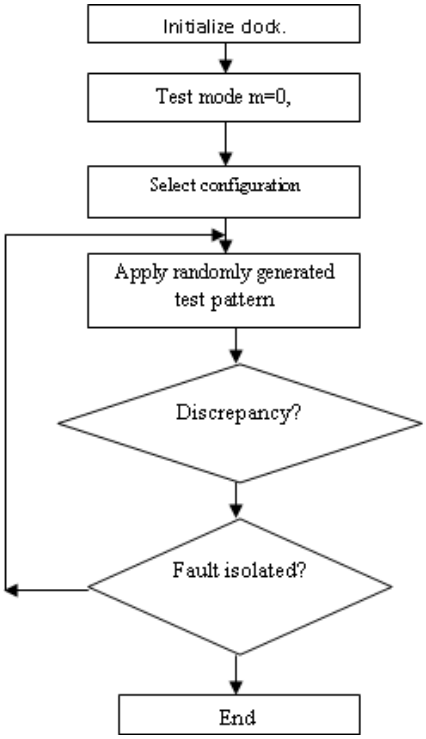

Fig 4 Adaptive Group Testing

IV. SIMULATION RESULT

Mentor graphics modelsim is used to check the functionality and fault coverage using VHDL coded BIST module.

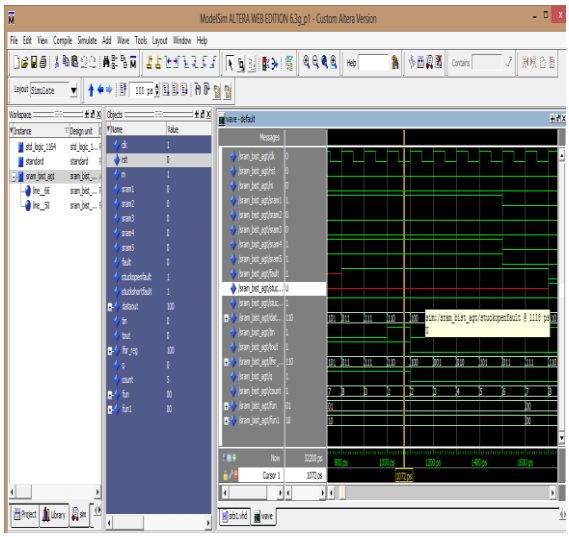

Fig 5 simulation result with stuck open fault

The simulation results in the above figure 5 shows the stuck open fault in which the data line is open which results in failure. The input for clock, test mode and reset is initialized to zero and simulation is made to run. The faulty output is obtained.

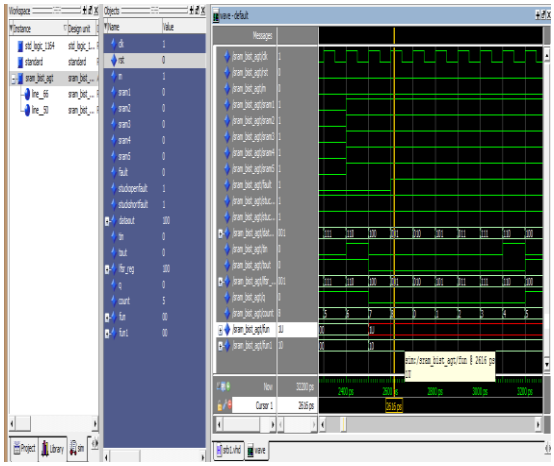

Fig 6 simulation result with functional fault

The simulation result in figure 6 shows the functional fault which occurs in the circuit. The inputs are initialized and simulation is run. The functional fault is obtained.

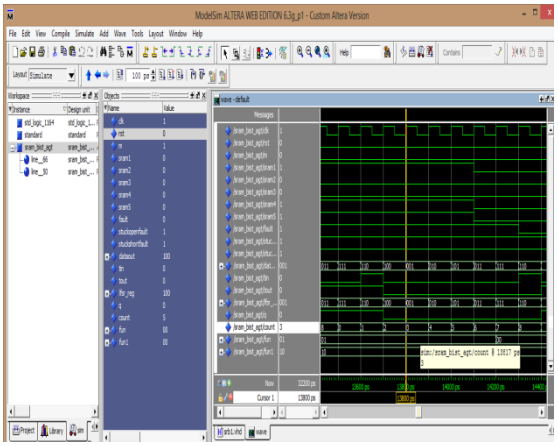

Fig 7 simulation result without fault

The above figure7 shows the simulation result where the data is provided to the circuit and there is open or short in the circuit so the correct output is obtained.

V.CONCLUSION

An organic, adaptive group testing-based method to tolerate faults on FPGAs is presented. The self-monitoring, self-reconfiguring self-healing and self-maintaining capabilities of the AGT based approach enable the system to achieve life-like behavior in respect to isolate faults, and maintain the pre-defined system goals. The AGT system exploits the redundant modules to carry out the normal operation during repair process. In all experiments, the approach successfully identifies a known-good set of resources, and the prime realization to replace the fault-affect configuration. In this simple logical fault models applicable to digital memories and the corresponding test procedures are explained .The advantage of logical models is that they have enough detail to adequately model a good number of faults like stuck open fault, stuck short fault etc. and at the same time simple to handle.

Further, partial reconfiguration can be exploited to handle some permanent faults adaptively with minimum perturbation to system operation and reduced reconfiguration time. Different fault models can be done for detecting various faults.

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