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Exploiting the Body of MOS Devices for High Performance Analog Design

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Abstract: In this paper we will discuss some techniques that can be applied to many conventional analog building blocks in order to improve their performance (such as gain and linearity) and decreasing their supply demand. Experimental prototypes have been implemented and tested, showing that the proposed techniques are promising candidates for enhanced analog IC design in nanoscale technologies

Keywords: Low voltage Amplifier, Transimpedence Amplifier, Current mirrors, Transconductors, Gain Boasting, Body Effect.

I. INTRODUCTION

The body (or bulk) terminal of CMOS transistors was once known principally for the adverse consequences of the so called body effect that is a change of the transistor threshold voltage, VT, due to a nonzero source to bulk voltage which, for an n-channel MOS transistor, is expressed $\mathbf{V_T = V_{T0} + \gamma \{(2\Phi_F - V_{BS})^{1/2} - (2\Phi_F)^{1/2}\}}$ where V_{T0} is the zero-bias threshold, Φ_F is the Fermi potential and γ is the body effect parameter. In the last years however, the foregoing effect has been favorably exploited, mainly by digital designers, to counteract the limitations incurred by deep submicron and nanoscale CMOS devices. For instance, reverse body bias, which increases the threshold voltage of transistors, was applied to reduce the subthreshold leakage during active burn-in and stand- by operation and to compensate for intradie and interdie parameter variations.

Besides, forward body bias was used in to design a 1-GHz communication router operating at 1.1-V supply, whereas adaptive body bias and dynamic voltage scaling were adopted to decrease the power consumption in microprocessors. Finally, body bias was exploited for yield optimization of digital CMOS circuits. The bulk terminal has also been utilized by analog designers to face the progressive supply voltage reduction. To enable body driving, the gate must be biased to form a conduction channel inversion layer and the drain current can be modulated by varying the bulk voltage through the body effect. The bulk-driven transistor is hence a depletion-type device which can work under negative, zero, or even slightly positive source-bulk voltages. Compared to conventional gate-driven circuits, the body-driven ones are characterized by a lower achievable voltage gain and/ or bandwidth as well as increased noise, caused by the limited transconductance value nevertheless, several body-driven implementations have been proposed for low-frequency low-gain applications.

II. BODY EFFECT

In many applications the source terminal is connected to the substrate (or body) terminal B, which results in the pn junction between the substrate and the induced channel having a constant zero (cutoff) bias. In such a case the substrate does not play any role in circuit operation and its existence can be ignored altogether. Body driven circuits are analyzed for application to low power, low supply demand, increasing the gain & bandwidth limit etc.

In integrated circuits, however, the substrate is usually common to many MOS transistors. In order to maintain the cut off condition for all the substrate-to-channel junctions, the substrate is usually connected to the most negative power supply in an NMOS circuit (the most positive in a PMOS circuit). The resulting reverse-bias voltage between source and body (V_{SB} in an w-channel device) will have an effect on device operation. To appreciate this fact, consider an NMOS transistor and let its substrate be made negative relative to the source. The reverse bias voltage will widen the depletion region. This in turn reduces the channel depth. To return the channel to its former state, V_{GS} has to be increased. The effect of V_{SB} on the channel can be most conveniently represented as a change in the threshold voltage V_T, Specifically, it has been shown that increasing the reverse substrate bias voltage V_{SB} results in an increase in V, according to the above relationship given in an introduction.

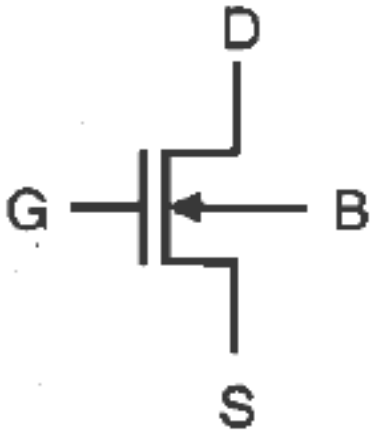

Fig. 1. N-MOS with Body Terminal

where V_{T0} is the threshold voltage for $V_{SB} = 0$; γ is a physical parameter with (2<f>f) typically 0.6 V.

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A. Zero Body Biasing

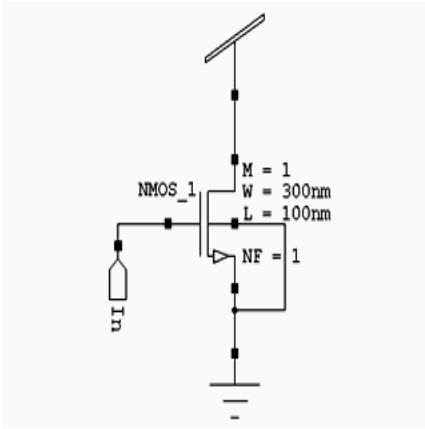

Fig. 2(a). N-MOS with Zero Body Biasing

In fig. 2(a). body terminal of N-MOS is connected to the source terminal, drain terminal is connected to the supply voltage and source is connected to the ground terminal. So, body to source voltage is zero (V_{BS}= 0V). A dc voltage is applied at the gate terminal of the transistor.

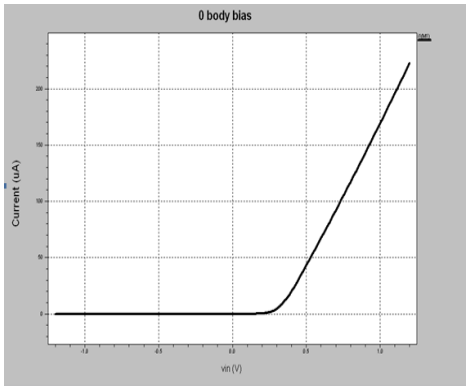

Fig. 2(b). N-MOS with Zero Body Biasing

Fig. 2(b). shows the current characteristics of zero body biased N-MOS transistor. We design the solution in 100nm & illustrative result of circuit in fig. 2(a) is shown in table. I.

B. Positive Body Biasing

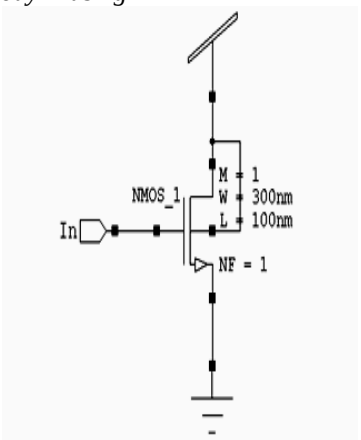

Fig. 3(a). N-MOS with Positive Body Biasing

In fig .3(a). body terminal of N-MOS is connected to the drain terminal, drain terminal is connected to the supply voltage and source is connected to the ground terminal. So, body to source voltage is not zero ($V_{BS}\neq$ 0V) and acquires a positive value. A dc voltage is applied at the gate terminal of the transistor.

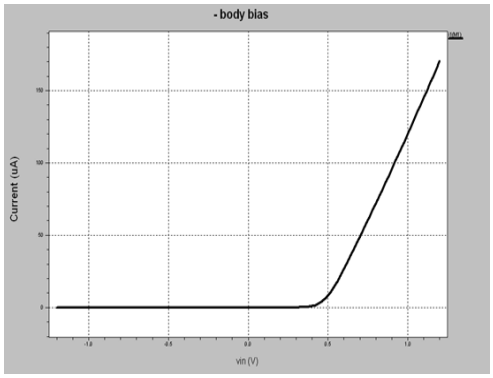

Fig. 3(b). N-MOS with Positive Body Biasing

Fig. 3(b). shows the current characteristics of positive body biased N-MOS transistor. We design the solution in 100nm & illustrative result of circuit in fig. 3(a). is shown in table. I.

C. Negative Body Biasing

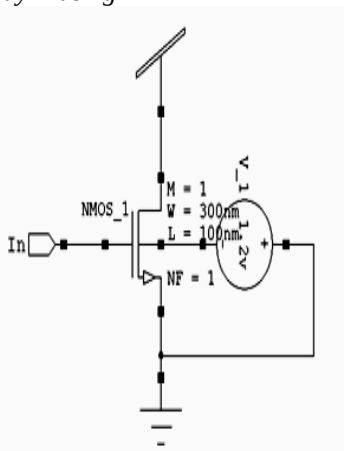

Fig. 4(a). N-MOS with Negative Body Biasing

In fig. 4(a). body terminal of N-MOS is connected to the negative voltage source , drain terminal is connected to the supply voltage and source is connected to the ground terminal. So, body to source voltage is not zero ($V_{BS}\neq$ 0V) and acquires a negative value. A dc voltage is applied at the gate terminal of the transistor

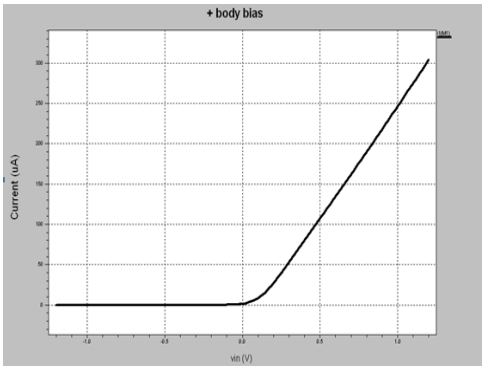

Fig. 4(b). N-MOS with Negative Body Biasing

Fig. 4(b). shows the current characteristics of negative body biased N-MOS transistor. We design the solution in 100nm & illustrative result of circuit in fig. 4(a). is shown in table. I.

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TABLE I Performance Comparison of Various Type of Biasing

Type of Biasing	Drain Current (I_D)	Threshold Voltage(V_{TH})	Trans conductance(G_M)
Zero Biasing	222.63µA	182.05mV	267.00µA/V
Positive Biasing	264.49µA	31.14mV	274.79µA/V
Negative Biasing	7.28µA	505.10mV	6.533µA/V

III. BODY REPLICA BIASING

The first technique we discuss here is a replica biasing approach that allows the quiescent current of a MOS device to be accurately set through its body terminal. It can be applied for example to set the standby current in a class AB output stage or in a minimum-supply differential pair while improving its common-mode rejection ratio.

A. Class AB Output Stage with Quiescent Current Control

Let us consider the well-known two-stage Miller operational amplifier. It is made up of an input source-coupled pair (M1-M2) with mirror load (M3-M4) and a second stage (M5 and M6). The gates of M5-M6 are tied together and directly connected to the output of the first stage Miller compensation through capacitor Cc across the second stage is also shown. This solution enables class AB operation at the output, since the maximum achievable output current in the positive and negative transition is independent of the quiescent current of M5 and M6 but is determined by the minimum and maximum voltage at the output of the first stage and by the chosen aspect ratio of M5-M6. Among all the possible alternatives, this output stage topology is the simplest one and for this reason it maximizes the output swing. The main drawback of this solution, that prevents its use in practical applications, is related to the ill definition of the quiescent current in the output branch (M5-M6). Its value cannot be set accurately, since it strongly depends on the matching properties of M5 and M6 (that have different channel type), on the quiescent output voltage of the first stage and on the supply voltages.

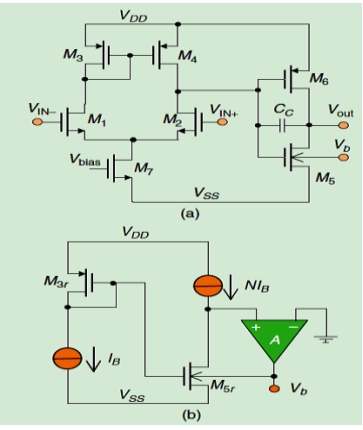

Fig. 2(a) Simplified schematic of the class AB OTA and (b) Simplified schematic of the biasing Circuit generating V_b.

This means that parameters related to this current (like output transconductance and dc power dissipation) are subject to large variations. With the proposed body-biasing technique, we exploit the bulk terminal of M5 to control the quiescent current of the output branch. The body voltage is set through a suitable feedback control section based on a replica bias. We assume that the desired quiescent current of M5-M6 is N times the quiescent current of M3 (and M4). Therefore, the aspect ratio of M6 is N times that of M3-M4 in order to equalize the V_{DS} voltage of M3-M4 (and M1-M2) and, consequently, to avoid systematic offset due to bias inequalities of the source-coupled pair.

1) Simulation Result of Class AB OTA

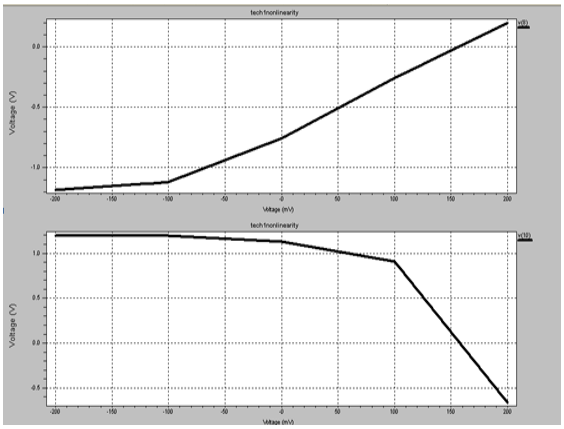

Fig. 5(a). Output waveform of the class AB OTA

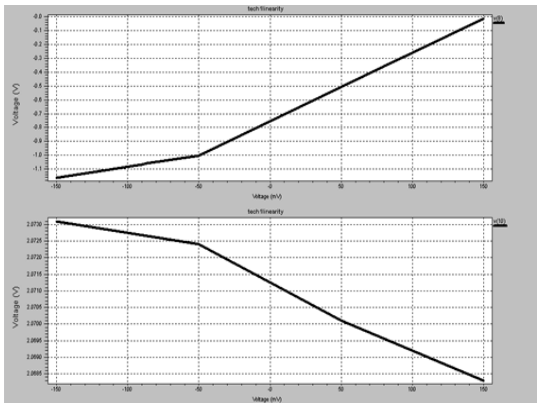

Fig. 5(b). Output waveform of the class AB OTA on applying body biasing

IV. CONCLUSION

In this work, Body driven circuits are analyzed for application to low power, low supply demand, increasing the gain and bandwidth limit etc. It is well known that the analog performance of nanoscale devices is and will be further impaired by the ultralow supply voltages adopted. In this paper we reviewed several techniques developed by the authors that can be profitably exploited to enhance the gain/ accuracy, linearity and/or reduce the minimum supply demand of analog building blocks designed in deep nanometer CMOS processes. Specifically, we described the following new circuits:class AB output stage for transconductance amplifiers with well defined quiescent current control.

The proposed approaches are based on the exploitation of the bulk of MOS transistors as an additional control terminal to be embedded in a local negative feedback loop. At this purpose, either continuous-time. or switched-capacitor feedback networks were adopted. The former are preferred when linearity performance is to be maximized. Of course, a the use of these technique requires that the bulk-to-source voltage must be limited to about 0.3V, so as to avoid that the bulk-source junction becomes appreciably forward biased and conducts a significant current. The solutions were studied analytically and validated through either experimental measurements or computer simulations. The obtained results were found in good agreement with the expected ones.

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