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Multicarrier Sinusoidal PWM Technique Based Analysis of Asymmetrical and Symmetrical 3Φ Cascaded MLI

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Abstract: This work proposes a comparison study of cascaded H-bridge multilevel inverter (CHBMLI) in which symmetrical and asymmetrical arrangement of five level and seven level H-bridge inverters are compared in order to find an optimized output voltage quality with lower harmonic distortion. Several studies have been conducted on the three phase cascaded symmetrical multilevel inverter (MLI).However, there are few studies that actually discuss or evaluate the performance of three phase H-bridge asymmetrical MLI. Here, three multicarrier pulse width modulation (PWM) techniques such as constant switching frequency, variable switching frequency and phase shifted PWM are proposed. MATLAB/SIMULINK software is used for simulation. The carried out simulation studies shows that an asymmetrical configuration provides high output voltage with very low total harmonic distortion (THD) using less switching devices.

Keywords: MLI, PWM, Multi Carrier, MATLAB, THD

I. INTRODUCTION

Multilevel inverter is a power electronic converter built to synthesize a desired AC voltage waveform from several levels of DC voltages. Here, the DC levels were considered to be identical in that all of them were batteries, solar cells, capacitors etc [1] [2]. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. Multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, fuel cells can be easily interfaced to a multilevel inverter system for a high power application [1][3]. The output voltage quality of the MLI is improved as the number of voltage level increases, so the quantity of output filters can be decreased. On the other hand, solutions with a low number of levels need a large and expensive LC output filter [4].A multilevel inverter has several advantages over a conventional two level inverter that uses a high switching frequency PWM. Multilevel inverter not only generates the output voltage with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. It can operate at both fundamental frequency and high switching frequency PWM. One particular disadvantage is that it requires more number of power semiconductor switches. The most common topologies of MLI are Diode-Clamped or Neutral Point Clamped MLI, Flying capacitor MLI and Cascaded H-bridge MLI [5]. The cascaded inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. With an aim to reduce the number of dc sources required for the cascaded MLI, this paper focuses mainly on asymmetric MLI that uses unequal dc sources in each phase to generate a seven level equal step multilevel output[11]. In symmetrical MLI, all H-bridge cells are fed by equal voltages and hence all arm cells produce similar output voltage steps[9]. In asymmetrical MLI, all arm cells are not fed by equal voltages. In this inverter, the arm cells have different effect on the output voltage. To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used. It is proposed to choose the dc-voltages sources according to a geometric progression with a factor of 2 or 3[4][12].

I. THREE PHASE CASCADED MULTILEVEL INVERTER

A basic structure of a cascaded MLI is shown in Fig.1.

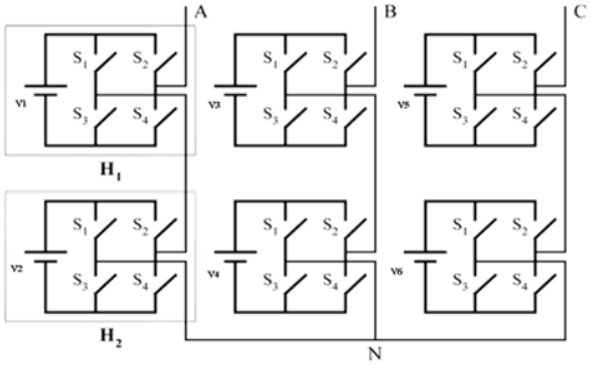

Fig. 1 Three phase cascaded multilevel inverter

It synthesizes a medium voltage output based on a series connection of power cells which use standard low voltage component configurations.

Each SDC (separate DC source) is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Through different combinations of the four switches, S_1-

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S_4, each converter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs.

$$V_0(t) = V_{0,1}(t) + V_{0,2}(t) + \ldots\ldots\ldots + V_{0,N}(t) \quad (1)$$

where N is the number of cascaded bridges.

If all the voltage sources in Fig.1 are equal to V_{dc} then the inverter becomes symmetrical MLI. The effective number of output voltage levels m in symmetric multilevel inverter is given by

$$m=2N+1 \quad (2)$$

The maximum output voltage is then,

$$V_{0max}=N\,V_{dc} \quad (3)$$

If the voltage sources V_1, V_3, V_5 is equal to V_{dc} and V_2, V_4 and V_6 is equal to $2V_{dc}$ the inverter becomes asymmetrical. The number of output voltage levels m in asymmetric multilevel inverter is given by

$$m=2^{N+1}-1, \quad \text{if } V_{dc,j}=2^{j-1}V_{dc} \quad (4)$$

The maximum output voltage of this N cascaded multilevel inverter is given by

$$V_{0max}=\sum_{j=1}^{n} V_{dc,j} \quad (5)$$

III. MULTICARRIER MODULATION STRATEGIES

The proposed asymmetric MLI is performed using multicarrier modulation techniques [6]. Three techniques such as constant switching frequency, variable switching frequency and phase shifted PWM [7] are implemented. Carriers used in MLI may be vertically shifted or horizontally shifted. In this paper, both vertical shifted and horizontal shifted carriers are taken for the analysis. The general principle of a carrier based PWM is the comparison of a reference waveform with a carrier waveform, this typically being a triangular waveform [8]. The carrier frequency defines the switching frequency of the converter and the high order harmonic component of the output voltage.

Subharmonic PWM is otherwise known as sinusoidal PWM (SPWM). Sinusoidal PWM for MLI is based on classic two level SPWM. But, the difference between two level SPWM and multilevel SPWM is the number of carriers used in multilevel SPWM. For an m-level inverter using bipolar multicarrier technique, (m-1) carriers with the same frequency f_c and same peak to peak amplitude A_c are used. The reference waveform has the amplitude A_m and frequency f_m and it is centred above the zero level. The reference wave is continuously compared with each of the carrier signals. If the reference wave is greater than a carrier signal, then the active device corresponding to the carrier are switched on. Otherwise the devices switch off. The frequency ratio m_f is defined as $m_f=f_c/f_m$. The amplitude modulation index m_a is defined as $m_a=2A_m/(m-1)A_c$.

IV. CONTROL TECHNIQUES FOR ASYMMETRICAL MLI

If the voltage sources in Fig.1 are V_{dc} and $2V_{dc}$, then it is asymmetrical MLI and it produces seven levels of output voltage such as $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0,$-V_{dc}$, $-2V_{dc}$,$-3V_{dc}$. The control techniques for asymmetrical MLI are as follows.

A. Constant Switching Frequency PWM (CSFPWM)

The constant switching frequency pulse width modulation technique is most popular and very simple switching scheme. For m level inverter, all (m-1) carriers use same frequency f_c and the same amplitude A_c and they are disposed such that the bands they occupy are contiguous. It is further subdivided into

- Phase Disposition PWM (PDPWM)
- Phase Opposition Disposition PWM(PODPWM)
- Alternate Phase Opposition Disposition PWM(APODPWM)

1) *PDPWM:* In PDPWM technique, all triangular carriers are arranged in phase.
2) *PODPWM:* In PODPWM technique, the carriers above the zero reference are in phase, but shifted by 180° below the zero reference.
3) *APODPWM:* In APODPWM technique, each triangular carrier is shifted by 180° from its adjacent carrier.

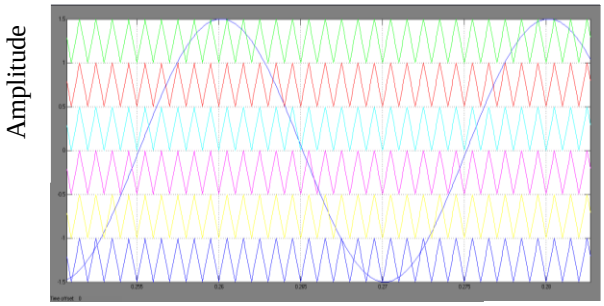

Fig.2 CSF PDPWM

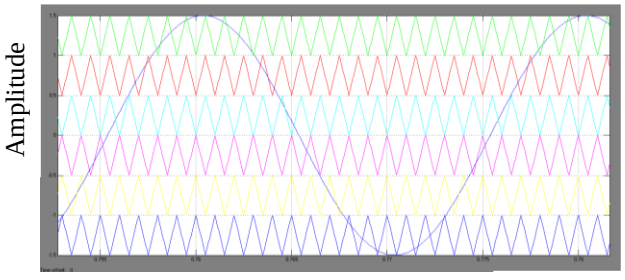

Fig.3 CSF PODPWM

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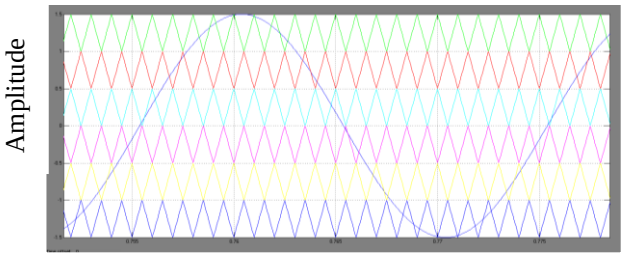


Fig.4 CSF APODPWM

Fig.2 to Fig.4 shows the multicarrier signal for constant switching frequency PWM techniques.

B. Variable Switching Frequency PWM (VSFPWM)

The number of switching for upper and lower devices is much more than that of intermediate switches in constant switching frequency carriers. In order to equalize the number of switching for all switches, variable frequency PWM is used. Here the carrier sets C1 and C6 will have the same frequencies, C2 and C5 will have the same frequencies and C3 and C4 will have the same frequencies.Fig.5 shows the multicarrier signal for variable switching frequency PWM.

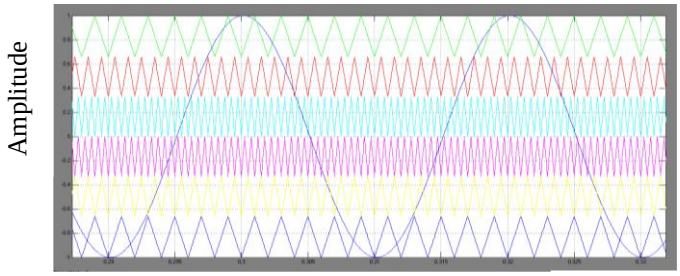


Fig.5 VSF PWM

C.Phase Shifted PWM (PSPWM)

Each cell is modulated independently using unipolar and bipolar pulse width modulation respectively, which provides the even power distribution among the cells. A carrier phase shift of 180°/m is introduced across the cells to generate stepped multilevel output with lower distortion[10].Fig.6 shows the multicarrier signal for phase shifted PWM. It uses m-1 carriers with same amplitude and frequency which are shifted by 90° to one another to generate the output voltage.

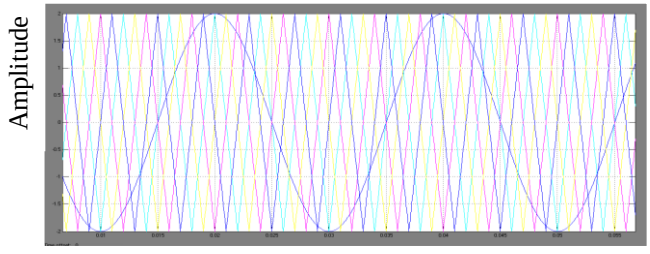


Fig.6 PS PWM

V. SIMULATION

In order to analyse and to test the proposed topology, simulations are conducted by MATLAB/SIMULINK software. The above mentioned PWM techniques have been implemented for both three phase five level symmetrical and seven level asymmetrical multilevel inverter.

A.Design Parameters

The simulation parameters for three phase symmetrical multilevel inverter with RL load are as follows

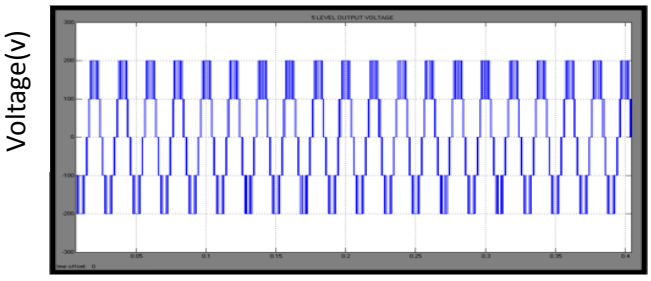
Input DC voltage,	V_{dc} =100V
Reference switching frequency,	f_m =50Hz
Carrier switching frequency,	f_c =2 kHz
Three Phase Load,	R =15 Ω, L=25mH

The simulation parameters for three phase asymmetrical multilevel inverter with RL load are as follows

Input dc voltage,	V_{dc1}=100V & V_{dc2}=200V
Reference switching frequency,	f_m =50Hz
Carrier switching frequency,	f_c =2 kHz
Three Phase Load,	R =15 Ω, L=25mH

B.Symmetrical MLI

To verify the results of symmetrical MLI, simulations have been conducted for several multicarrier PWM techniques as mentioned above. The five level output voltage waveforms of the symmetrical MLI are shown in Fig.7.



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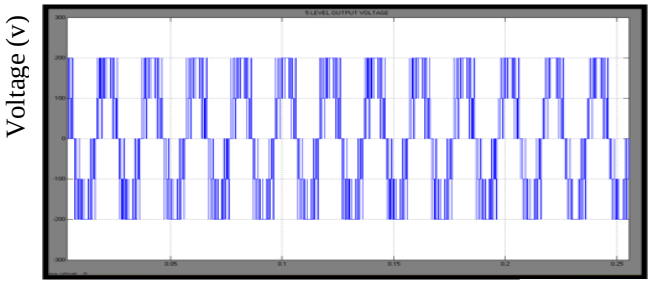

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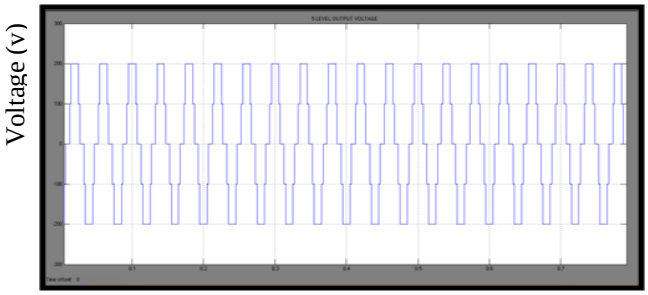
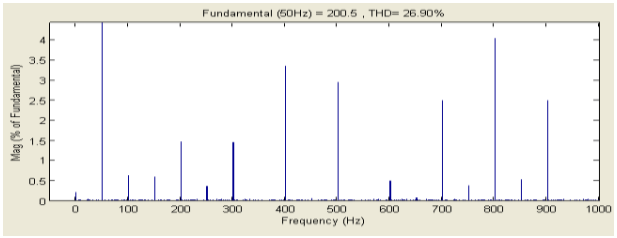


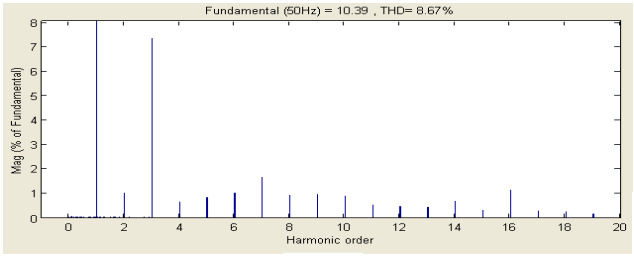
(c)

Fig.7. Output phase voltage waveform for symmetric MLI (5 level) using
(a) Constant switching frequency
(b)Variable switching frequency
(c)Phase shifted PWM

The total harmonic distortion of the above techniques are observed using FFT analysis. The voltage and current harmonic spectrums are shown in Fig.8.



(a)



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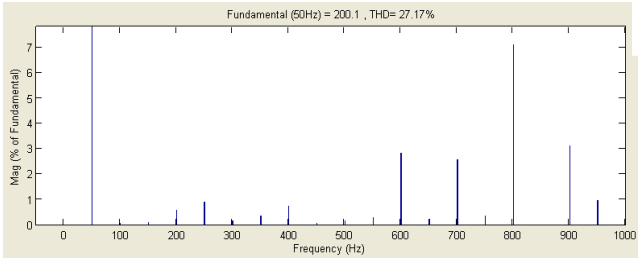

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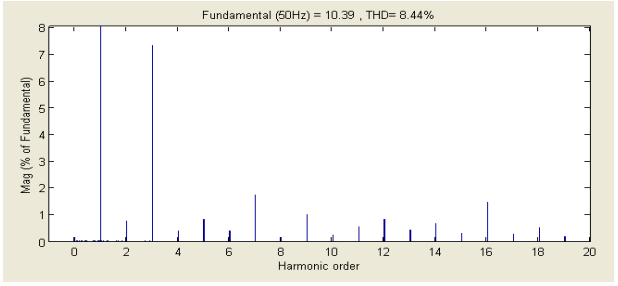

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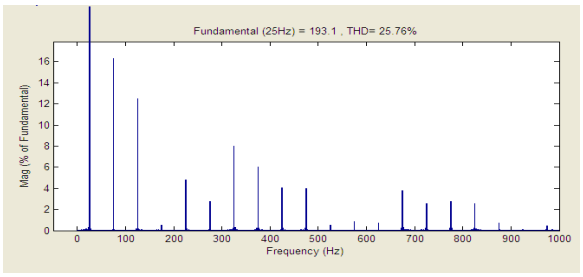

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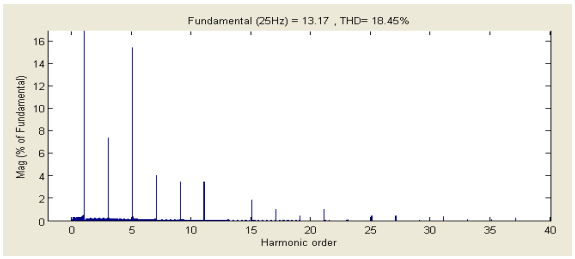
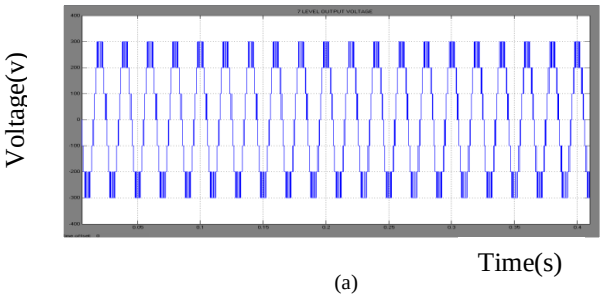


(f)

Fig.8. Voltage and current harmonic spectrum for
(a) & (b) Constant switching frequency
(c) & (d) Variable switching frequency
(e) & (f) Phase shifted PWM

C.*Asymmetrical MLI*

To verify the proposed asymmetrical MLI, simulations have been conducted for several multicarrier PWM techniques and the obtained results are compared with symmetrical MLI. Fig.9 shows the output phase voltage waveform for constant switching frequency PWM technique.



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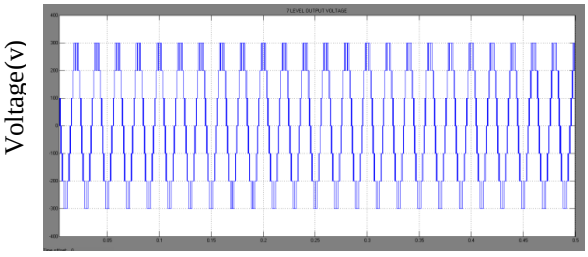

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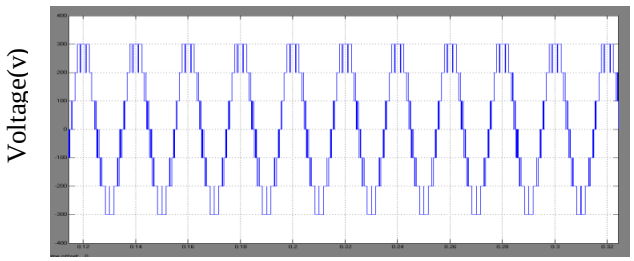
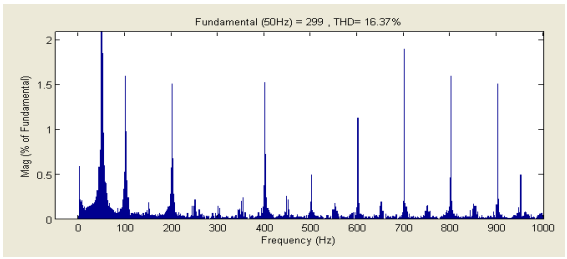


(c)

Fig.9. Output phase voltage waveform for constant switching frequency asymmetric MLI (7 level) using
(a) PDPWM
(b)PODPWM
(c)APODPWM

The voltage and current harmonic spectrums for various constant switching frequency PWM techniques is shown in Fig.10.



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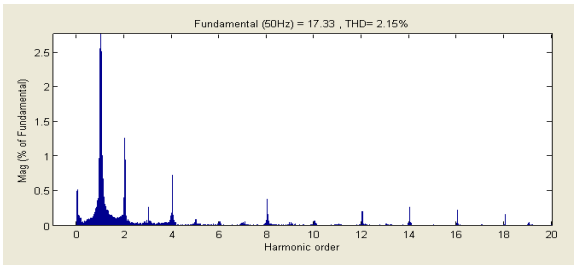

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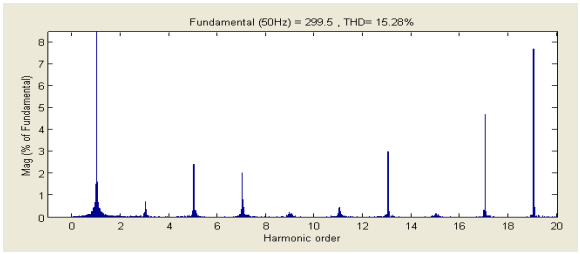

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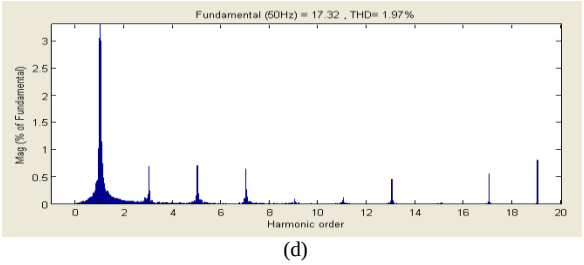

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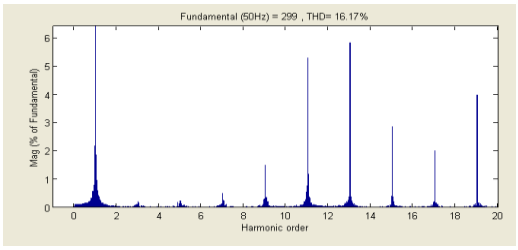

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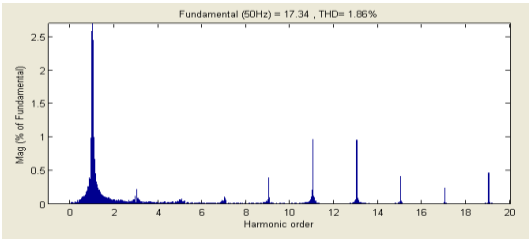
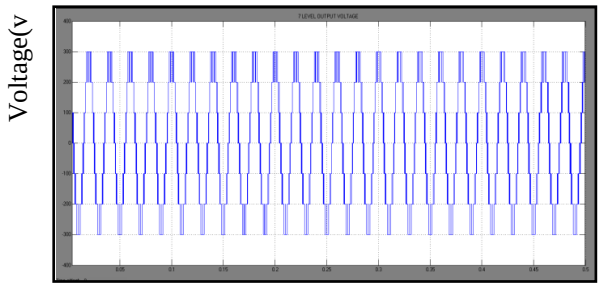


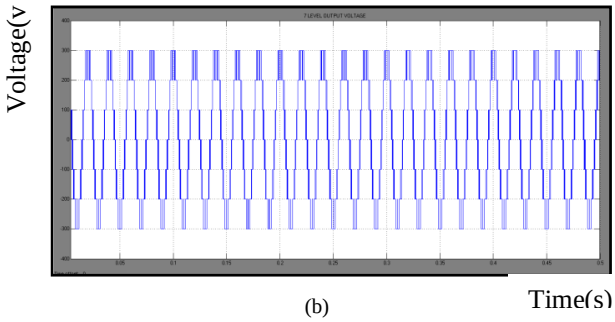
(f)

Fig.10. Voltage and current harmonic spectrum for constant switching frequency
(a) & (b) PDPWM
(e) & (d) PODPWM
(e) & (f) APODPWM

Figure.11 shows the seven level output voltage waveform for variable switching frequency PWM and phase shifted PWM.



(a)



(b)

Fig.11. Output phase voltage waveform for asymmetric MLI (7level) using
(a) Variable switching frequency
(b) Phase shifted PWM

The voltage and current harmonic spectrums for variable switching frequency and phase shifted PWM is shown in Fig.12.

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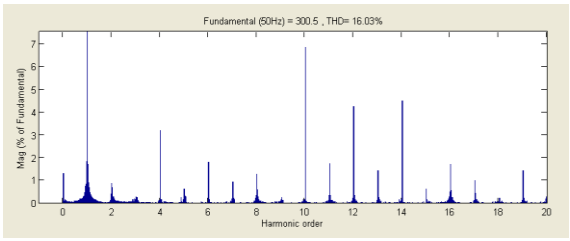

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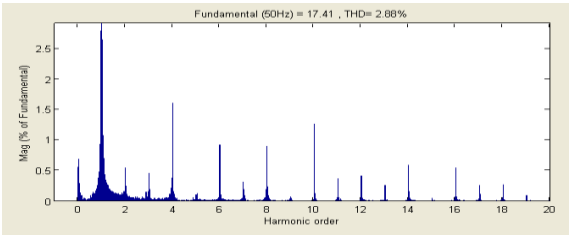

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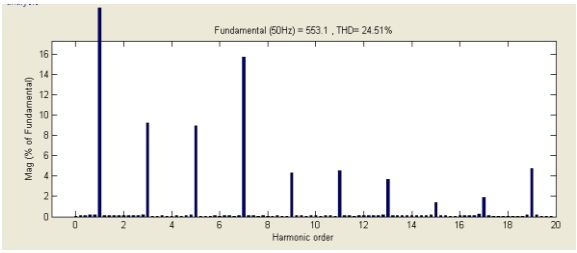

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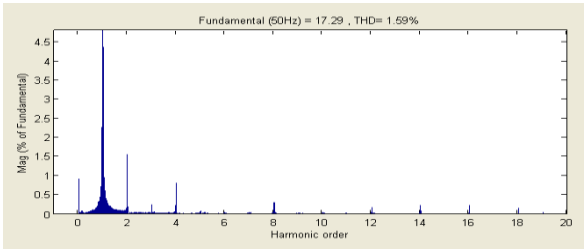

(d)

Fig.12. Voltage and current harmonic spectrum for
(a) & (b)Variable switching frequency
(c) & (d) Phase shifted PWM

The root mean square (RMS) value of the output voltage and total harmonic distortion of voltage and current were compared for both symmetrical MLI and asymmetrical MLI. Table I shows the performance comparison of symmetrical and asymmetrical multilevel inverter. The readings were taken for various values of R and RL loads.

The maximum output voltage for the symmetrical multilevel inverter is 150.3V and for asymmetrical multilevel inverter it is 218.2V.The minimum voltage and current harmonic for symmetrical MLI is 25.76% and 8.35% respectively. The minimum voltage and current harmonic for asymmetrical MLI is 15.28% and 1.59% respectively. From the Table I it is clear that, by using same circuit configuration the magnitude of the output voltage is greater in asymmetrical MLI than symmetrical MLI and it also shows that the total harmonic distortion is lesser in asymmetrical MLI.

TABLE I
PERFORMANCE COMPARISON OF SYMMETRICAL AND ASYMMETRICAL MLI

	Symmetrical			Asymmetrical		
	THD_V (%)	THD_I (%)	V_0	THD_V (%)	THD_I (%)	V_0
CSFPD	26.91	8.67	146.8	16.37	2.15	215.6
CSFPOD	26.26	8.67	146.2	15.28	1.97	215.2
CSFAPOD	26.11	8.35	146.5	16.17	1.86	216.0
VSFPWM	27.18	8.44	146.6	16.03	2.88	216.4
PSPWM	25.76	18.45	150.3	24.51	1.59	218.2

VI. CONCLUSION

In this paper, three different schemes the constant switching frequency, variable switching frequency and phase shifted pulse width modulation are incorporated. Indeed, symmetrical and asymmetrical arrangements of five and seven level H-bridge inverters have been compared in order to find an optimum arrangement with lower harmonic distortion and optimized voltage quality. It is clear from the simulation results that the asymmetrical configuration provides nearly sinusoidal voltages with very low voltage and current harmonics when compared to symmetrical MLI. Also, it is confirmed that the number of switches for symmetrical and asymmetrical multilevel inverter is same. For same circuit configuration, the magnitude and number of levels of the output voltage of asymmetrical MLI is higher than that of the symmetrical MLI.

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