Energy Efficient Advanced Low Power CMOS Design to reduce power consumption in Deep Submicron Technologies in CMOS Circuit for VLSI Design

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Abstract: Low power has emerged as a principal theme in today's electronic industry. Energy efficiency is one of the most critical features of modern electronic systems designed for high speed and portable applications. Reduction of power consumption makes a device more reliable and efficient. The minimum amount of power consumption was a major driving force behind the development of CMOS technologies. As a outcome, CMOS technology are best known for low power consumption devices. However, for minimizing the power consumption of system or device, simply knowing that CMOS devices may consume less power than equivalent devices from other technologies does not help much. It is important to know not only how to calculate power consumption, but also to calculate how various factors such as input voltage level, input rise time, source leakage current, Gate current, Switching power, short-circuit power, power-dissipating capacitor, and output loading affect the power requirement of a device. This paper presents an energy efficient and ecofriendly technique for overcoming power consumption in a CMOS devices, focusing on calculation of power-dissipation in various components and, finally, the determination of various ways to reduce the total power consumption in a CMOS device. The proposed technique has less power dissipation when compared to the conventional CMOS design style also the proposed technique is advantageous in many of the low power digital circuit design applications.
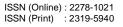
Keywords: low power, energy efficient, digital circuits, source leakage current, gate current leakage, switching power, short circuit, reverse biased diode leakage, Sub-threshold Current Leakage, Gate oxide Tunneling Leakage.

I.   INTRODUCTION

Power consumption is one of the top issues in VLSI circuit design, for which CMOS is the prominent technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Mobile battery-powered electronic devices have created a growing demand for energy-efficient circuit design. Cellular phones alone represent a large industry and create both an opportunity for innovation and the potential for profitability. Future progress in mobile electronics will depend on the development of inexpensive devices with complex functionality and long battery life. Even before the mobile era, power consumption has been a major concern. To overcome problem related to power dissipation, many scientists and researchers have proposed various energy efficient techniques from the device level to the architectural level. However, there is no universal technique to cut tradeoffs between power consumtion, delay and area and so, designers are required to select suitable and efficient techniques that satisfy application and product needs[7]. The aim of this paper is to show how devices, circuits, and architectures within this design space may be optimized for minimum energy consumption. Even in the realm of high-performance microprocessors, power has become a limiting constraint. Traditional scaling of high performance FETs uses a combination of supply-voltage (Vdd) and threshold voltage (Vth) reduction to accommodate both performance and power requirements, but the rapid rise of sub threshold and gate leakage has placed limits on this scaling strategy. It is clear that new strategies are necessary to address the power concerns in high performance designs.

There are several VLSI techniques to reduce leakage power, input rise time, source leakage current, Gate current, Switching power, short-circuit power, power in capacitance, and also dissipation in output loading affect the power consumption of a device. Each technique provides an efficient way to reduce power loss, but disadvantages of each technique limit the application of each technique. Previous techniques are summarized and compared with our new approach presented in this paper. Generally static leakage power consists of gate oxide leakage and sub-threshold leakage [2]. Currently sub-threshold leakage seems to be the main contribution factor as compare to all type of leakage power [8]. We propose a new approach, thus providing a new choice to implement low-power VLSI circuit design. This power consumption techniques in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power dissipation. We have also presented additional information to help explain the causes of power consumption, and proposed possible solutions to minimize power dissipation in a CMOS devices.

II. THE HISTORY AND TREND OF POWER DISSIPATION OF DIFFERENT COMPONENT OF CMOS

For several decades Moore's law has served as a beacon to predict device density and its subsequent power dissipation. The Moore law, states that semiconductor transistor density, and hence performance, almost doubles every 18 months. Dr. Moore made his prediction in the 1970′s and history supports his conclusion, the chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades, as shown in Figure 1 [2]. While the 1 billion transistor integration mark was achieved some years ago, we now frequently see processors having more than 2B transistors on a die. In newer technologies, power is a primary design constraint. Power dissipation has skyrocketed due to transistor scaling, chip transistor counts and clock frequencies.
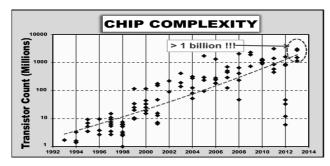

Fig.1: The chip complexity chart below shows the trend in transistor integration on a chip over the past two decades.

Leveraging sophisticated strategies to lower leakage and manage voltage and variability have bolstered the continuing in total power consumtion. This is helping rein in energy consumtions from PCs, servers, and similar devices and systems. As power reduction becomes mandatory in each application of any appliances, the trend for adjusting near-constant clock frequencies also continues as shown below in frequency trend plot. This will yield solutions with less cost and cooling demands, resulting in greener products in future.
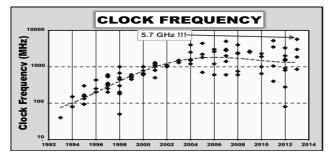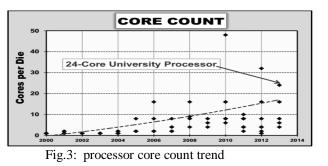

Fig.2 : Clock Frequency Trend

Processors are choosing to trade off performance by reducing supply voltage. The performance loss due to voltage and clock frequency reduction is compensated by further increased parallelism in processes. Today , devices are using more than 8 cores processors in the system and significant core count trend chart with respect to years as been shown below

Fig.3: processor core count trend

In addition to the trend to integrate more cores on a single chip. Similarly multiple die within a single package are appearing. In ISSCC 2013, IBM have presented aprocessor which have a multi-chip module , six CPUs and two embedded DRAM cache chips. In addition , dedicated co-processing units for graphics and communications are now commonly integrated on these complex systems-on-chip designing. Design of these SoCs requires wide range of collaboration with many disciplines including electronic circuits design, architecture structure, graphics for display, technology, packaging, design, energy efficiency and software implementation[5]. The chart below shows the general trend of large cache integration.
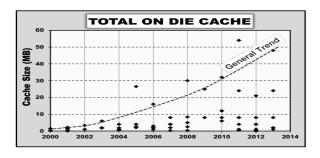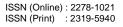

Fig.4: Die Cache Capacity Trend

In the sixties, the power consumption/dissipation of early electronics circuits wer high. Since there was no obvious spatial constraint, maintaining large cooling rooms were the norm. Nevertheless, the boundation in both processing speed and size advances in electronics circuit design and materials that reduced power dramatically and as a result required low cooling system technology. Only a few exotic or high-speed computers required either air conditioning or forced convection cooling by air. This trend continued to dominate for many years and created a false sense of security that the issue related with heat dissipation may have been control. This was further amplified significantly by the new introduction of CMOS technology that continues to replace Bipolar technology [7]. As shown, CMOS and Bipolar technologies have paralleled each other with a 10 year time shift.
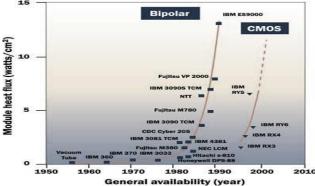
Fig.5: Power dissipation trends, comparison of Bipolar
and CMOS technologies.

III.   MECHANISMS OF POWER DISSIPATION

Mechanisms of power dissipation are usually divided into two classes: dynamic and static power dissipation. Dynamic dissipation of power mainly occurs operational mode of circuit, for example, the circuit is performing some other operation on data. Static power dissipation becomes an issue when the circuit is inactive or in a power-down mode.

A. Dynamic Power Dissipation: Dynamic power dissipation can be further subdivided into three major categories: switched power dissipation, short-circuitdissipation, and glitch power dissipation. All of them more or less depend on the aoerational ctivity, signal timing, load capacitance , and supply voltage of the electronic circuit. The continuous charging and discharging of the load capacitance is necessary to transmit information in CMOS circuits. This charging and discharging causes for the switched power dissipation. The power consumption of a CMOS digital circuit can be represented as

Dynamic Power Dissipation Calculation in CMOS:

$$\text{Pout} = P(t)dt = V_{dd}\int_0^T I(t)dt = V_{dd}\int_0^{V_{dd}} C_L\, dV_{out}$$

$$= C_L V_{dd}^2$$

As we observe from the equation, energy doesn't depend on frequency

Energy loss for Nc clock cycles:

$P(N_c) = C_L V_{dd}^2\, n(N_c)$ **, where** (N_c) **: is the number** $0 \rightarrow 1$ **transitions in** N_c **clock cycle**

$$P_{avg} = \lim_{N\to\infty}\left[\frac{P\,N_c}{N_c}\right]f = \left[\lim_{N\to\infty}\frac{n(N_c)}{N_c}\right]C_L V_{dd}^2\, f$$

Note: Power depends on frequency
$P_{Total} = C_L V_{dd}^2\, f + f\, I_{short}\, V_{dd} + I_{leak}\, V_{dd}$

Where f is the clock frequency , C is the average switched Capacitance per clock cycle, Vdd is the supply voltage , I is the short circuit current and I leak is the leakage power dissipation current. Using a lower Vdd is an effective way

to reduce the dynamic power consumption since Ist term is proportional to the square of Vdd.It should also be noted that the short circuit and leakage power dissipation are also strongly dependent on threshold voltage(Vdd). However, lower Vdd can degrades efficiency as well as overall performance of circuits.

Power = Energy/transition * transition rate
$= CL * V_{dd}^2 * f_{0\to 1}$ $= CL * V_{dd}^2 * P_{0\to 1}$ $= CEFF * V_{dd}^2$
 Ceff = Effective Capacitance = CL * $P_{0\to 1}$

Power Dissipation is Function of Data Dependent and Switching Activity:

Example: Static 2 Input NOR Gate

Table1: Power Dissipation is Function of Data Dependent and Switching Activity

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume: P (A=1) = ½ , P (B=1) = ½   Then: P (Out=1) = 1/5
 P (0→1) = P (Out=0) * P (Out=1) = 4/5 * 1/5 = 4/25
Ceff = 4/25 * CL
3.2.2 Short-Circuit Power Dissipation
 In real circuits signals have non-zero rise and fall times which causes both the P net and N net of the CMOS gate to conduct current simultaneously. This leads to the flow of a short- circuit current for a short period of time. The input and output slopes of a gate should be equal to minimize the overall short circuit dissipation in gates [John Rabaey (2003)][12]. Also large load capacitance can significantly reduce the short-circuit dissipation of the driving gate

1)   Glitch Power Dissipation

Glitches are undesired signal transitions which do not contribute any valuabe information. Still they are associated ith switched dissipation power and short-circuit power dissipation. Glitches can be divided into two categories: generated and propagated. If the input signals to a gate are distorted in time, there is absolute signal of present danger in agenerated glitch at the output. If a glitch approaces at the input of a gate and if the input is sensitive at the moment, a propagated glitch will be created[11] .The number of glitches present in a circuit, which consisting many gates, depends on the depth of logic, the logic function and the gate fan outs. In some circuits, the major part of the dynamic power dissipation is due to presence of glitches in the electronic circuit. In certain situation glitches have peak voltages that are in the center of the transition interval, their contribution to the short circuit power can be non-negligible [John Rabaey (2003)]. However, the glitch can be minimized by scale down the

supply and threshold voltages probably at different phases of the circuit. The rates of voltage scaling depend on type of process like it is low standby, low power, or high performance[10](Ayman A et al (2001)) .The glitch behavior under these circumstances has been studied where two voltage-scaling techniques have been used. One technique where the threshold voltage is kept constant when the supply voltage is lowered and the second technique where the threshold voltage is scaled at the same rate as the supply voltage.

B. Static Power Dissipation

The static power components become important when the circuits are at rest, i.e. when there is no activity in the circuits and they are all biased to a specific state of circuit. The static power dissipation mainly includes sub threshold and reversed- biased diode leakage currents. Due to the necessary but harmful (in a leakage- power sense) down – scaling of threshold voltages, the sub threshold leakage is becoming more and more pronounced. Below the threshold voltage, in weak inversion, the transistors are not completely off. The sub threshold current has a strong dependence on the threshold voltage. Sub threshold Current: Sub-threshold current that arises from the inversion charges that exists at the gate voltages below the threshold voltage. Tunneling Current: There is a finite probability for carrier being passed through the gate oxide which results in tunneling current thorough the gate oxide.Reverse-biased Diode Leakage: Reverse bias current in the parasitic diodes.

1) Leakage Power

Leakage power as a fraction of the total power increases when clock clock frequency falls. For a gate it is a small fraction of the total power; it can be significant for very large circuits. Scaling down features requires lowering the threshold voltage, which also increases leakage power; almost doubles with each shrinking[12]. Multiple-threshold devices are used to reduce leakage power. There are different types of power leakage shown below due to loss of current:
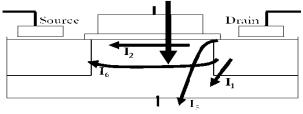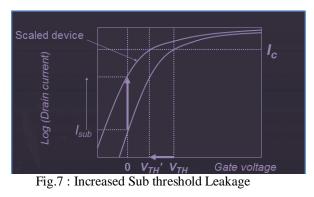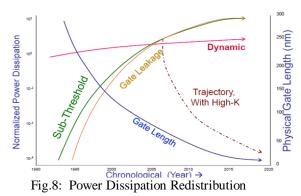

Fig.6: Leakage Power Component

2) Static Power leakages Leakages in CMOS

I1: reverse bias PN junction (both ON & OFF), I2: sub threshold leakage (OFF) ,I3: Gate Leakage current (both ON & OFF), I4: gate current due to hot carrier injection (both ON & OFF), I5: gate induced drain leakage (OFF) And I6: channel punch through current (OFF)

Fig.7 : Increased Sub threshold Leakage

Fig.8: Power Dissipation Redistribution

Sub threshold Current

$$I_{sub} = \mu_0 \, C_{ox} \, (W/L) \, V_t^2 \, exp\{(V_{GS} - V_{TH}) / nV_t\}$$

μ_0: *carrier surface mobility*, C_{ox}: *gate oxide capacitance per unit area* ,*L: channel length*
W: gate width, $V_t = kT/q$: *thermal voltage* and *n: a technology parameter*

3) Junction Leakage

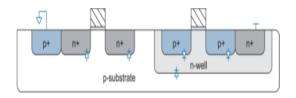The PN junctions between diffusion, substrate and well are all junction diodes.These are revered biased as substrate is connected to GND and well connected to Vdd. However, reversed biased diode also conduct small amount of current.

Fig.9: Junction Leakage due to Reverse Biasing

Junction Leakage

The reverse-biased junction current is expressed as follows:

$$ID = IS [\, exp \, (VD/vT) - 1 \,]$$

Where, IS depends on the doping level, the area, and perimeter of the diffusion region and VD is the diode voltage

4) Tunneling

There is a finite probability for carrier being passed through the gate oxide of CMOS. This results in tunneling

current thorough the gate oxide. The effect is predominating for lower oxide thickness. • The gate oxide leakage current can be expressed as follows:

I gate=K W gate (Vdd /Tgate)2 exp (– α Tgate/Vdd)
(K and α are experimentally derived factors).
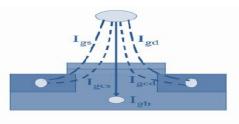

Fig.10: Static Power loss in CMOS Tunneling

IV.   POWER REDUCTION TECHNIQUES FOR VARIOUS POWER DISSIPATING COMPONENTS
.
In the beginning of the last decade, battery-powered hand-held devices such as mobile phones and laptop computers emerged. This called for low-power operation and a lot of design methods on different hierarchy levels were summarized by Chandrakasan et al. (Chandrakasan.C (1992)).

A.   Voltage Scaling and Reduced Voltage Swing

Reducing the supply voltage is an attractive solution to reduce the power dissipation since both the switched and the short-circuit power dissipation have a strong dependencyon threshold voltage(Vdd). A delay signal can be mitigated by lowering the threshold voltage but then the sub threshold leakage will increase exponentially. Hence it is important to select appropriate threshold and supply voltages. Another way of sustaining the throughput is to do an architectural voltage scaling. Then the throughput is kept by either parallelization (Ayman A et al (2001)) or pipelining (Pucknell (2004)).Both techniques introduce some overhead switched capacitance due to the extra hardware added but this is power-wise compensated for by the lower supply voltage. To reduce the active (dynamic) power, Vdd and Vth (Tezaswi Rajaetal (2004)),(Uming Ko et al (1995)) hopping schemes have been proposed.

B.   Clock Frequency Reduction

Reducing the clock frequency is not as beneficial as reducing the supply voltage. However, many processors in now a day have different power-down modes where the clock signal is inactive to block of the application that are unused at the that moment. This pocess is known as clock gating which can be used in most cases as conjunction with other low-power techniques.

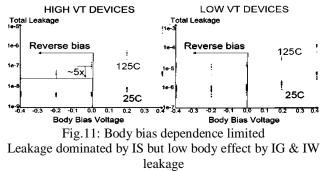*C. Switched capacitance reduction*

Reducing the switched capacitance is similar power efficient as reducing the clock frequency of circuit. Many advanced techniques have been proposed to reduce the switched capacitance. The selection of logic style can

significantly affect the critical capacitances. Whenever a low-power solution is searched for, conventional static CMOS is often a safe and effeicient and Multiplexers and XOR gates are an exception since they can be implemented in pass-transistor logic styles using fewer transistors. In flip-flops and registers, the capacitance of the clock nodes is important since the clock signal has a high activity. So, he flip-flops with a small number of clocked transistors have been proposed[8] (Weste.N and Eshraghian.K (1993)).

Table .2: Saved   Energy Comparision by Varying both Vdd and f

Voltage (V_{dd})	Frequency (f)	Power (P_d)	Energy (E_d)
V_{dd}	f_{max}	P_d	E_d
$V_{dd} / 2$	f_{max} *	$P_d / 4$	$E_d / 4$
$V_{dd} / 2$	$f_{max} / 2$	$P_d / 8$	$E_d / 4$
V_{dd}	$f_{max} / 2$	$P_d / 2$	E_d

D. Methods to Modulate IS Leakages
We can reduce the reverse IS leakage by variang the vias volatage both for both low and high VT devices shown in the figure below:

Fig.11: Body bias dependence limited
Leakage dominated by IS but low body effect by IG & IW leakage

E. IG: Methods to Reduce Gate Leakage: Using Nitrogen N and High-K
IG depends on both gate dieelectric material concentration and temperature. We can limit the IG current leakage by selecting the appropriate material. The leakage current variation with temperature and dielectric strength is given below in the diagram
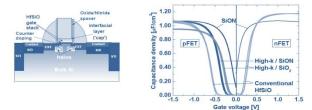

Fig.12: Optimized high-k dielectric stack reduces pFET Vt shift by 200~300 mV and selective use of ultra-thin interface/surface   modification   layers   and   Increased Nitrogen concentration decreases gate leakage current
F. Methods to Reduce Junction Leakages

Leakage modulated primarily by transistor doping profiles and Band to band tunneling increases with doping levels &

steeper gradients. Gate field enhanced tunneling increases with thinner gate dielectric.
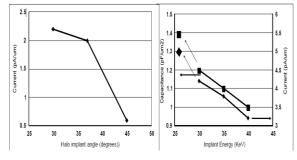

Fig.13: Graph between NFET Junction Leakage current , Halo Angle PFET Junction Leakage and S/D Energy

G. Power reduction in Switching Power Components

Reduction of area diffusion capacitance, reduction of perimeter capacitance with film scaling and additional AC drive current benefit from gate coupling are useful for controlling the power loss due to switching. There are various options to Gate Capacitance Scaling: Need better electrostatic control to scale LG, Higher gate inversion capacitance, High-K gate dielectric material to reduce EOT , Metal gate material to eliminate gate depletion, Fully depleted double gate structures and Better channel control through structural change
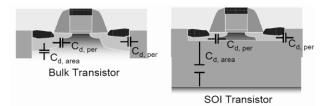

Fig.14: Capacitance Reduction

Capacitance Scaling with Metal Gate: LG must decrease to prevent capacitance increase. Short channel effect degradation when metal gate work function deviates too far from band edge and lose portion of performance benefit and most of power benefit.
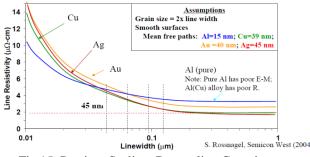

Fig.15: Passives Scaling: Decoupling Capacitors

V.   VLSI CIRCUIT DESIGN TECHNIQUES FOR LOW POWER

A.   Adiabatic Circuits

In adiabatic circuits power is reused instead of dissipating . It can be done by externally controlling the length and shape of signal transitions energy spent to flip a bit can be

reduced to very small values. Diodes are are not used in the design of Adiabatic Logic because of thermodynamically irreversible nature. MOSFETs should not be turned ON when there is notable potential difference between source and drain voltage of CMOS. And similarily should not be turnoff when there is a significant current flowing through the device. In the adiabatic circuit shown above initially, f and /f at Vdd/2, P at Gnd, and /P at Vdd. On valid input, the pass gate is turned on by gradually swinging P and /P. Rails f and /f "split", gradually swinging to threshold voltage (Vdd) and Gnd. Pass gate is turned off as soon as output is sampled,. Internal node is restored by gradually swinging f and Vdd/2.Once the electronic device is turned on energy transfer takes place in a controlled manner so that there is no potential drop across the device.
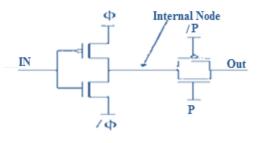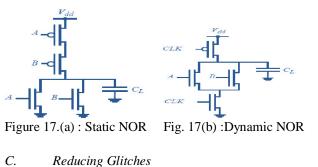

Fig.16: Charge Recovery Logic

B.   Logic Design for Low Power

Choices between static versus dynamic CMOS, traditional CMOS versus pass-transistor logic styles and synchronous versus asynchronous timing styles have to be made during the design. In cae of static CMOS circuits, the power dissipation component due to short circuit current is about the 10% of the total power consumption. On the other hand, in case of dynamic circuits we don't face this kind of problem, since there is no direct dc path from supply voltage to ground(Gnd). Only in cae of domino-logic circuits design there is such a path, in order to overcome sharing, so,there is short-circuit power dissipation.

Figure 17.(a) : Static NOR   Fig. 17(b) :Dynamic NOR

C.   Reducing Glitches

Glitches occur in a logic chain when two parallel driving common gate arrive at different times. In this situation, the output instantly switches to incorrect value before settling to correct result value. Consider the circuit shown below in the diagram. Let us assume that in the absence of buffer path A is high speed and Path B is slow. Initially if A=0 and B=1 then Z=0.Next if B is to switch to 0 and A to 1 since B is slow as comparision to A, then the data 0

arriving at B will be slow and hence Z switches towards 1 instantly before switching back to zero which is resulting in power dissipation.
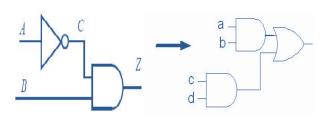

Fig.18: Glitch Free AND Gate as shown in figure above buffers are generally used to delay path A to overcome glitches

D. Logic Level Power Optimization

During logic optimization for low power,we fix the value of technology parameters such as supply voltage , and we are free are for selecting the functionality and sizing the gates. Path equalization by using buffer insertion is one of the prominent techniques which ensures that signal propagation pathbetween inputs to outputs of a logic gate is similar in length to overcome glitches. (which is created by misaligned input transitions) (T. Burdet et.al, , Journal of VLSI Signal Processing Systems, vol.13, no. 2-3, pp. 203-221, August 1996)
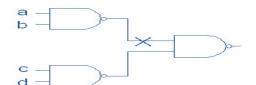

Fig.19: Logic Remapping for Low Power

Other power minimization techniques include local transformations as described in abov figure which is a re-mapping transformation , where a high-activity node (marked with x) is removed and replaced by new mapping onto an and or gate.

E. Standby Mode Leakage Suppression

Static/Leakage power, originates from substrate currents and subthreshold leakages. For technologies 1 μm and above , PSwitching was predominant. However for deep-submicron processes below 180nm, Leakage becomes prominent factor which is also a major concern in recent technologies, as it impacts battery lifetime. When transistors are not switching or in stand-by mode, CMOS technology has been extremely power-efficient, and system designers controls leakage power from CMOS chips. Multiple-threshold and variable threshold circuit techniques are often used to meet leakage power constraints,. In multiple-threshold CMOS, the process provides two different threshold transitors. In case of Speed-critical sub-circuits, low-threshold are employed and they are fast and leaky where as High-threshold transistors are slower but exhibit low sub-threshold

leakage. They are also employed in noncritical or slow paths of the chip. Multiple-threshold techniques tend to lose effectiveness as more transistors become timing-critical.

F. Variable Body Biasing

Variable-threshold circuits dynamically control the threshold voltage of transistors through substrate biasing and hence overcome shortcoming associated with multi-threshold design of circuit. This technique is used when a variable-threshold circuit is in standby, NMOS transistor's substrate is negatively biased, and their threshold rises mainly because of the biasing effect of body. Similarly the substrate of PMOS transistors is biased by positive body bias to rises their threshold(Vth) in stand-by. Although Variable-threshold circuits can overcome associated quiescent/static leakage, but they require control circuits which modulate substrate voltage in stand-by mode. In this case, when the circuit is in standby mode the body of both PMOS and NMOS are biased by third supply voltage to increase the threshold(Vth) of the MOSFET as shown in the Figure. However, during normal mode they are switched back to decrease the threshold(Vth).
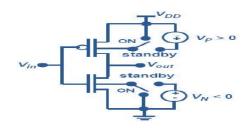

Fig.20: Variable Body Biasing

G. Sleep Transistors

Sleep Transistors are High Vt transistors connected in series with low Vt logic as shown below .When the main circuit consisting of Low Vt devices are ON the sleep transistors are also ON resulting in normal operation of the circuit. Since High threshold (Vt)is connected in series with Low threshold (Vt) circuit the leakage current power loss is measured by High threshold (Vt) devices and is quiet low[15]. Therefore,the resultant static power dissipation is reduced.

Fig.21: Circuit Design with Sleep Transistors

H. *Dynamic Threshold MOS*

In dynamic threshold CMOS (DTMOS), the threshold voltage(Vt) is altered dynamically to suit the operating state of the circuit. A low threshold voltage allows for higher current drives in the active mode of operation, while high threshold voltage in the standby mode gives low leakage current. Dynamic threshold CMOS can be achieved by controlling the both gate and body. The supply voltage of DTMOS is limited by the diode built-in potential in body silicon technology and the pn diode between source and body should be in reverse biased state. So, this technique is only beneficial for ultralow voltage (0.6V and below) circuits in CMOS.
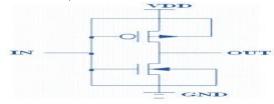

Fig.22: DTMOS Circuit

I. *Short Circuit Power Suppression*

When pairs of PMOS and NMOS transistors are conducting simultaneously,it causes the short circuit currents that arise Short Circuit Power. In static CMOS circuits, short-circuit path exists for direct current flow from VDD to ground, when **VTn< Vin< VDD-|VTp|**
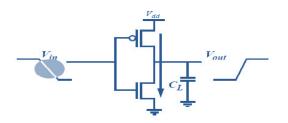

Fig.23: Short Circuit Power in CMOS Circuits

One way to reduce short circuit power is to keep the input and output rise/fall times the same. If **Vdd < Vtn + |Vtp|** then short-circuit power can be eleminated. when the load capacitance is very large, the output fall time is larger in comparison input rise time and the drain-source voltage of the PMOS transistor is zero.So, the short-circuit power will be zero. Whereas, if the load capacitance is very small, and the output fall time is smaller than the input rise time. Then, the drain-source voltage of the PMOS transistor is close to VDD during most of the transition period which will be resulting very large the short-circuit power.

VI.   A LOOK AT THE FUTURE

Based on what we know to date, making some projections for the next 5 to 10 years is fairly straightforward. If there are no step changes in crcuit technology implementation then, it is apparent that power dissipation will be a major bottleneck across the industry. For the coming future, all data presented here and elsewhere points to die level heat fluxes of 40 - 50 W/cm^2 as the norm, not the exception. Barring specialized electronics that may exceed these levels (ultra-speed computers and space/military applications), this implies circuit power dissipation of several hundred watts and systems of several kilowatts. Further, there are no clear sign of that speed is decreasing or that the industry is stepping away from the system-on-chip design concept. The combination of speed, compactness and system features will push power dissipation and its management to the limit.

VII.   CONCLUSION

Power consumption is associated with load capacitance, frequency of operation, supply voltage input voltage level, input rise time, source leakage current, Gate current, Switching power, short-circuit power, power-dissipation capacitance, and output loading affect. A reduction of any one of these is beneficial for us and power consumption provides many benefits such as less heat is generated, which overcome many   problems associated with high temperature, such as the need for heat sinks. This provides low cost product to the consumer . Therefore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

REFERENCES

[1]. Chu, R.C., Simons, R.E., and Chrysler, G.M., "Experimental Investigation of an Enhanced Thermo syphon Heat Loop for Cooling of a High Performance Electronics Module," Proceedings of the 15th IEEE Semiconductor Thermal Measurement and Management Symposium," pp.1-9, 1999.

[2] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal ofSolis-State Circuits, Vol. 30, No. 8, pp. 847-854, 1995.

[3]. Colwell, R. "CPU Power Challenges 1999″, ISPLED '99
[4]. Lucent Technology Microelectronics Data Book
[5]. Ruby, W. M. "Managing Power Dissipation in System-on-a-Chip Designs" Web publication.
[6]. Frenkil, G. "Controlling Power Dissipation in Submicron IC's," Web publication.
[7] S.Samanta" Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool" Special issue of International Journal of computer communication Technology.vol 2.isuue 2,3,4.pp300-303. 2010.

[8] Takada, M. Nakamura, K.; Yamazaki, T. 1995 High speed submicron BiCMOS memory. IEEE Trans. Elect. Dev. 42 (1995) 497-504.

[9] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low power CMOS digital design,'' IEEE J. Solid-State Circ., vol. 27, no. 4, pp.473-484, Apr. 1992.

[10] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005.

[11] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization andSimulation, pp. 148-158, 2004.

[12] International Technology Roadmap for Semiconductors by Semiconductor IndustryAssociation, 2002. [Online]. Available http://public.itrs.net

[13] Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling

of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, August 1998.

[14] Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, 1998.

[15] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization andSimulation, pp. 148-158, 2004.

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