

# CONDITIONAL CLOCKING FLIP-FLOP FOR LOW POWER HIGH-SPEED MOBILE APPLICATION SOC

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**Abstract:** An extremely low-power flip-flop named topologically-compressed flip-flop is planned. As compared with standard FFs, the FF reduces power dissipation by seventy fifth at 1/3 information activity. This power reduction magnitude relation is that the highest among FFs that are reported thus far. The reduction is achieved by applying topological compression methodology, merger of logically equivalent transistors to associate unconventional latch structure. The terribly little variety of transistors, only three, connected to clock signal reduces the facility drastically, and therefore the smaller total transistor count assures identical cell space as standard FFs. In addition, absolutely static full-swing operation makes the cell tolerant of provide voltage and input slew variation. associate experimental chip design with forty nm CMOS technology shows that nearly all standard FFs are replaceable with planned FF whereas protective the same system performance and layout space.

**Keywords:** Flip-flops, low-power, VLSI

## I INTRODUCTION

THE mobile market keeps on increasing. Additionally to the standard mobile, camera, and pill computer, development of varied types of wearable info equipment or attention associated instrumentality has recently prospered in recent years. In those types of battery-working instrumentality, reduction of power may be an important issue, and demand for power reduction in LSI is increasing. Supported such background, varied types of circuit technique have already been planned. In LSI, typically quite 1/2 the facility is dissipated in random logic, of that 1/2 the facility is dissipated by flip-flops (FFs). Throughout the past dozen years, many low-power FFs are rush into development. However, in actual chip style, the standard FF remains used most frequently as a most well-liked FF as a result of its well-balanced power, performance and cell space. The aim of this paper is to gift an answer to attain all of the goals: power reduction with none degradation of temporal order performance and cell space.

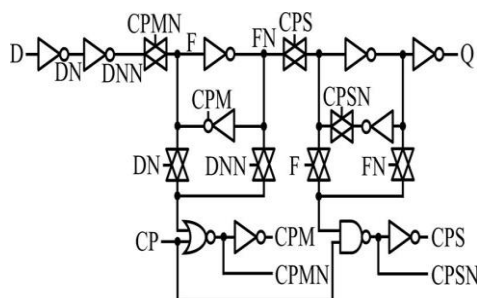


Fig 1 Conventional sense-amplifier flip-flop

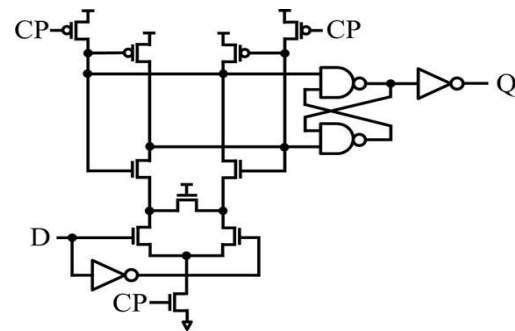


Fig 2 Differential sense-amplifier flip-flop (DiffFF)

## II RELATED WORK

In this section, we tend to analyze issues on antecedently reported typical low-power FFs with comparison to a traditional FF shown in Fig. 1. A pair of shows a typical circuit of differential sense-amplifier type FF (Diff FF) [1]–[3]. This kind of circuit is extremely effective to amplify small-swing signals, therefore is usually utilized in output of memory circuits. In this FF, however, the result of power reduction goes down within the condition of lower information activity, because these varieties of circuits have pre-charge operation in each clock-low state. Moreover, if we tend to use reduced clock swing, a customized clock generator and an additional bias circuit are necessary. Fig. shows a circuit of conditional-clocking kind FF (CCFF) [4]–[6].

This circuit is achieved from a useful purpose of read. The circuit monitors input file amendment in each clock cycle and disables the operation of internal clock if input file aren't modified.

By this operation, power is reduced once input

file aren't modified. However sadly, its cell space becomes virtually double that of the standard circuit shown in Fig.

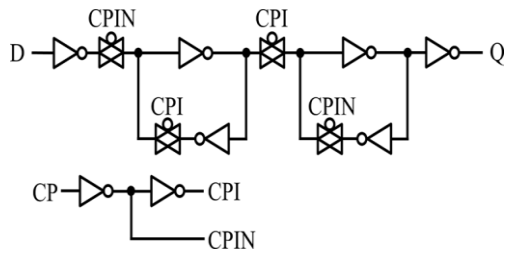


Fig. 3. Conditional-clocking flip-flop (CCFF).

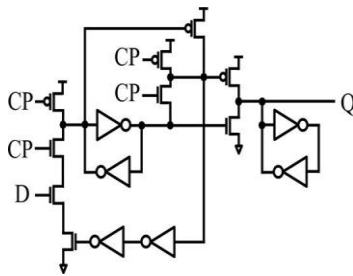


Fig. 4. Cross-charge control flip-flop (XCFF).

Chiefly attributable to this size issue, it becomes arduous to use if the logic space is comparatively giant within the chip. Fig. four shows the circuit of cross-charge management FF (XCFF) [7]. The feature of this circuit is to drive output transistors separately so as to scale back charged and discharged gate capacitance. As a result, the impact of power reduction can decrease. Circuits as well as preset operation have an equivalent drawback [8]. The adaptive-coupling sort FF (ACFF) [9], shown in Fig 4, is predicated on a 6-transistor memory cell. During this circuit, rather than the unremarkably used double-channel transmission-gate, a single-channel transmission-gate with further dynamic circuit has been used for the information line so as to scale back clock-related transistor count.

However, during this circuit, delay is well full of input clock slew variation as a result of differing kinds of single-channel transmission-gates area unit employed in an equivalent information line and connected to an equivalent clock signal.

Moreover, characteristics of monaural transmission-gate circuits and dynamic circuit's area unit powerfully full of method variation. Thus, their optimization is comparatively tough, and performance degradation across varied method corners may be a concern. Let us summarize the analysis on antecedently rumored low-power FFs. For Diff FF [1] and XCFF [7], pre-charge operation may be a concern particularly in lower information activity. As regards CCFF [4], its cell space becomes a bottleneck to use.

### III PROPOSED DESIGN APPROACH

In order to cut back the facility of the FF whereas keeping competitive performance and similar cell space, we have a tendency to tried to cut back the semiconductor unit count, particularly those operational with clock signals, while not introducing any dynamic or pre-charge circuit. The facility of the FF is usually dissipated within the operation of clock-related transistors, and reduction of semiconductor unit count is effective to avoid cell space increase and to cut back load capacitance in internal nodes. One reason is as a result of transmission-gates would like a 2-phase clock signal, so the clock driver can't be eliminated. Another excuse is that transmission-gates ought to be created by each PMOS and NMOS to avoid degradation of information transfer characteristics caused by mono MOS usage. Therefore, rather than transmission-gate sort circuit, we have a tendency to begin with a combinable sort circuit as shown in Fig. 3. to cut back the transistor-count supported logical equivalence, we have a tendency to take into account a technique consisting of the subsequent 2 steps. Because the beginning, we have a tendency to attempt to have a circuit with 2 or additional logically equivalent AND or OR logic components that have identical signaling combination, particularly as well as clock signal because the input signals. Then, merge those components in semiconductor unit level because the second step.

### IV. PROPOSED DESIGN STRUCTURE FOR COMPRESSED FLIP-FLOP

After work several varieties of latch circuits, we've got created associate degree unconventionally structured FF, shown in Fig. 7. This FF consists of various kinds of latches within the master and also the slave components. The slave-latch could be a well-known Reset-Set (RS) sort, how ever the master-latch is associate degree asymmetrical single data-input sort. The feature of this circuit is that it operates single section clock, and its 2 sets of logically equivalent input AND logic, X1 and Y1, and X2 and Y2. Fig. shows the transistor-level schematic of Fig.7

Supported this schematic, logically equivalent transistors area unit united as follows. For the PMOS aspect, 2 semiconductor unit pairs in M1 and S1 blocks in Fig. eight may be shared as shown in Fig. 7. Once either N3 or CP is Low, the shared common node becomes VDD voltage level, and N2 and N5 nodes area unit controlled by PMOS transistors gated N1 and N4 separately once each N3 and CP area unit High, each N2 and N5 nodes area unit force all the way down to VSS by NMOS transistors gated N3 and CP. still as M1 and S1 blocks, 2 PMOS semiconductor unit pairs in M2 and S2 blocks area unit shared. For the NMOS aspect, transistors of logically equivalent operation may be shared still. 2 transistors in M1 and M2 blocks in Fig. ten may be shared. Transistors in S1 and S2 area unit shared still.

Further within the PMOS aspect, CP-input transistors in S1 and S2, may be united, as a result of N2 and N3 area unit logically inverted to every different. Once CP is Low, each nodes area unit in VDD voltage level, and either N2 or N3 is ON. Once CP is High, every node is in frealnce voltage level. In thought of this behavior, the CP-input transistors area unit shared and connected as shown in Fig. 8. The CP-input semiconductor unit is functioning as a switch to attach S1 and S2. This circuit consists of seven fewer transistors than the initial circuit shown in Fig. 8. The amount of clock-related transistors is simply 3. Note that there's no dynamic circuit or pre-charge circuit, thus, no further power dissipation emerges. We have a tendency to decision this re-duct ion technique Topological Compression (TC) technique. The FF, TC-Method applied, is named Topologically-Compressed Flip-Flop (TCFF).

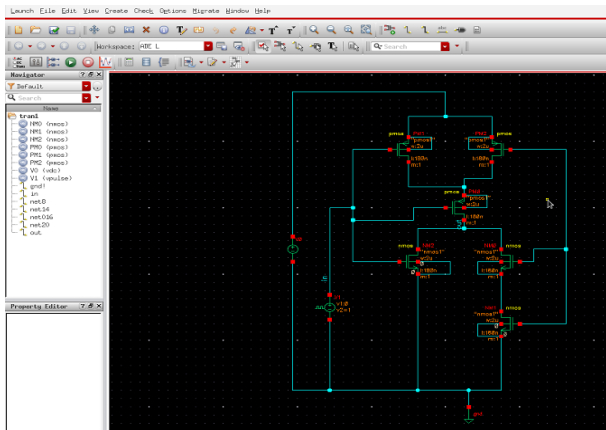


Fig5. Transistor merging in PMOS side

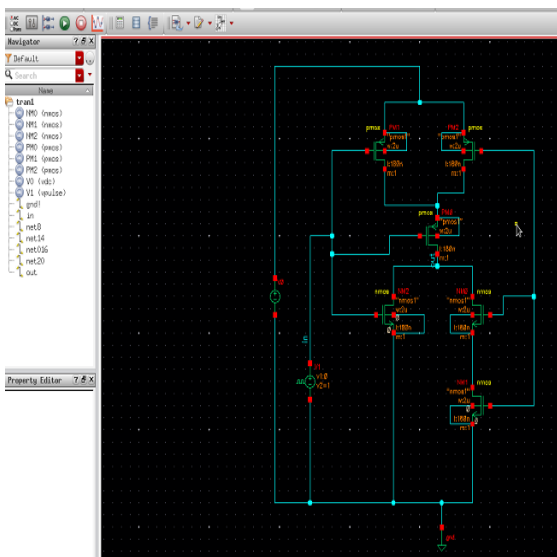


Fig6. Transistor merging in NMOS side

## V. PERFORMANCE SIMULATION

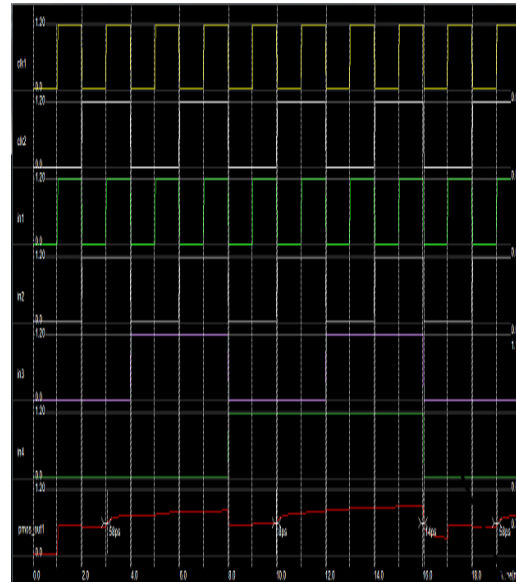


Fig 7 Transistor merging output waveform

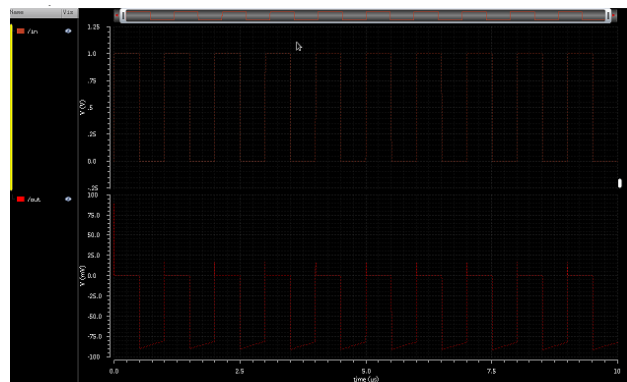


Fig 8 Transistor merging output waveform

The performance of TCFF is incontestable by SPICE simulation with forty nm CMOS technology. For comparison with different FFs, an equivalent semiconductor electronic transistor in each FF as well as TCFFso as to simulate an equivalent conditions. Some normal values area unit assumed for junction transistor sizes for the aim of comparison; zero.24 m for breadth and zero.04 m for length in PMOS, and 0.12 m for breadth and zero.04 m for length in NMOS. Fig. shows the normalized power dissipation versus knowledge activity compared to different FFs. TCFF consumes the smallest amount power among them in the majority ranges of knowledge activity. Average knowledge activity of FFs in associate degree LSI is often between five-hitter and V-day. The facility dissipation of TCFF is sixty six under that of TGFF at 100 percent knowledge activity. Within the same manner at 1/3 knowledge activity, its 85% lower. Table I summarizes the transistor-count, the CP-Q delay, the setup/hold time, and therefore the power magnitude relation of every FF. As for delay, TCFF is nearly an equivalent because the standard, and higher than different FFs.

Setup time is that the solely inferior parameter to the standard FF, and regarding seventy notation larger than the worth of the standard one. For hold time, TCFF is healthier than the standard FF. In summary, solely setup time is giant, however TCFF keeps competitive performance to the standard and different FFs. Fig. shows the supply-voltage dependence of the CP-Q delay. TCFF is feasible to work right down to zero.6 V offer voltage because of basically fully static operate. Though' TCFF operates with single section clock signal, a clock buffer isn't necessary. The circuit is directly driven from a clock pin. Fig. twenty shows the clock-input-slew dependence of the CP-Q delay ACFF. In order to use TCFF round the important condition, adjustment of semiconductor device size is taken into account. In TCFF, since data-input or data-output operation is controlled by 3 clock - related transistors, by ever-changing the scale of these transistors, performance is modified. Ever-changing solely 3 transistors in twenty one transistors of a TCFF circuit doesn't have an effect one cell space a lot of. Table IV shows performance of TGFF, TCFF, and also the resized TCFF. Within the resized TCFF, solely the 3 clock-related transistors square measure doubled in size. Fig. Shows the normalized power dissipation for TCFF and also the resized TCFF compared to TGFF. Compared to the first TCFF, delay and setup time is improved by five-hitter and twenty first, severally, within the resized TCFF. Power dissipation will increase thirty ninth, however continues to be fifty three under TGFF. Fig. twenty eight shows the results of replacement in 333 megacycles per second clock frequency as well as the resized TCFF additionally to TGFF and also the original TCFF. Total replacement rate is the maximum amount as ninety fifth, and half a mile is replaced by the first TCFF and seven is replaced by the resized TCFF. In summary, as well as a range of clock-related semiconductor device sizes, TCFF is applied to numerous speed systems, and it will cut back whole chip power additional effectively.

S.No	Conventional FF	TCFF	TGFF
Power in mW	183	148	129
Supply Voltage	0.9	0.9	0.9
Frequency in MHz	330	330	330
Propagation Delay in ns	203	186	178
Area (mm <sup>2</sup> )	0.0998	0.0094	0.067

Table 1. Comparison of various FF

### CONCLUSION

An extremely low-power FF, TCFF, is planned with topological compression style methodology. TCFF has very cheap power dissipation in most vary of the information activity compared with alternative low-power FFs. the facility dissipation of TCFF is 80 % not up to that of TGFF at third information activity while

not space overhead. The topology of TCFF is definitely expandable to varied sorts of FFs while not performance penalty. Applying to a 250 MHz experimental chip style with forty nm CMOS technology, ninety eight of standard FFs area unit replaced by TCFFs. in an exceedingly whole chip, 37% of power reduction is calculable with very little overhead of space and temporal arrangement performance.

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