

# Implementation of Area Optimized Advanced Encryption Standard

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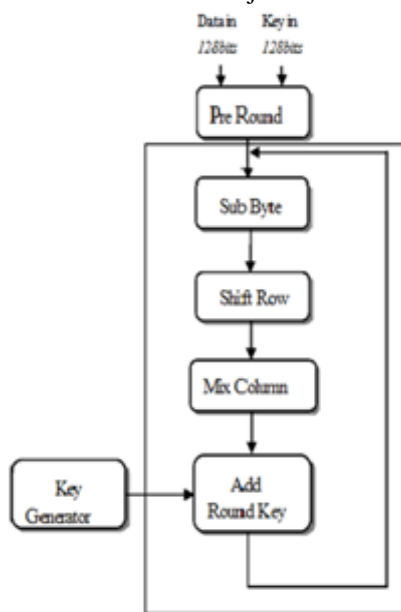
**Abstract:** Advanced Encryption Standard (AES) is the current standard for secret key encryption. AES was created by two Belgian cryptographers, Vincent Rijmen and Joan Daemen, to overcome the disadvantages of Data Encryption Standard (DES). The Federal Information Processing Standard 197 used a standardized version of the algorithm called Rijndael for the Advanced Encryption Standard. The algorithm uses a combination of Exclusive-OR operations (XOR), substitution with an S-box transformation, row and column rotations, and a MixColumns. All the transformations of encryption are simulated using an iterative design approach in order to minimize the hardware consumption. To reduce manual operations a verilog code is developed, synthesis and simulations of code is done by using Xilinx and Modelsim. It was successful because it was easy to implement and could run in a reasonable amount of time on a regular computer.

**Key Words:** EDK, REAL TIME COMMUNICATION, AGS, SECURITY, XPS, RTOS.

## I. INTRODUCTION

The Advanced Encryption Standard, in the following referenced as AES, is the winner of the contest, held in 1997 by the US Government, after the **Data Encryption Standard** was found too weak because of its small key size and the technological advancements in processor power. Fifteen candidates were accepted in 1998 and based on public comments the pool was reduced to five finalists in 1999. In October 2000, one of these five algorithms was selected as the forthcoming standard: a slightly modified version of the Rijndael

transformation requires a second input, which is the secret key. It is important to know that the secret key can be of any size (depending on the cipher used) and that AES uses three different key sizes: 128, 192 and 256 bits



The Rijndael, whose name is based on the names of its two Belgian inventors, **Joan Daemen** and **Vincent Rijmen**, is a **Block cipher**, which means that it works on fixed-length group of bits, which are called blocks. It takes an input block of a certain size, usually 128, and produces a corresponding output block of the same size. The

INPUT	CIPHER KEY
32	2B
43	7E
F6	15
A8	16
88	28
5A	AE
30	D2
8D	A6
31	AB
31	F7
98	15
A2	88
E0	09
37	CF
07	4F
34	3C



**KEY GENERATION:**

04	E0	48	28
66	CB	F8	06
81	19	D3	26
E5	9A	7A	4C

**KEY INPUT:**

2B	28	AB	09
7E	AC	F7	CF
15	D2	15	4F
16	AB	88	3C

**Steps:**

1. Take Last Column Of Key Input:  
09 CF 4F 3C
2. S-byte Transformation(Using 'S'Table)  
01 A 84 EB
3. Shift left to One Position  
8A 84 EB 01

ROUND	RCON VALUE
R0	01
R1	02
R2	04
R3	08
R4	10
R5	20
R6	40
R7	80
R8	1B
R9	36

4. Adding RCON Value To Step 3

$$\begin{matrix} [8A] & [84] & [EB] & [01] \\ \Rightarrow & [01] & [00] & [00] & [00] \end{matrix}$$

As total is 32 bits '01' is added to MSB and Remaining 0's

$$\begin{matrix} 8A \rightarrow 10001010 \\ 01 \rightarrow 00000000 \\ \hline 1000101 \\ \text{8 B} \end{matrix}$$

$$\begin{matrix} 5. \quad 8B \ 84 \ EB \ 01 \quad \oplus \text{columns} \\ \text{Each XOR with 4 columns} \\ 8b \ 84 \ eb \ 01 \\ 2b \ 7e \ 15 \ 16 \\ 8B \rightarrow 10001011 \quad 84 \rightarrow 10000100 \\ 2B \rightarrow 00101011 \quad 7e \rightarrow 01111110 \\ \hline \quad \quad \quad 1010 \ 0000 \quad \quad \quad 1111 \ 1110 \\ \quad \quad \quad \text{A} \quad 0 \quad \quad \quad \text{F} \quad \text{A} \\ EB \rightarrow 11101011 \\ 15 \rightarrow 00010101 \\ \hline \quad \quad \quad 1111 \ 1110 \\ \quad \quad \quad \text{F} \quad \text{E} \end{matrix}$$

**KEY EXPANDED OUTPUT:**

A0	88	23	29
FA	54	A3	6C
FE	2C	39	76
17	B1	39	05

04	E0	48	28
66	CB	F8	06
81	19	D3	26
E5	9A	7A	4C

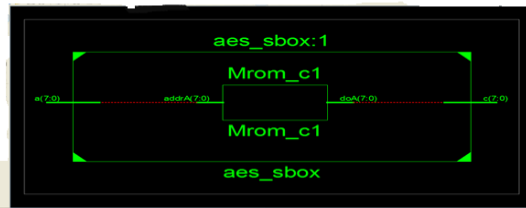
**ADD ROUND KEY OUTPUT:**

A4	68	6B	02
9C	9F	5B	6A
7F	35	EA	50
F2	2B	43	49

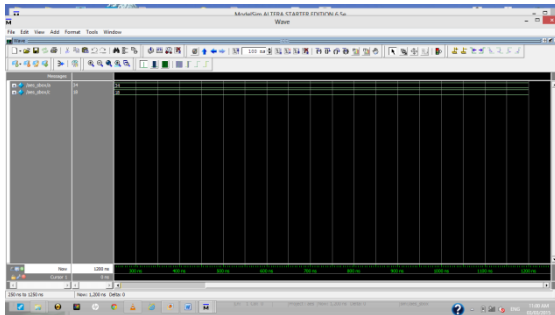


First Cipher Key Output

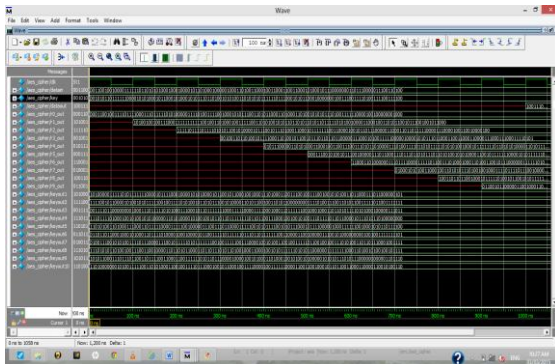
Implementing the algorithm manually is difficult. In order to reduce this, we are converting this algorithm into a verilog code and can be synthesised, simulated using XILINX and MODEL SIM tools.



S-BOX BLOCK DIAGRAM :  
S-BOX SIMULATION:



CIPHER SIMULATION:



### CONCLUSION

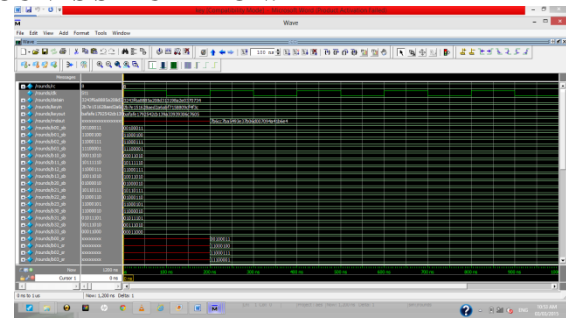
The Rijndael algorithm was chosen as the new Advanced Encryption Standard (AES) for several reasons. The purpose was to create an algorithm that was resistant against known attacks, simple, and quick to code. Choosing to use field GF(2)<sup>8</sup> was a very good decision. The block size and key size can vary making the algorithm versatile.

Optimized and Synthesizable VHDL code is developed for the implementation of encryption process. Each program is tested with some of the sample vectors provided by NIST and output results are perfect with minimal delay. Therefore, AES can indeed be implemented with reasonable efficiency on an FPGA, with the encryption taking an average of 320 ns (for every 128 bits).

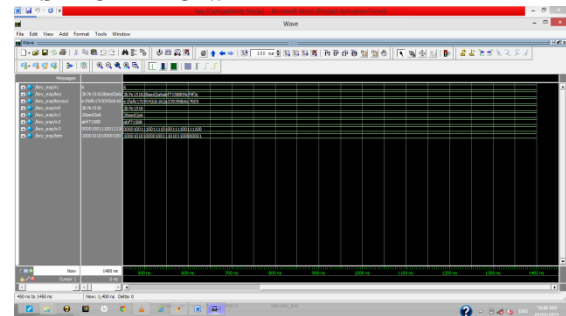
The time varies from chip to chip and the calculated delay time can only be regarded as approximate. Adding data pipelines and some parallel combinational logic in the key scheduler and round calculator can further optimize this design.

AES was originally designed for non-classified U.S. government information, but, due to

### ROUNDS SIMULATION:



### KEY SIMULATION:



its success, AES-256 is usable for top secret government information [11]. As of July 2009, no practical attacks have been successful on AES [12].

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