

An Optimized Design of Counter Using Reversible Logic

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Abstract: Reversible computing has been gaining a great deal of attention from researchers because of its low power consumption. A good amount of research work has been carried out in the area of reversible combinational logic as well as sequential design of reversible circuits. In this paper we proposed efficient designs for both the asynchronous and synchronous counter circuits that are optimized in terms of quantum cost, delay and the number of garbage outputs.

Keywords: Reversible Logic, Delay, Garbage Output, Flip-Flop, Quantum Cost.

I. INTRODUCTION

Energy dissipation in modern circuit design is rapidly becoming a primary design concern. According to Landauer's the amount of energy dissipated for every irreversible bit operation is $KT \ln 2$ joules of heat energy, where K is the Boltzmann's constant ($1.3807 \times 10^{-23} \text{JK}^{-1}$) and T is the operating temperature [1]. At room temperature (300 K), $KT \ln 2$ is approximately 2.9×10^{-21} J, which is small but not negligible in complete system. This heat dissipation dramatically reduces the performance and lifetime of the circuits. In 1973 C.H. Bennett showed that $KT \ln 2$ energy dissipation can be avoided, if a computation is carried out in a reversible way, since this energy dissipation occur when a bit of information is discarded during computation [2].

Researchers introduced several design of reversible sequential circuits and work is still going on. Researchers [12-16] proposed the implementation of all types of latches, flip-flops and their master-slave design. This paper proposes a novel concept on reversible asynchronous and synchronous counters using T flip-flop.

The rest of the paper is organized as follows: Section II provides some basic definitions related to reversible logic. Section III describes some basic reversible logic gates. Section IV presents the design of our proposed reversible synchronous and asynchronous counter using proposed T flip-flop and its comparison with the existing work. Finally Section V concludes the work.

II. BASIC DEFINITIONS

A. Reversible Gate

A reversible logic gate is an n -input n -output (denoted by $n \times n$) logic circuit in which there is a one-to-one correspondence between its inputs and outputs [3]. If the input vector I_v of the reversible gate is defined as $I_v = (I_1, I_2, \dots, I_{n-1}, I_n)$ and the output vector O_v defined as $O_v = (O_1, O_2, \dots, O_{n-1}, O_n)$, then according to the definition, $I_v \square \square O_v$, i.e., it can generate unique output vector from each input vector and vice versa.

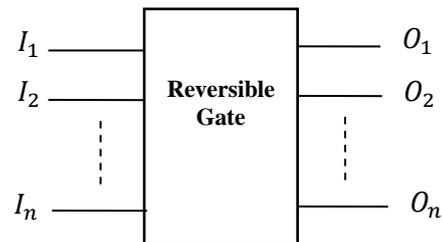


Fig.1. A $n \times n$ Reversible gate

B. Quantum Cost

Complex reversible gate are realized by using 1×1 NOT gate and 2×2 reversible gate and the quantum cost of these complex gate is calculated as the number of 1×1 and 2×2 reversible gate. Each 1×1 and 2×2 reversible gate is considered as unit for measuring overall quantum cost [4]. The quantum cost of Peres gate is 4 in Fig. 6.

C. Garbage Output

Garbage output is defined as the outputs that are not primary output or output that are not used as input to other gate. More formally, unwanted or unused or unutilized outputs which are needed only to maintain reversibility of a reversible gate (or circuit) is known as garbage output.

D. Delay

The path which consist maximum number of gates for any input to any output in the circuit is known as critical path. Delay of a reversible circuit is the delay of this critical path. We used Mohammadi and Eshghi [5] proposed logical depth for measuring delay. The delay of each 1×1 and 2×2 reversible gates is taken as unit delay, i.e. 1.

E. Constant Input

The input that is added to a function to make it reversible is called constant input. Input lines are either 0 or 1 should be as minimum as possible.

F. Gate Count

It refers to the total number of reversible gates used in the designed circuit. But gate count is not a good metric for

comparison since each reversible gate is of different computational complexity, and thus will have a different quantum cost and delay [6].

In this paper quantum cost, delay and the number of garbage outputs are used as the cost metrics while comparing the proposed design with the existing designs.

III. BASIC REVERSIBLE LOGIC GATES

A. NOT Gate

1*1 NOT gate is the simplest among all the reversible gates where the gate has only one input (A) and one output (P) such that $P = \bar{A}$. NOT gate is used as an inverter to invert the applied input. The quantum cost of this gate is 1. The NOT gate is shown in Fig. 2.



Fig.2. 1*1 NOT gate

B. Feynman Gate

Feynman gate (FG) is the only 2-input 2-output (2*2) reversible gate. It is also known as Controlled-NOT (C-NOT) gate. The input vector $I_v = (A, B)$ and output vector $O_v = (P = A, Q = A \oplus B)$. The quantum cost of Feynman gate is 1 [7]. The Feynman gate is shown in Fig. 3.

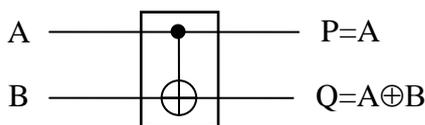


Fig.3. 2*2 Feynman gate

C. Double Feynman Gate

The input vector I_v and output vector O_v of 3*3 Double Feynman gate (DFG) is defined as $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus B, R = A \oplus C)$. The quantum cost of Double Feynman gate is 2 [8]. The Double Feynman gate is shown in Fig. 4.

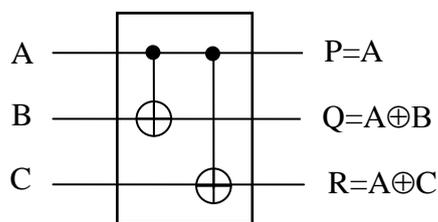


Fig.4. 3*3 Double Feynman gate

D. Toffoli Gate:

Toffoli gate (TG) is one of the most popular reversible gates, invented by Tommaso Toffoli. It is also known as the Controlled-Controlled-NOT(C-C-NOT) gate. The input vector I_v and output vector O_v of 3*3 Toffoli gate [9] is defined as $I_v = (A, B, C)$ and $O_v = (P = A, Q = B, R = AB \oplus C)$. The quantum cost of Toffoli gate is 5. It requires 2V, 1V⁺ and 2 CNOT gates. The Toffoli gate is shown in Fig. 5.

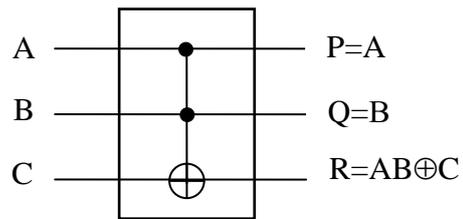


Fig.5. 3*3 Toffoli gate

E. Peres Gate

The input vector I_v and output vector O_v of 3*3 Peres gate (PG) [10] is defined as follows: $I_v = (A, B, C)$ and $O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$. It is just like a Toffoli gate but without the last Feynman gate from right. Since it requires 2V, 1V⁺ and 1 CNOT gate, it has the Quantum cost of 4. The Peres gate is shown in Fig. 6.

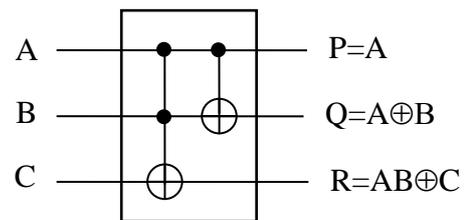


Fig.6. 3*3 Peres gate

IV. PROPOSED REVERSIBLE COUNTER USING T FLIP-FLOP

Even though many research has been done in sequential logic circuits, but quantum cost minimization create a vest research area. Fredkin and Toffoli [11] first proposed the design of reversible sequential circuits. Recently Positive Polarity Reed Muller (PPRM) expression is used to design synchronous counter by Khan [17]. We have a proposal for designing a synchronous and asynchronous counter, in which cost metrics are minimized. To design this counter at first we have proposed two design of reversible T flip-flop which is the core component of the counter.

A. Proposed clocked T Flip-Flop

The characteristic equation of a T flip-flop is $Q^+ = (T \oplus Q).C \oplus \bar{C}.Q$. The same result can also be obtained from simplified equation as $Q^+ = (T \cdot C) \oplus Q$. It can be mapped with the Toffoli gate. Our proposed clocked T flip-flop in Fig. 7 is realized by a Toffoli gate and a Feynman gate. The proposed T flip-flop has quantum cost 6, delay 6 and has the bare minimum of 1 garbage bit.

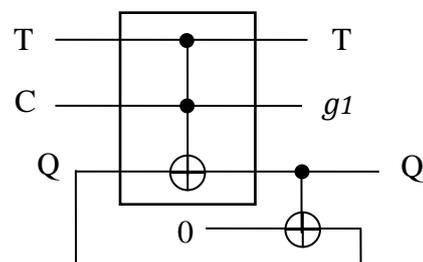


Fig.7. Proposed reversible T flip-flop

The characteristic equation of a T flip-flop can also be mapped with the Peres gate. Our proposed another clocked T flip-flop is realized by a Peres gate and a Feynman gate in (Fig. 8) with quantum cost 5, delay 5 and garbage bit 1.

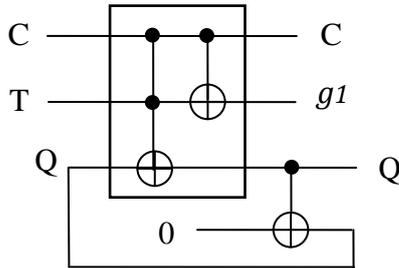


Fig.8. Proposed reversible T flip-flop

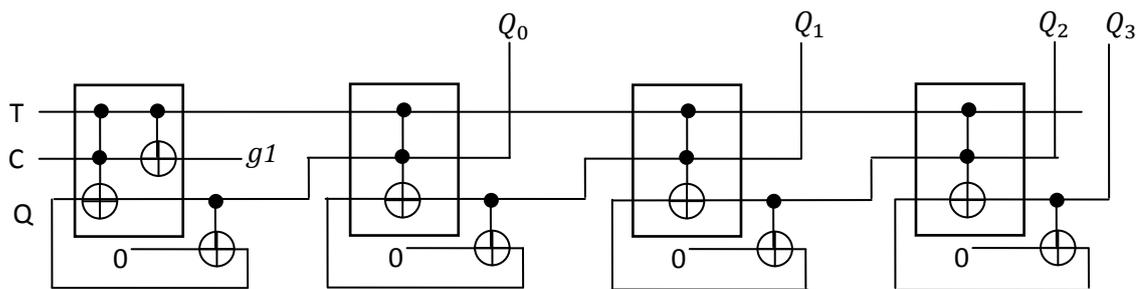


Fig.9. Proposed design of reversible 4-bit asynchronous counter

Table I. Comparisons of proposed asynchronous counter with existing design

4-bit asynchronous counter	Cost comparison		
	Quantum cost	Delay	Garbage outputs
Proposed	23	23	1
Existing[18]	55	55	12
Improvement in (%) w.r.t. [18]	58.18	58.18	91.66

Theorem: To construct n bit asynchronous counter, if g is the total number of gates required to design the counter producing b number of garbage outputs then $g \geq 2n$ and $b=1$.

Proof: Each flip-flop consists of two gates; n bit counter requires n number of flip-flops. No additional gates are required to interconnect each other. So total number of gates required to design the counter is $2n$, hence $g \geq 2n$. Similarly, only the first flip-flop produces one garbage output. No garbage output produced while interconnection among flip-flops. So the total number of garbage out is fixed 1, hence $b=1$.

Theorem: The quantum cost of an n bit asynchronous counter is $Q_c \geq 6n-1$.

Proof: For $n=1$, only one Peres gate and one Feynman gate is required to construct the counter. The quantum cost of Peres gate is 4 and quantum cost of Feynman gate is 1. So the total cost $4+1=5$.

Now for $n>1$, one Toffoli gate and one Feynman gate is required for each flip-flop in the counter except the first one which requires one Peres gate instead of Toffoli gate. So for n bit asynchronous counter it needs $(n-1)$ Toffoli

B. Proposed Reversible Asynchronous Counter

In proposed asynchronous counter each flip-flop is connected to a constant input T. The clock input of the first flip-flop is connected to the clock line and other three flip-flops use their clock inputs driven by the Q output of the preceding flip-flop in Fig. 9. The flip-flop holding the least significant bit receives the incoming count pulse. The counter is constructed by using 3 Toffoli gates, 1 Peres gates and some Feynman gates. The resulting quantum cost is 23, delay 23 and garbage output 1. Comparisons with existing result are given in Table I.

gate, n Feynman gate and one Peres gate. The quantum cost of Toffoli gate is 5. So the total quantum cost is $5*(n-1) + 1*(n) + 4 = 6n-1$, Hence $Q_c \geq 6n-1$.

C. Proposed Reversible Synchronous Counter

In synchronous counter all flip-flops are clocked at the same time by a common clock pulse. Thus all flip-flops change state simultaneously. In proposed synchronous counter the flip-flop changes its state only when all the preceding flip-flops are in the state $Q = 1$ shown in Fig. 10. This 4-bit synchronous counter has quantum cost 32, delay 32 and garbage output 4. Comparisons with existing result are shown in Table II.

Table II. Comparisons of proposed synchronous counter with existing design

4-bit synchronous counter	Cost comparison		
	Quantum cost	Delay	Garbage outputs
Proposed	32	32	4
Existing [17]	35	35	4
Improvement in (%) w.r.t. [17]	8.5	8.5	0

Theorem: To construct n (≥ 3) bit synchronous counter, if g is the total number of gates required to design the counter producing b number of garbage outputs then $g \geq 4n-4$ and $b \geq n$.

Proof: Each flip-flop consists of two gates; n bit counter requires n number of flip-flops. For $n=3$, one Toffoli and one Feynman is required to carry out all the outputs to the next higher positioned flip-flop.

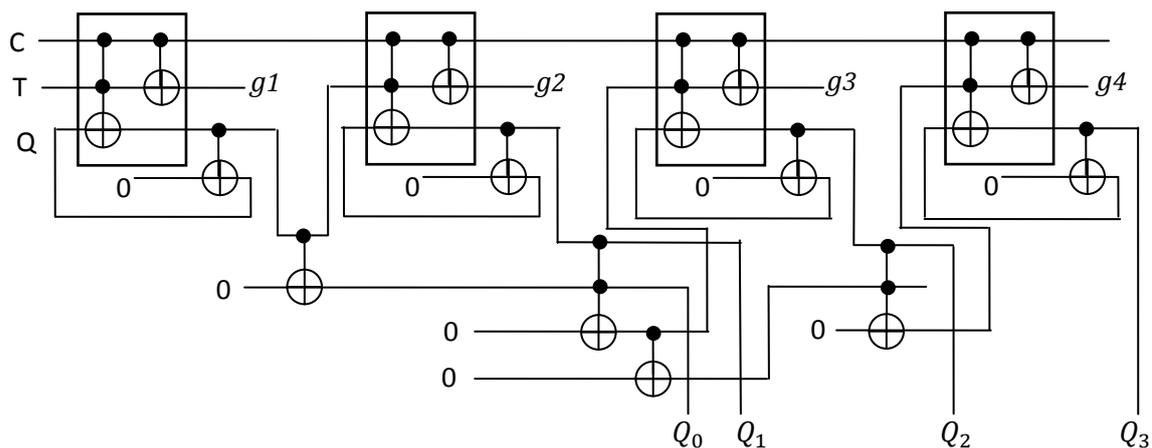


Fig. 10. Proposed design of reversible 4-bit synchronous counter

So total number of gates required is $3*2+2=8$. For $n>3$, $2n$ number of gates required for the flip-flops and $2(n-2)$ number of gates are required to carry out all the lower outputs to the next higher outputs. So the total number of gates required is $2n+2(n-2)=4n-4$. Every flip-flop produces only one garbage output. No garbage output produced while interconnection among flip-flops and to carry out outputs to next higher flip-flop. So the total number of garbage out is n , hence $b \geq n$.

Theorem: The quantum cost of an $n (\geq 3)$ bit synchronous counter is $Q_C \geq 11n-12$.

Proof: For $n (\geq 3)$ bit synchronous counter it requires n flip-flops. Each flip-flop consists of one Peres gate and one Feynman gate. Additional $(n-2)$ Toffoli gates and $(n-2)$ Feynman gates are required to carry out all the outputs to the next higher flip-flop. So it requires n number of Peres gate, $(n-2)$ number of Toffoli gates and $n+(n-2)=2n-2$ number of Feynman gates. Quantum cost of Peres gate is 4, Toffoli gate is 5 and Feynman gate is 1. So total quantum cost = $4*n + 5*(n-2)+1*(2n-2)=11n-12$, hence $Q_C \geq 11n-12$.

V. CONCLUSION

A novel design of 4-bit synchronous and asynchronous counter with the help of T flip-flops has been proposed. Tables I and II demonstrates that the comparison is carried out for reversible counter circuit is better than the existing designs in terms of quantum cost, delay and garbage outputs. Appropriate theorems and proof are presented to clarify the proposed design and establish its efficiency. We believe this optimization can contribute significantly in reversible logic community.

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