

Performance Analysis of RCA - CSKA and CSA with Proposed Adder Cell

K. Samanna¹, M. Mahaboob Basha²

M. Tech Scholar, ECE Department, AVR&SVR CET Nandyal, Kurnool, Andhra Pradesh, India¹

Associate Professor, ECE Department, AVR&SVR CET, Nandyal, Kurnool, Andhra Pradesh, India²

Abstract: In this work, 32-bit ripple carry adder, Carry Skip adder and Carry Save adder circuits have been proposed with ten transistor based one bit full adder. Lower area and high performance chips are the most important parameters in today's VLSI designs. The minimum power consumption target and lower area can be met by decreasing the hardware size and which is achieved by reducing the transistor count. Therefore the three designed circuits have been simulated by using Microwind 3.1 VLSI CAD tool. Various parameters such as area, power dissipation, propagation delay and PDP have been determined from layouts of feature size 90nm and 65nm technologies. The adder circuits have been analyzed using BSIM 4 parameter analyzer. Finally the simulation results were compared with conventional adders in terms of total power consumption, delay, area and power delay product.

Keywords: CMOS; Conventional Full Adder; Low Power design; 32-bit RCA;32-bit CSKA; 32-bit CSA.

I. INTRODUCTION

The rapid development in the fields of Electronics and Computer Science Engineering has led to the fast growth of Very Large Scale Integrated (VLSI) circuits applications. Most of the VLSI applications such as digital signal processing, image and speech processing and microprocessors, use arithmetic operations very extensively. The most commonly used arithmetic operations are addition and multiplication. The 1-bit full adder cell is the basic building block for all arithmetic operations. Therefore improving its performance is vital to increase the performance of the overall modules. The increasing usage of portable devices such as mobile phones, ipads, tablets, MP3 players etc., has led to the need of redesigning the existing operations modules to improve their performance in some aspects, mainly in power dissipation and area required. Hence the research of low power, high performance adder cells is gaining a lot of importance. [1].

Moreover the proper choice of logic style is very crucial for implementing the combinational circuits for considerable power savings. There are number of power reduction techniques adopted to reduce the power consumption at circuit level and integrated circuit level such as reducing supply voltage and reducing transistor size. Due to the quadratic relation between supply voltage and power, the reduction in supply voltage is the effective technique to reduce the power consumption. However there will be a large leakage current will flow due the decrease of threshold voltage when supply voltage is decreases, which in turn decrease the performance of the circuit. Therefore in this paper different adders circuits were implemented at 90nm and 65nm technologies based on ten transistors one bit full adder.

The rest of the paper is organised as follows. The basic concept of adder architecture is discussed in section II. Section III describes design of 32-bit adders with 28

transistors. The Proposed 32-bit adder circuits with 10T full adder cell are discussed in Section IV. Power, Area, Delay and PDP Calculations and comparison of results Using Microwind VLSI Cad Tool is presented in section V. Section VI conclude this paper.

II. DESIGN OF CONVENTIONAL FULL ADDER

Conventional Full adder is a combinational circuit that performs addition between two bits taking into account that a one may have been added lower significant stage.

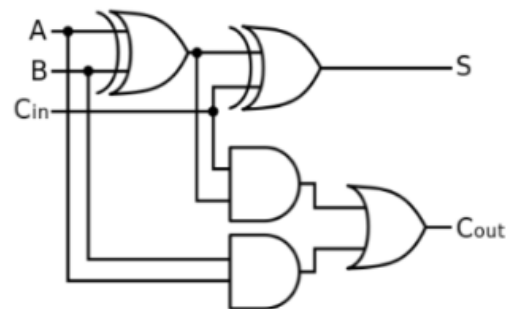


Fig.1 Logic Circuit of Conventional Full adder.

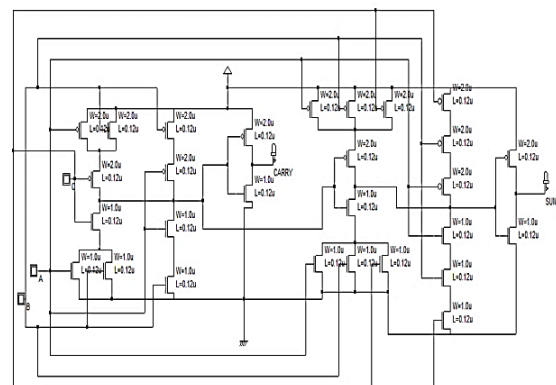


Fig2. Transistor Level Circuit of Conventional Full adder.

This circuit has three inputs and two outputs. The three inputs A, B and C denote the minuend, subtrahend and carry respectively.[2].

The two outputs S and C_{out} represent sum and carry, respectively. The logic circuit and transistor level schematic of full adder is shown in Fig.1 & Fig 2.and truth table in Table I. [3],[4].

TABLE1 TRUTH TABLE OF FULL ADDER

Inputs			Outputs	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = A \text{ xor } B \text{ xor } C$

$C_{out} = AB + BC + AC$

Where A, B, C inputs and S, Cout are outputs..

III.DESIGN OF 32-BIT RCA, CSKA AND CSAA WITH CONVENTIONAL FULL ADDER

Conventional Full Adder with twenty eight transistors is used for designing 32-bit ripple carry adder, carry skip adders and Carry Save adders. As arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates like AND, OR and universal gates like NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).[6]. Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs a C_{in}, which is the C_{out} of the previous adder. This kind of adder is a Ripple Carry Adder, since each carry bit "ripples" to the next full adder.

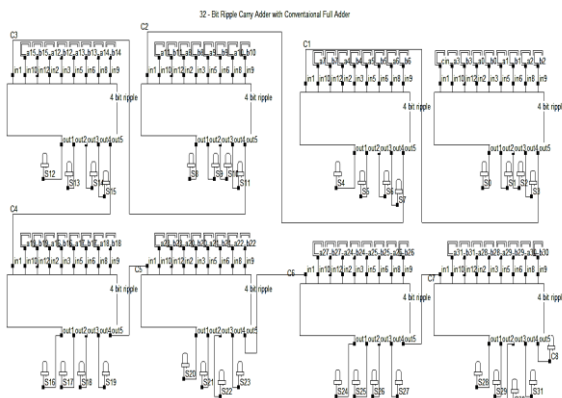


Fig 3. 32-Bit RCA with Conventional Full adder.

The block diagram of 32-bit Ripple Carry Adder is shown here below.[7],[8]. The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. The carry skip adder divides the words to be added into blocks. Within each block, ripple carry is used to produce the sum bit and the carry. The Carry Skip Adder reduces the delay due to the carry computation i.e. by skipping over groups of consecutive adder stages [9]. • If each A_i ≠ B_i in a group, then we do not need to compute the new value of C_{i+1} for that block; the carry-in of the block can be propagated directly to the next block. • If A_i = B_i = 1 for some i in the group, a carry is generated which may be propagated up to the output of that group. • If A_i = B_i = 0, a carry, will not be propagated by that bit location. The basic idea of a carry-skip adder is to detect if in each group all A_i ≠ B_i and enable the block's carry-in to skip the block when this happens as shown in figure1. In general a block-skip delay can be different from the delay due to the propagation of a carry to the next bit position [10],[11]. With carry skip adders, the linear growth of carry chain delay with the size of the input operands is improved by allowing carries to skip across blocks of bits, rather than rippling through them. Fig 4 represents 32-bit carry skip adder with conventional full adder.

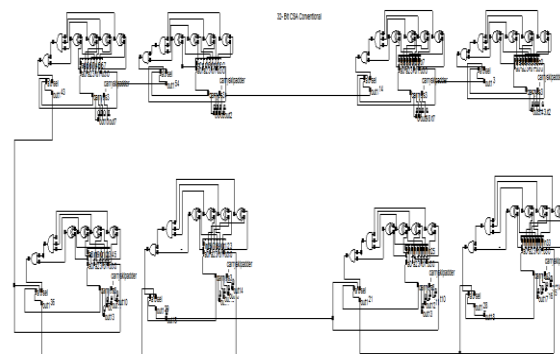


Fig. 4 32-Bit CSKA with Conventional Full adder.

A Carry-Save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.

Consider the sum:

$$\begin{matrix} 12345678 + \\ 87654322 \\ \hline \text{Result}=100000000. \end{matrix}$$

Using the arithmetic we learned as children, we go from right to left, "8+2=0, carry 1", "7+2+1=0, carry 1", "6+3+1=0, carry 1", and so on to the end of the sum. Although we know the last digit of the result at once, we cannot know the first digit until we have gone through every digit in the calculation, passing the carry from each digit to the one on its left. Thus adding two n-digit numbers has to take a time proportional to n, even if the machinery we are using would otherwise be capable of

performing many calculations simultaneously. Carry-save arithmetic works by abandoning the binary notation while still working to base 2.

It computes the sum digit by digit, as
 $101110101010110111100000001101+$
 $1101111010101011011111011101111$
 $= 21122120202022022122111011102212.$

The notation is unconventional but the result is still unambiguous. Moreover, given n adders (here, n=32 full adders), the result can be calculated in a single tick of the clock, since each digit result does not depend on any of the others. If the adder is required to add two numbers and produce a result, carry-save addition is useless, since the result still has to be converted back into binary and this still means that carries have to propagate from right to left. But in large-integer arithmetic, addition is a very rare operation, and adders are mostly used to accumulate partial sums in a multiplication. Fig.5 represents 32-bit Carry Save adder.[13].

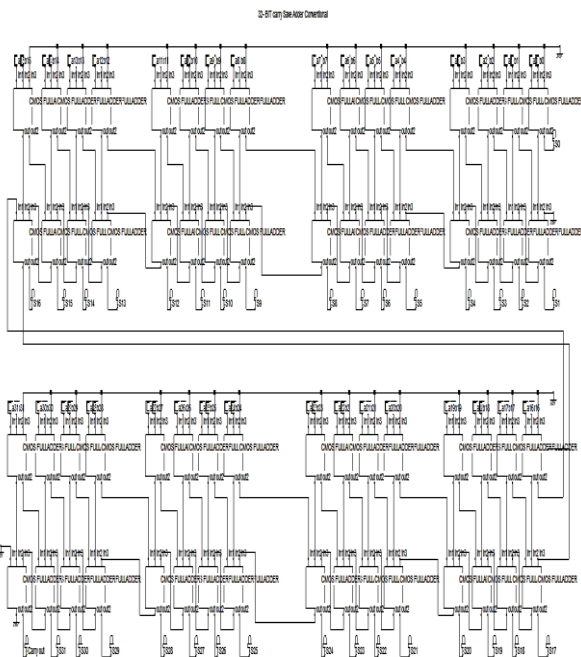


Fig 5. 32-bit CSA cell with Conventional Full adder.

IV. DESIGN OF PROPOSED ADDER CELL

The Circuit diagram of ten transistors based Full Adder is shown in Fig 6. and the designed circuit is used for implementing four bit, sixteen bit and thirty two bit ripple carry, Carry Skip and carry save adders for analysing the performance of proposed adder cells in terms of area, power, delay and power delay product.[5].

Table II, and III represents performance analysis of conventional and Proposed 32-bit Ripple Carry, Carry Skip and Carry Save Adders at 90nm and 65nm technologies, Table IV shows number of transistors required for implementing one bit full adder for Conventional and Proposed one, Table V shows number of Full Adder cells required for implementing 32-bit RCA/CSKA/CSA's. Fig 3, Fig 4 and Fig 5 Shows 32-bit RCA/CSKA/CSA's by Conventional Full Adder and Fig

7, Fig 8 and Fig 9 Shows 32-bit RCA/CSKA/CSA's by Proposed Full Adder with ten transistors, Fig 10, Fig 11 & Fig.12 represents Layouts of 32-bit RCA/CSKA/CSA's with Proposed Full Adder, where as Fig 13 and Fig 14 represents Graphical analysis of the results tabulated in Tables II, III. Table IV represents performance Parameters of different adder circuits. Table V represents no. of transistors required for implementing 32-bit RCA/CSKA/CSA. Table VI represents Performance of different adders rank wise.

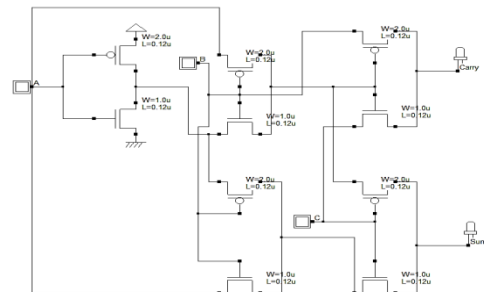


Fig6. Full adder cell with ten transistors.

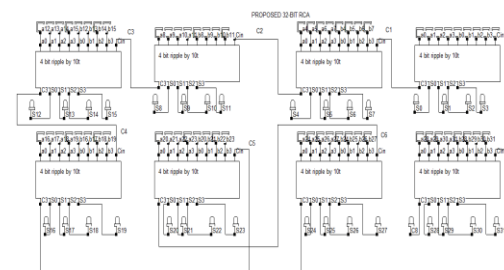


Fig7. 32-bit Ripple Carry Adder cell proposed adder cell.

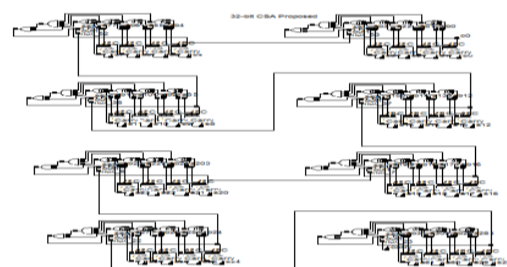


Fig8. 32-bit CSKA cell proposed adder cell.

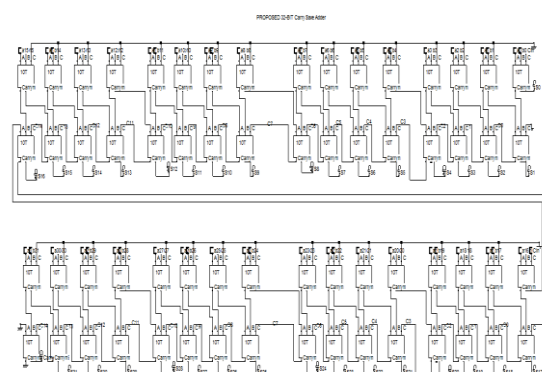


Fig 9. 32-bit CSA cell proposed adder cell.

V. SIMULATION RESULTS

For the designed 32-bit RCA, CSKA and CSA's circuits with Conventional and proposed Adder cells, simulation were carried out with Microwind 3.1 CAD tool in 90nm and 65nm technologies. Comparative analysis is done in terms of area, power, delay and power delay product at room temperature [12].

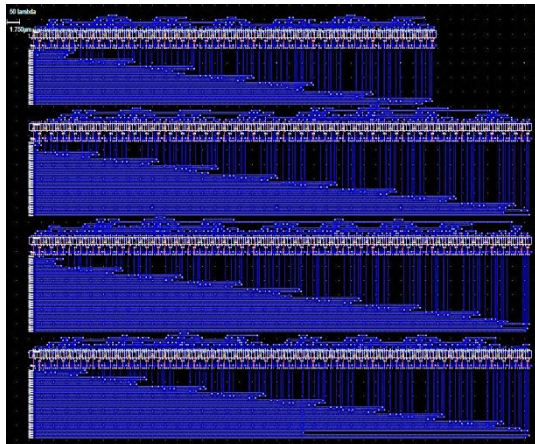


Fig 10. Layout of 32-bit Rippple Carry Adder with Proposed Full adder.

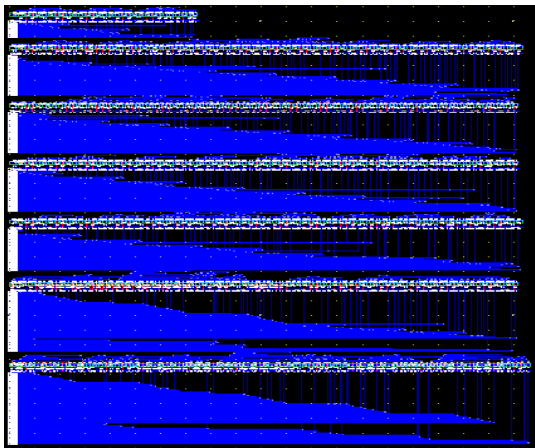


Fig11. Layout of 32-bit Carry Skip Adder with Proposed Full adder.

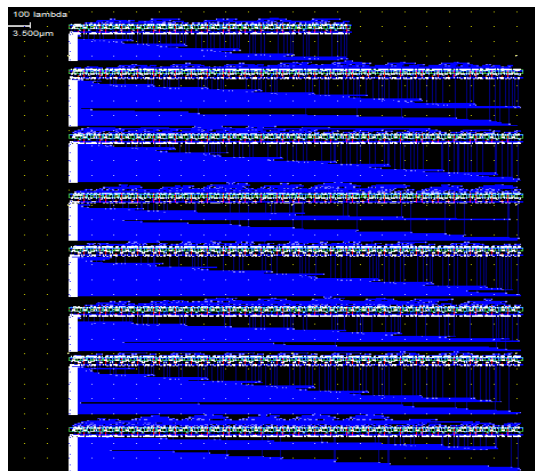


Fig 12. Layout of 32-bit Carry Save Adder with Proposed Full adder.

TABLE2 SIMULATION RESULTS OF CONVENTIONAL AND PROPOSED CIRCUITS IN 90NM/27°C

ADDERS	ARE A (μm ²)	PO WE R in (μw)	DEL AY in (ns)	PDP VALUE(μw X ns)
CONVENTIO NAL FULL ADDER	770	205.00	0.480	98.40
32- bit RCA	6348	464.00	23.67	10982.8
32- bit CSKA	10998	478.00	6.800	3250.4
32- bit CSA	14076	722.00	23.715	17122.2
PROPOSED FULL ADDER	252	48.849	0.345	16.852
32- bit RCA	3404	69.828	6.925	484.04
32- bit CSKA	6392	260.00	5.380	1398.8
32- bit CSA	6072	158.00	8.935	1411.7

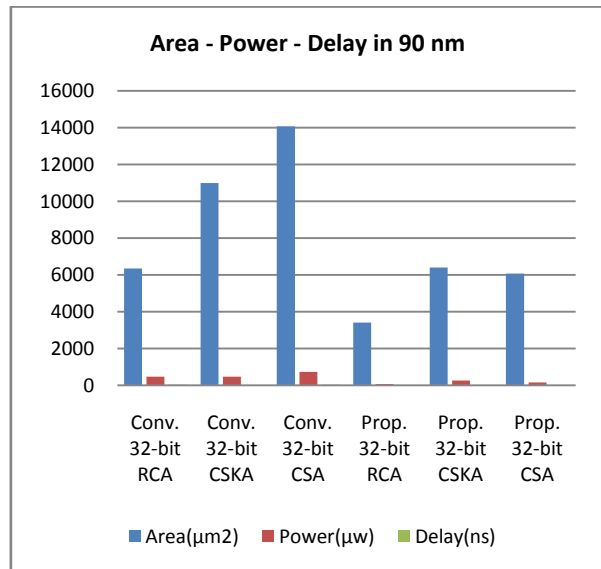


Fig 13. Graphical Analysis of the results tabulated in Table II

TABLE3. SIMULATION RESULTS OF CONVENTIONAL AND PROPOSED CIRCUITS IN 65NM/27°C

ADDERS	AR EA (μ m ²)	POW ER in (μw)	DEL AY in (ns)	PDP VALU E(μw X ns)
CONVENTIONA L FULL ADDER	480	93.768	0.432	40.507
32- bit RCA	3888	195.00	11.610	2263.9
32- bit CSKA	6643	214.00	3.432	734.44

32- bit CSA	8568	331.00	10.703	3542.6
PROPOSED FULL ADDER	154	24.574	0.318	7.814
32- bit RCA	2088	31.025	3.396	105.36
32- bit CSKA	3796	112.00	2.612	292.54
32- bit CSA	3672	72.318	4.113	297.44

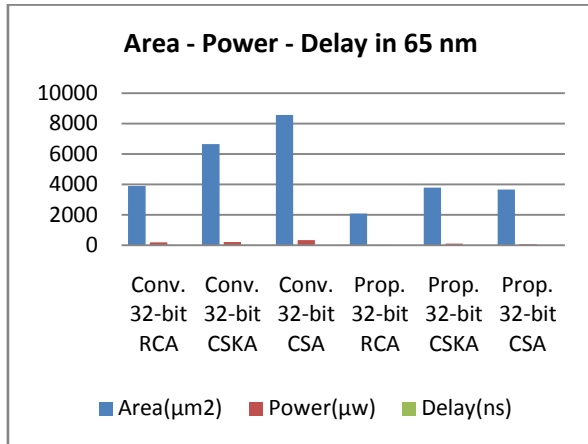


Fig 14. Graphical Analysis of the results tabulated in Table III.

TABLE4. NO. OF TRANSISTORS REQUIRED FOR IMPLEMENTING ADDER CELL

No. of Transistors	Pmos	Nmos
Conventional	14	14
Proposed	5	5

TABLE5. NO. OF TRANSISTORS REQUIRED FOR IMPLEMENTING 32-BIT RCA/CSKA/CSAA

Type of Adder	Number of Transistors
32- bit RCA	320
32- bit CSKA	450
32- bit CSA	640

TABLE6. PERFORMANCE OF DESIGN CIRCUITS BY RANK AREAWISE:

Rank	Name of the Circuit	Area (µm ²)
1	32-bit RCA	2088
2	32-bit CSA	3672
3	32-bit CSKA	3796

POWER WISE:

Rank	Name of the Circuit	Power (µW)
1	32-bit RCA	31.025
2	32-bit CSA	72.318
3	32-bit CSKA	112.00

DELAY WISE:

Rank	Name of the Circuit	Delay (ns)
1	32-bit CSKA	2.612
2	32-bit RCA	3.396
3	32-bit CSA	4.113

POWER DELAY PRODUCT:

Rank	Name of the Circuit	PDP (µw X ns)
1	32-bit RCA	105.36
2	32-bit CSKA	292.54
3	32-bit CSA	297.44

VI. CONCLUSION

The three different circuits have been simulated using Microwind/DSCH 3.1 VLSI CAD tool in 90nm and 65nm technologies with BSIM4 analyser. From the results it is observed that 32-bit Ripple Carry Adder with Proposed Adder cell is Energy Efficient one as the power delay product value is less compared to other architectures and carry skip adder achieve first rank in case of propagation delay.

As the proposed techniques reduce the PDP to great extent compared conventional one, these circuits can be used as the primary building blocks of DSP processors for the better energy efficiency.

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