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Power Reduction using Single Ended 8T SRAM Cell with NBTI Technique

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Abstract: Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence but it is still volatile in the conventional sense that data are eventually lost when the memory is not powered. In this paper, a new 8T SRAM cell, which employs a single bitline scheme to perform the write and read operations, is proposed. This scheme enhances the write ability and read stability by cutting off the feedback loop of the inverter pair, thereby eliminating the read and write constraints on the transistor dimensions. SRAM based structures within the processor are especially liable to NBTI as one of the PMOS devices in the memory cell always has an input "0". So in order to reduce the power consumption, an inverter is connected to the other end of NMOS device, such that the inverter replaces the ground. Now the size may be somewhat increased but the power leakage is controlled by the use of the inverter.

Keywords: SRAM, NMOS, PMOS, NBTI

I. INTRODUCTION

SRAM cell design requires a careful balance of read stability, write margin and data retention in standby. Device sizing to minimize SRAM cell area and leakage power while achieving high-speed operation should also be considered. To solve these difficulties, design techniques to mitigate variations in large-scale SRAM have been extensively studied by many researchers. In general, read-assist circuits reduce write margins, while write assist circuits degrade read margins. Because of this trade-off, special care should be taken to evaluate theleast area overhead (<1%) among all schemes. Both PBL and PWL-RMW provide the best improvements (26X) in effective cell failure rate at 0.7V Vcc, but incur significant area overhead (4-8%) since they need pulsing circuits or sense-amps per-column. At 0.7V Vcc, PWL improves effective cell failure rate by 15X while incurring <1% area overhead. Both PBL &PWL-RMW provide the best improvements in cell stability at low Vcc but their area overheads are significant.

Due to increased demand of small feature size SRAM on the chips increases the demand of excessive power, particularly, in wireless sensor nodes and mobile applications. However, as the voltage is scaled down to combat the rise in power and other issues like the lower noise margins (responsible for cell stability) arise in conventional 6T SRAM cells. Solutions involving additional transistors, i.e. 7T and 8T cells have been explored to lower power consumption while reducing these adverse effects in the cell performance. We will therefore look into one of these SRAM cell topologies, the 8T SRAM cell which operates at sub-threshold voltages successfully.Traditional 6T SRAM face many challenges in deep sub-micron technologies. Predictions in suggest that the variations will limit the voltage scaling because of the degradation in SNM and write margin. Further, such data destruction may even occur at normal Vdd levels due to the increase in transistor mismatch that accompanies geometrical scaling.

Additionally, techniques for boosting the supply voltage in SRAMshave been proposed to achieve more stable data retention during read operation. 8T SRAM cell has a much greater enhancement in stability by eliminating cell disturbances during a read access and thus facilitating the continued technology scaling.

It also requires separate read and write word-lines but without read disturbances so that the SNM improves significantly.

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II. BACKGROUND AND RELATED WORKS

A. 6T SRAM

Static random access memory (SRAM) can retain its stored information as long as power is supplied. This is in contrast to dynamic RAM (DRAM) where periodic refreshes are necessary or non-volatile memory where no power needs to be supplied for data retention, as for example flash memory.

The term ``random access" means that in an array of SRAM cells each cell can be read or written in any order, no matter which cell was last accessed. The structure of a 6 transistor SRAM cell, storing one bit of information, can be seen in The core of the cell is formed by two CMOS inverters, where the output potential of each inverter is fed as input into the other . This feedback loop stabilizes the inverters to their respective state. The access transistors and the word and bit lines, WL and BL, are used to read and write from or to the cell. In standby mode the word line is low, turning the access transistors off.

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In this state the inverters are in complementary state. When the p-channel MOSFET of the left inverter is turned on, the potential is high and the p-channel MOSFET of inverter two is turned off.To write information the data is imposed on the bit line and the inverse data on the inverse bit line, BLB.

Then the access transistors are turned on by setting the word line to high. As the driver of the bit lines is much stronger it can assert the inverter transistors. As soon as the information is stored in the inverters, the access transistors can be turned off and the information in the inverter is preserved.

The memory cell shown here forms the basis for most static random-access memories in CMOStechnology. It uses six transistors to store and access one bit. The four transistors in the center form two cross-coupled inverters. In actual devices, these transistors are made as small as possible to save chip-area, and are very weak.

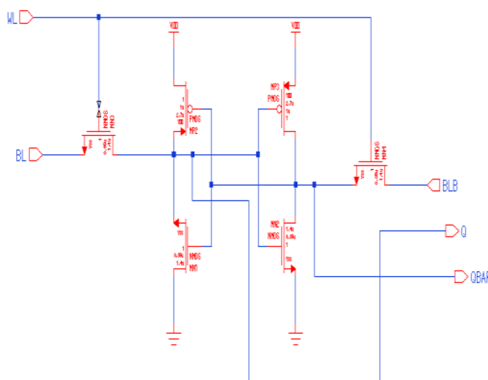

Fig.1 6T SRAM

Due to the feedback structure, a low input value on the first inverter will generate a high value on the second inverter, which amplifies (and stores) the low value on the second inverter. Similarly, a high input value on the first inverter will generate a low input value on the second inverter, which feeds back the low input value onto the first inverter.

Therefore, the two inverters will store their current logical value, whatever value that is. The two lines between the inverters are connected to two separate bitlines via two n-channel pass-transistors (left and right of the cell). The gates of those transistors are driven by a wordline. In a larger SRAM, the wordline is used to address and enable all bits of one memory word (e.g. all 32 bits at address 0xcafe from a 64Kx32 SRAM chip). As long as the wordline is kept low, the SRAM cell is disconnected from the bitlines. The inverters keep feeding themselves, and the SRAM stores its current value. When the wordline is high, both n-channel transistors are conducting and connect the inverter inputs and outputs to the two vertical bitlines.

That is, the two inverters drive the current data value stored inside the memory cell onto the bitline (left) and the inverted data value on the inverted-bitline (right). This data can then be amplified and generates the output value of the SRAM cell during a read operation.

B. 7T SRAM

The below Fig show the circuit diagram and the operation waveform of the proposed cell scheme, respectively. The salient feature of the scheme is an additional nMOS connected to the source of driver nMOS transistors of the memory cell, which enables small swing of bit lines in a write operation. This additional nMOS is referred as the switch Vss in the rest of this paper. A bit line is precharged to Vdd - Vtn by an nMOS load transistor and is pulled down to Vdd – Vtn -DBL in a write "0" operation, where Vtn and BLB are threshold voltage of the load nMOS and write swing, respectively.

The precharge level must not be Vdd because access transistors of the cell cannot turn on in the write operation in this scheme. There is no additional power consumption even if the write and read cycles come alternately, because there is no mismatch between the voltage level of bit lines in read cycles and that in write cycles. The source-line control signal is synchronized with the word line signal WL, and the switch Vss is turned off before WL goes up to high in a write cycle.

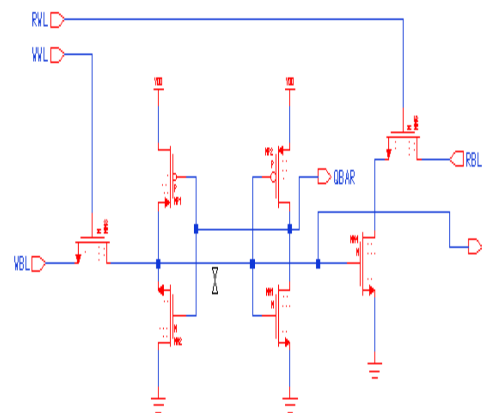

Fig. 2 7T SRAM

Even if the voltage difference between a pair of bit lines is small, the cell node can be inverted because the driver nMOS transistors do not draw current while the word line is activated, to the switch. Here the 7T uses the two invertors which are cross coupled in the middle order, such that different single ended transistors composed of write bit line(WBL),read bit line(RBL),write word line(WWL) and read word line(RWL).

The floating charge Qc is at the end of WBL transistor, so the output of 7T is obtained in Q and its inversion is at QBAR. A 7T SRAM cell is used with a separate double ended write port and a single ended read port. By separating the two ports has advantages:the write periphery is not needed in short read bit lines, the write bit lines can be controlled by the use of static invertors, which inturn reduces the power dissipation.

C. SINGLE ENDED 8T SRAM

The process variations which mainly include the random threshold voltage variations due to dopant fluctuations, line edge roughness and poly gate grain size variations are responsible for degrading the stability of the memory and

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hence significantly reduce the DC read, write and retention margins of CMOS SRAM cells. On the other side, the SRAM size on the chip has been continuously increased along with the advancement of microprocessors.Thus, to satisfy the functionality of a large number of SRAM cells in memory and thus achieve high yield, the design has to provide more stability than 6T SRAM. To improve the stability of the SRAM cell, topology of the conventional 6T SRAM cell has been changed and various new topologies have been proposed. This work analyses the SRAM's Stability factors for 8T at various process corners using 65nm CMOS technology. In this paper the read & write stability is being discussed. It is observed that 8T SRAM cell has much better static noise margin (SNM) as compared to conventional 6T SRAM cell.

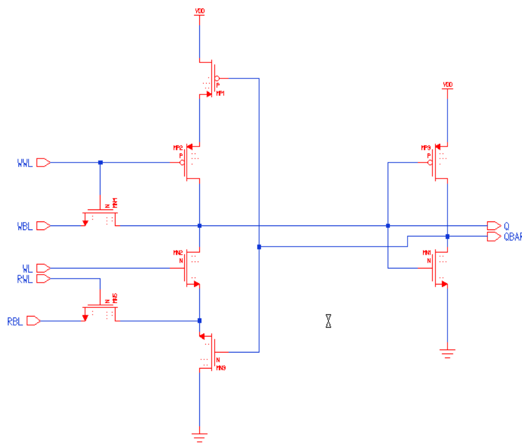

Fig. 3 8T SRAM

III. PROPOSED METHOD

Negative Bias Temperature Instability (NBTI) is a well-known reliability concern for PMOS transistors. We review the literature to find seven key experimental features of NBTI degradation. These features appear mutually inconsistent and have often defied easy interpretation. By reformulating the Reaction-Diffusion model in a particularly simple form, we show that these seven apparently contradictory features of NBTI actually reflect different facets of the same underlying physical mechanism.

Basically this new single ended 8T SRAM cell consists of an inverter which replaces the two ground of the SRAM cell.So in the ideal stage(where there is no data)the power leakage in the PMOS is reduced considerably by the use of the invertor.

The PMOS transistor is negatively biased for certain period of time which is also called as stress mode.The interface traps are eliminated by applying of input logic '1' to the gate terminal(Vgs=0).

In this paper we are going to tackle this NBTI problem by increasing the recovery time.

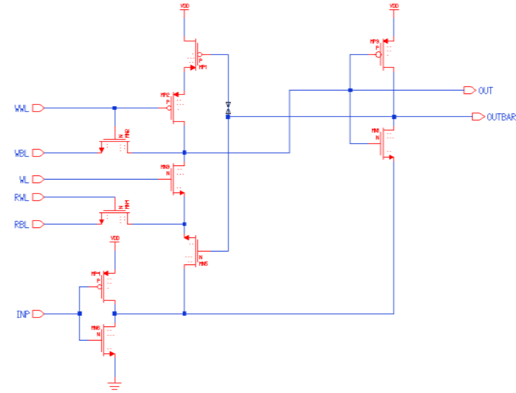

Fig. 4 8T SRAM Using Recovery Boosting

This method is called as recovery boosting and it is valid only when the data is considered as invalid.

During the normal mode of operation the inverter has an input has a value '1'which in turn consider the value as output '0' that is taken as ground.The ground voltage node is raised as the input has an output '1' of the SRAM cell.

IV. RESULTS AND DISCUSSION

By implementing the 6T, 7T and 8T SRAM using the MENTORGRAPHICS tool, the results are as follows,

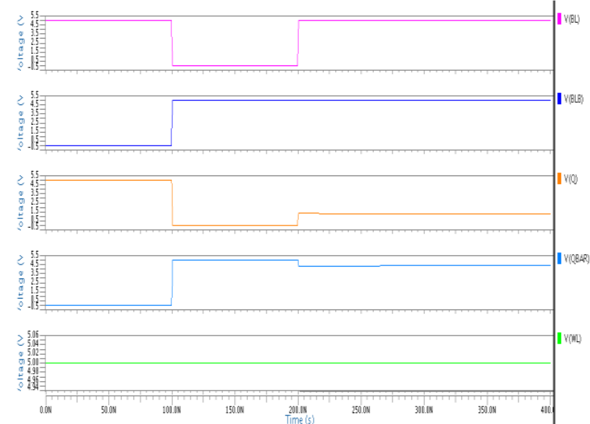

Fig. 5 Output of 6T SRAM

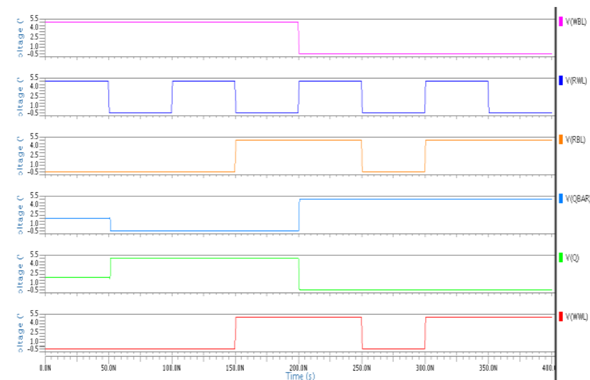

Fig. 6 Output of 7T SRAM

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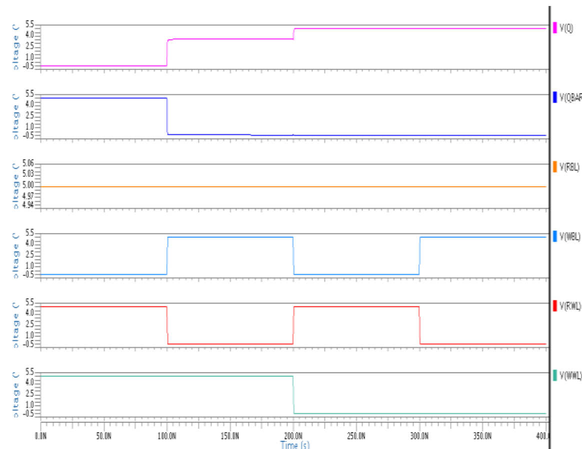

Fig. 7 Output of 8T SRAM

In this new method, the world line (WL)is always in the active low inorder to perform both read and write operations.

TABLE I

Features	Existing 8T	Proposed 8T
Total Power Dissipation	1.7401mWATTS	3.851pWATTS

V. CONCLUSION

Thus NBTI is one of the most important reliability problem faced by processor designers.The SRAM cells are vulnerable to NBTI ,as the input to one of PMOS device in the cell always use logic '0'.In this paper a new method was proposed by connecting an inverter to the drain of two NMOS ,which creates a recovery boosting method. As single ended 8T SRAM cell is best among the other 6T and 7T SRAM cells, thereby reducing the switching activities. Hence, because of this recovery boosting technique, the power dissipation of the memory cell is reduced as shown in the table.

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