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Optimization of the Digital Radio Mondiale Receiver Software Implementation to Support Digital Radio Mondiale Plus on DSP

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Abstract: Digital Radio Mondiale is a standard for digital radio broadcasting. To reduce number of cycles consumption, optimization is done to different modules of the current software implementation of the DRM receiver. Profiling is done to all modules. Cycle intensive modules are identified and optimized by using intrinsics. Correlation function achieved optimization with overall ~69% reduction, resample module achieved optimization of ~91.03% reduction, base band filter achieved ~47% reduction and signal presence tacking module optimization resulted in ~49.5% reduction. There is no degradation in the sensitivity of the receiver after optimization. Optimization has brought improvement in the processing time.

Keywords: Digital Radio Mondiale (DRM), Million Cycles per Second (MCPS), Intrinsic, Profiling.

I. Introduction

Digital Radio Mondiale (DRM) is a new digital radio broadcasting standard, to bring analog AM radio into digital era. This was developed by DRM consortium members and was approved by the European Telecommunication Standard Institute (ETSI) in 2001. The perceived audio quality is much better and the reception is more reliable. It also provides additional text and data services. It provides different transmission modes and different bandwidths to cope up with different channel conditions. Maximum bandwidth is 20 kHz and no of OFDM carriers is less. These features motivate real time software implementation of a DRM receiver on a DSP. Through profiling cycle intensive modules are identified for the current software implementation and these are optimized by loop unrolling and by using core specific intrinsic to reduce number of cycles consumption.

II. System Overview

Band of frequencies used for DRM broadcasting below 30 MHz are as follows, the low frequency band from 148.5 to 283.5 kHz in region 1, the medium frequency band from 526.5 to 1606.5 kHz in regions 1 and 3 and from 525 to 1705 kHz in region 2 and the high frequency bands from 2.3 to 27 MHz worldwide. Band of frequencies used for DRM+ broadcasting above 30 MHz are as follows, analog television broadcasting (Band I) : 47Mhz to 68MHz, OIRT FM Band : 65.8MHz to 74MHz, Japanese FM Band : 76MHz to 90 MHz, FM Radio Broadcasting (Band II) : 87.5MHz to 107.9 MHz and Digital Broadcasting (Band III) : 174MHz to 240 MHz.

Typically channel bandwidth for radio broadcasting below 30 MHz is 9/10 kHz, it supports half channel bandwidth 4.5/5 kHz to support simulcast with AM broadcasting and supports twice the nominal bandwidth i.e. 18/20 kHz to provide larger transmission capacity. Channel width for radio broadcasting above 30 MHz is 100 kHz.

A subset of MPEG xHE-AAC (Extended High-Efficiency Advanced Audio Coding), a subset of MPEG-4 AAC (Advanced Audio Coding) and MPEG Surround (MPS) are used for source coding. Bit rate available for these coding are in the range from 8 kbit/s (half channels) to 20 kbit/s (standard channels) to up to 72 kbit/s (double channels) and bit rate for broadcasting channels above 30 MHz is in the range of 37 kbit/s to 186 kbit/s.

DRM transmission super frame of 1200 ms. It is divided into three transmission frames of 400 ms. Super frame consists of three logical channels, Main Service Channel (MSC) which consists of payload, Fast Access Channel (FAC) which gives information about channel parameters and Service Description Channel (SDC) which gives information on how to decode the MSC. Before channel coding pseudo random binary code is used to scramble the bits and the unwanted regularity in the transmitted signal. Multilevel coding is used in combination with QAM modulation. Different QAM modulation for different modes is given in the Table 1.

Table 1.
Different modulation scheme for different modes and logical frames

Logical Channels	Mode A, B, C and D	Mode E
MSC	64/16-QAM	16/4-QAM
FAC	16/4-QAM	4-QAM
SDC	4-QAM	4-QAM

Pilot cells which are distributed in time and frequency are used for time, frequency and frame synchronization. These are also used for time tracking and channel estimation.

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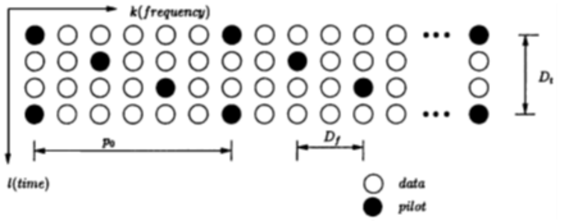

Fig 1: Pilot pattern form DRM mode B

III. IMPLEMENTATION

A. *Hardware and Software Requirement*

Hardware requirements are as follows, Computer, System on Chip (SoC), Test Transmitter, Coaxial cable, UART Cable, Speaker/Headphones and Power Supply to SoC 5v. Software requirements are as follows, GUI, Terminal v1.9 (debugging tool for serial communication), C code editor and C code compiler. Conceptual test setup is shown in the Fig 2.

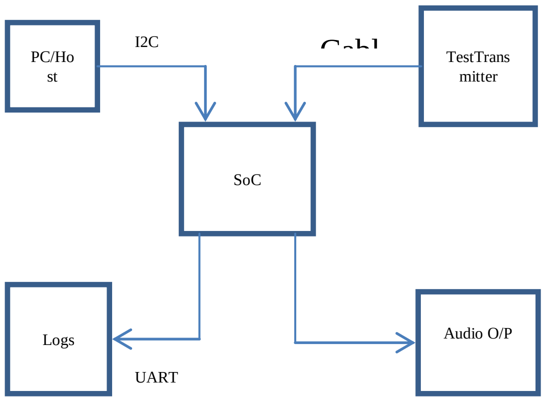

Fig 2: Conceptual Test Setup for DRM transmission and reception

B. *Profiling*

To know time and MCPS consumption from different modules, profiling is done on target broad and flow chart for profiling is as shown in the fig 3.

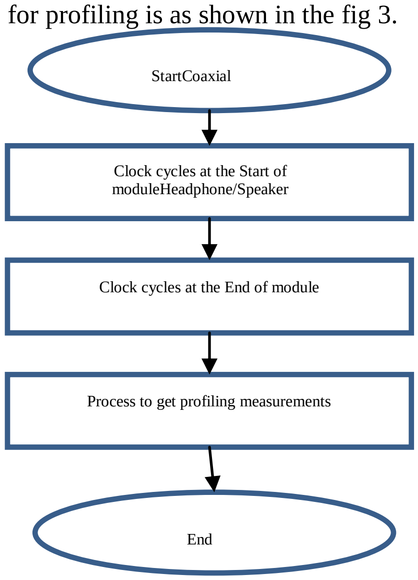

Fig 3: Flow chart for Profiling

C. *Optimization* through Intrinsic

Cycle intensive modules are determined through profiling and performance optimization of cycle intensive modules is carried out using core specific intrinsic. Generic C code is replaced by complier specific intrinsic to reduce no of cycle's consumption and to further reduce cycles consumption by arithmetic computations and loops, loop unrolling is done along with usage of single instruction, multiple data (SIMD) concepts. Flow chart for optimization of cycle intensive modules is as shown in Figure 4.

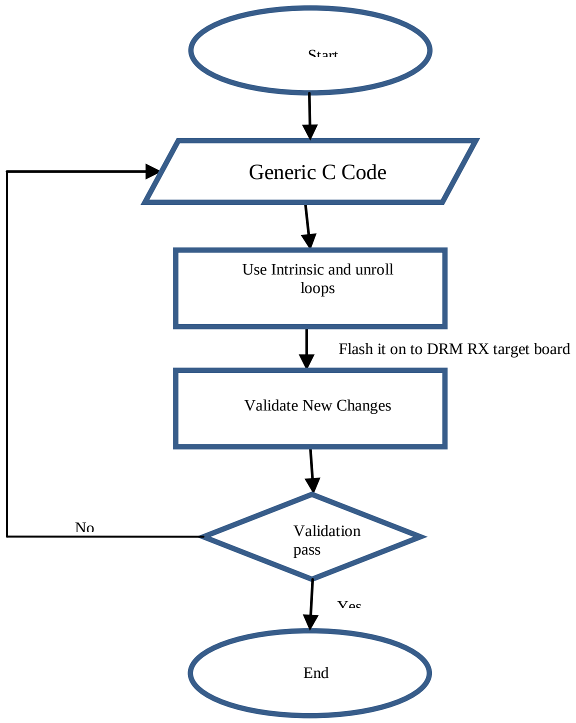

Fig 4: Flow chart for performance optimization of cycle intensive modules

IV. RESULTS

To get profiling measurements test vector is modulated and transmitted from the test transmitter. Signals are transmitted through coaxial cables to the target board. Personal computer or host can be used to send commands to the target board through I2C and SPI interface. Received signals are processed in the SoC and debugging messages are sent to the debugging terminal through UART cable and processed audio output is sent to speaker or to headphone as shown in the Figure 2.

Test vector specifications used for profiling are as follows, audio file format is .wav file, MSC uses 64-QAM modulation, bandwidth is 20kHz, robustness mode is A, radio frequency output at the test transmitter is 95dBuV and target board clock frequency is 265MHz.

In DRM receiver correlation module was consuming 6.54 MCPS, inputs to this module are real 16 bit filter coefficients and complex 16 bit data. Optimization is done

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as shown in the Figure 4 and there is 78.917% (i.e. 1.38 MCPS) reduction in the cycles consumption.

Resample is used to decimate input samples by 2. Inputs to this function are 16 bit complex data, decimation factor is 2 and MCPS consumption before optimization is 23.87 and after optimization MCPS consumption is 2.14. There is 91.03% reduction.

Base band filtering consumes 11.74 MCPS and inputs to this function are 16 bit complex filter coefficients and 16 bit complex data. After optimization it is taking 6.21 MCPS and there is 47.4% reduction in the cycle consumption.

Signal presence tracking is done to check whether signal is present by comparing averaged signal value with the threshold value. Input to this function is 16 bit complex data and there is 49.5% reduction in the MCPS consumption.

Optimised code is flashed onto the DRM receiver target board and Sensitivity test which measures the ability of the receiver to decode weak signals is done and compared with the minimum receiver requirements. There is no change in the sensitivity of the receiver with the optimized code.

V. CONCLUSION

Cycle intensive modules were successfully optimized by using core specific intrinsics. Code is successfully implemented on the target board and heard audio without any artifacts. Sensitivity testing is done for the same implementation, there is no degradation of the sensitivity and it matches with the minimum receiver requirements. Optimization have reduced number of arithmetic computations and it has brought improvement in processing time (speed up improvement) by reducing number of cycles consumption by different modules.

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