ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 5, May 2015

Design, development and Performance Analysis Of 8-point FFT chip using VHDL for OFDM Applications

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Abstract: In several wired and wireless applications high-speed performance is required, which is only possible by using conventional multi-carrier transmission techniques, but this will results in the lowering of spectrum efficiency. So, in such applications the principle of Orthogonal Frequency Division Multiplexing (OFDM) is used. This paper gives the details of the design, development and performance analysis of 8-point FFT algorithms to be used in OFDM systems based on the IEEE 802.11a standard for WLAN. Generally, the inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) operations are used as the modulation and demodulation in the OFDM systems, and the sizes of FFT/IFFT are varied in various applications of OFDM systems. Actually, in the complete architecture of OFDM system, all the mathematical manipulations take place in IFFT & FFT blocks while remaining blocks convert the data from one format to another format. VHDL programming language is used to develop the design and synthesized on Virtex-5 FPGA in Xilinx 14.2 software and Modelsim 10.1 is used for functional simulation.

Keywords: Fast Fourier Transform (FFT), Inverse Fast Fourier Transform (IFFT), Orthogonal Frequency Division Multiplexing (OFDM), Hardware Description Language (HDL).

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) has recently become a key modulation technique for both wired and wireless applications. OFDM is also used as a multiplexing technique. It has been applied in digital terrestrial television broadcasting (DVB) and digital audio broadcasting (DAB) [3]. OFDM has also been adopted for wireless local area network (WLAN) and digital subscriber loop (DSL) applications [4].

OFDM is also known as multicarrier modulation technique which combines a large number of orthogonally selected carriers to transmit a frequency domain stream in parallel form with high data-rate. The multipath channel introduced a problem of inter symbol-interference (ISI) which is significantly reduced in OFDM owing to the relatively low rate parallel data transmission through multiple carriers.

The orthogonal nature of the sub carriers in OFDM allows the spectrum of each sub carrier to overlap without interfering with each other.

This overlapping results in a high spectral efficiency by allowing the sub carrier spectra to be densely packed in the frequency domain. The Multipath immunity and Spectral efficiency are two major features of OFDM.

II. OFDM BLOCK DIAGRAM

The simulation block diagram of OFDM is shown in Fig. 1. OFDM transmission part has serial data as input data which is converted into parallel form and mapped as the input of IFFT in OFDM modulator.

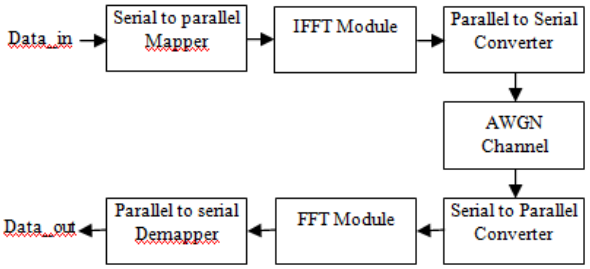

Fig. 1 Functional block diagram of OFDM (data transfer scheme)

The parallel output of OFDM modulator is converted to serial form and passed through AWGN channel. The output of AWGN is also in serial form which again converted to parallel form and given as input to FFT in demodulator. The parallel data of FFT demodulator is demapped as serial output data at receiving end.

III. FAST FOURIER TRANSFORM

To efficiently compute the discrete Fourier Transform (DFT), Fast Fourier Transform algorithm is used. The DFT of sequence x(n) over length N is given by the relation which is a complex valued sequence X(k) [5].

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi nk/N}, Where\ 0 \le k \le N-1 \quad (1)$$

Equation (1) can be represented by the relation

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, Where\ 0 \le k \le N-1 \quad (2)$$

Where W_N represents the complex valued phase factor called as twiddle factor, which is the N^{th} root of unity and given by $W_N = e^{-j2\pi/N}$

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Similarly the equation of IDFT is expressed as

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k) W_N^{-nk}, Where\ 0 \le n \le N-1 \quad (3)$$

Fig. 2 shows the general butterfly structure to compute any DIT FFT value and Fig. 3 shows the DIT FFT flow diagram after reduction in computations.

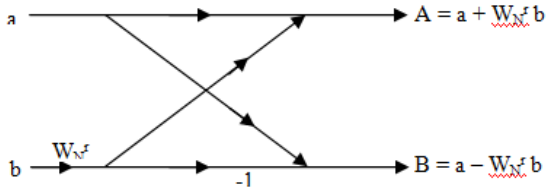

Fig. 2 Generic Butterfly to compute any DIT FFT value

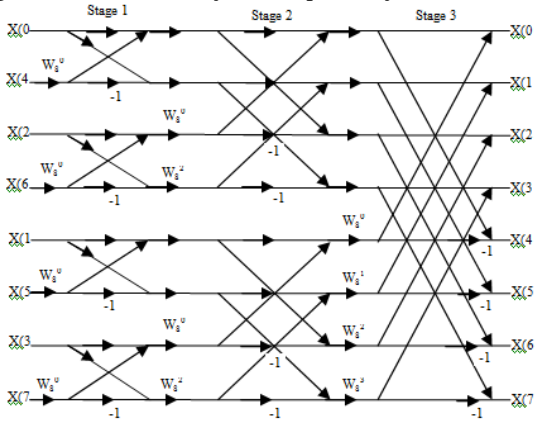

Fig. 3 DIT FFT flow diagram after reduction in computations

The value of twiddle factor is

$$W_N^K = e^{-j\left(\frac{2\pi}{N}\right)k}$$

For N=8

$$W_8^{-0} = e^{-j\left(\frac{2\pi}{N}\right)0} = e^0 = 1$$

$$W_8^{-1} = e^{+j\left(\frac{2\pi}{N}\right)1} = \cos\left(\frac{\pi}{4}\right) + j\sin\left(\frac{\pi}{4}\right) = 0.707 + j\,0.707$$

$$W_8^{-2} = e^{+j\left(\frac{2\pi}{N}\right)2} = \cos\frac{\pi}{2} + j\sin\frac{\pi}{2} = j$$

$$W_8^{-3} = e^{+j\left(\frac{2\pi}{N}\right)3} = \cos\left(\frac{3\pi}{4}\right) + j\sin\left(\frac{3\pi}{4}\right) = -0.707 + j\,0.707$$

IV. XILINX AND MODELSIM OUTPUT OF 8-POINT FFT

The RTL and internal schematic of 8-Point FFT is shown in fig. 4 and 5 and its Modelsim output is shown in fig. 6 and 7. In fig. 6, X(0)…… X(7) represents the input of FFT module and Y(0)….Y(7) represents the output of FFT module. Functional simulation on Modelsim depends on the following step inputs.

Step input 1: Force the value of data_in and X(0) to X(7) and run

Step input 2: The output of FFT are separated in real and imaginary terms because the output of FFT may be a complex number real_Y(0)….. real_Y(7) are the real terms and im_Y(0)…….im_Y(7) are imaginary terms of output.

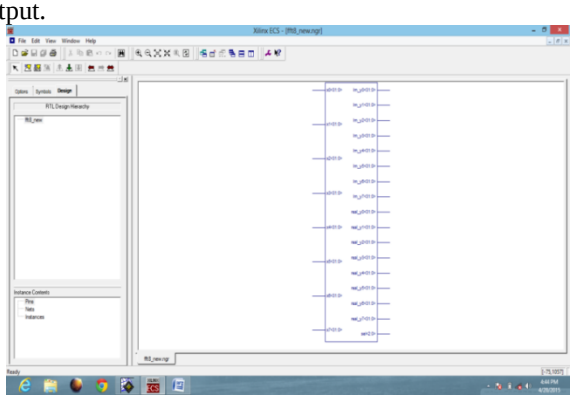

Fig. 4 RTL view or Chip design of 8-Point FFT

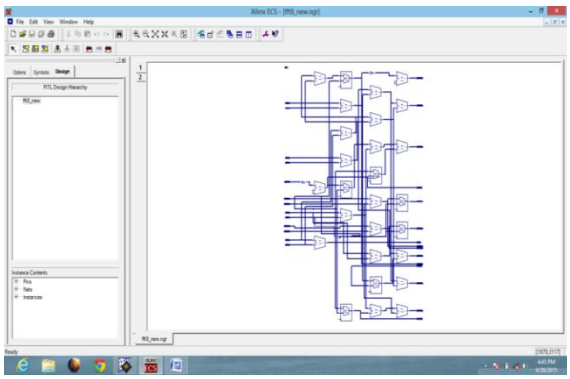

Fig. 5 Internal Schematic of 8-Point FFT

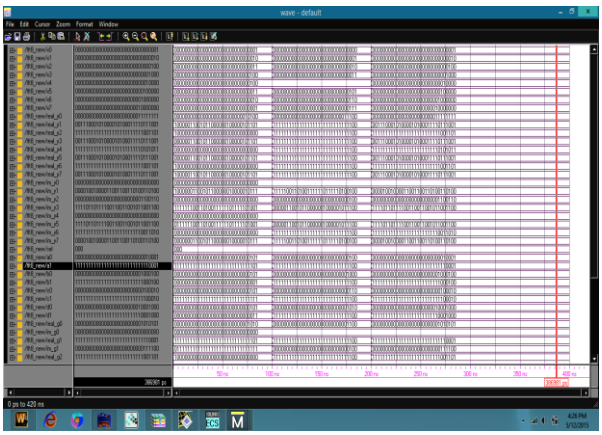

Fig. 6 Modelsim output of 8-point FFT

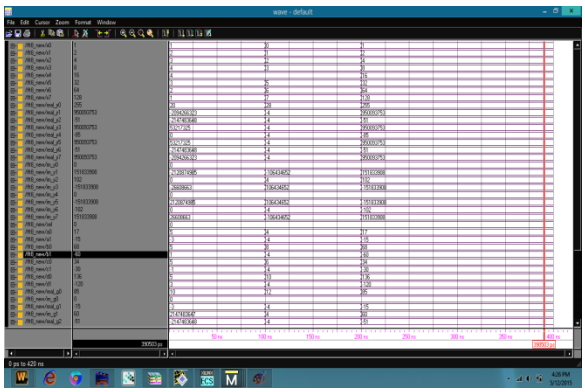

Fig. 7 Modelsim output of 8-point FFT with complex numbers

DOI 10.17148/IJARCCE.2015.45149

ISSN (Online) 2278-1021
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International Journal of Advanced Research in Computer and Communication Engineering
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V. COMPARATIVE ANALYSIS OF 8-POINT FFT WITH REFERENCE PAPER

Table 1 lists the comparative analysis of proposed design with reference paper [6].

Table 1 Comparison of proposed design with ref [6]

Device part	With Ref [6]	Proposed design
Number of Slices	15%	0.35%
Dedicated Logic Registers	15%	0.35%
No of 4 input LUTs	15%	0.35%
DSP Block elements	75%	3%
Path Delay	17.988ns	17.807ns

The comparison charts of the proposed design with ref [6] are shown in Fig. 8 in terms of number of slices, number of 4 input LUTs, logic registers and DSP block elements.

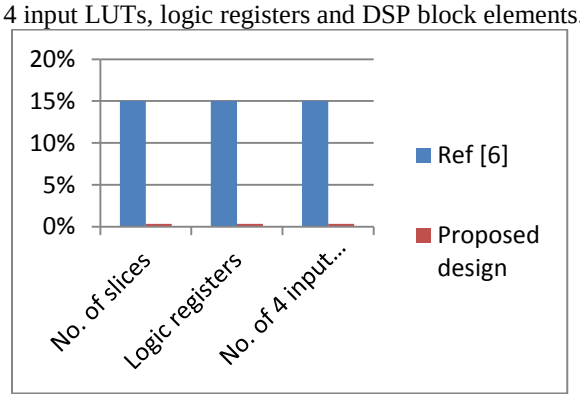

Fig. 8(a) Comparison of the proposed design with ref [6]

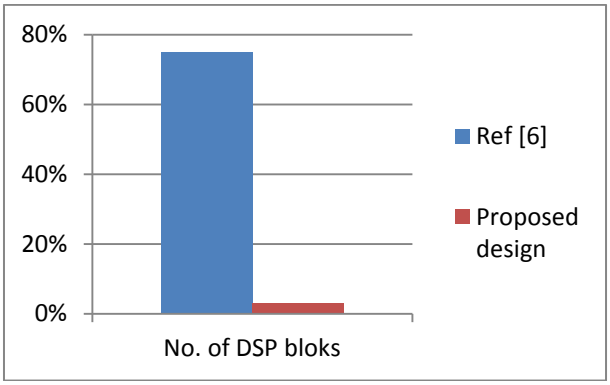

Fig. 8(b) Comparison of the proposed design with ref [6] (Contd.)

The results of our simulation work compared with existing work with reference paper [6]. In our design the number of slices utilization is 0.35%, number of 4 input LUTs utilization is 0.35%, number of registers utilized is 0.35%, number of DSP blocks utilized is 3% and path delay is 17.807ns.

It is also seen that there is 15% unitization of number of slices, 15% utilization of number of LUTs, 15% utilization of number of registers, 75% utilization of number of DSP blocks and path delay is 17.988ns with ref [6]. Our results are the optimized solutions and applicable to extend the implementation of N-point FFT.

VI. CONCLUSION

The hardware chip design and synthesis of 8-point FFT module is done using Xilinx 14.2 software in VHDL programming language. The simulation of results is done on Modelsim 10.1 b student edition successfully. The FFT modules are tested for the various test cases. FFT is utilized in demodulation schemes and data transfer is checked out with FFT/IFFT transceiver used in OFDM and OFDMA applications. The results of our simulation work compared with existing work with reference paper [6] are found optimized. With the help of parallel and pipeline and processing feature the design is applicable to develop upto 'N' point FFT which is applicable to OFDMA applications.

ACKNOWLEDGMENT

The authors would like to express their sincere thanks for the support of BTKIT Dwarahat, Uttarakhand, India to carry out this research work.

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