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Design and Implementation of a Digital Anti-Aliasing Filter using FPGA for Communication Systems

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Abstract: In this paper, we discuss a practical way to synthesize and filter the base band signal in the background of different interference signals resulting from white noise placed within the signal band and sinusoidal interference signal placed out of the signal band. This will be done by a one digital filter of type FIR LPF with Hamming window by using a digital programmable device (Cyclone II EP2C70F896C6 FPGA from ALTERA) placed on education and development board DE2-70. This filter is designed using VHDL language within Quartus II 9.1 design environment. The proposed method depends on designing a set of DDFS to synthesis the base band signal and the various interference signals so the specifications of the base band signal become very closed from the real one, and designing a FIR LPF, so the result is removing all the interference signals and overcoming on the anti-aliasing phenomena by this digital filter. The FIR LPF operation results are studied by using a digital oscilloscope for input and output signals due to different sinusoidal interference signals and white noise in time and frequency domains.

Keywords: Anti-AliasingFilter, FIR LPF, DDFS, FPGA.

I. INTRODUCTION

-In all digital communication devices, a LPF is used to set the spectrum of the base band signal within the frequency range from 0 to 3400Hz to select the signal on the background of different interference signals and remove the anti-aliasing interference phenomena of the processed signal samples.
-In reference [1], D.V.N. Koteswara Raoet al. present a an Anti-Aliasing Low Pass Filter is designed for removal of aliasing.
-In reference [2], Alison de Oliveira Moraeset al. present a digital anti-aliasing LPFfor space telemetry systems design with cut off frequency of 2000Hz and attenuation of 100dB.
-In reference [3], Li-Hua and Xiu-li Zhang presents a half-band filter with cascading method in the random access channel of LTE system down-sampling process using matlab simulation and FPGA implemented scheme.
-In this research, a digital filter of type FIR LPF is designed by using VHDL language with order of 1500, and cut off frequency of 3400Hz, also the base band signal simulator with frequency of 2000Hz and interference signal with frequencies of 3500Hz, 3900Hz, were designed.
-The serial using of these filters for high order affects on the processing signal structure, so the signal processing operation may be distorted and different from the real case of the signal.
-The proposed filter achieves the signal filtering under different interference signals effect, these signals differ in frequency and with signal band width within range (from 0 to 3400Hz), a filter order of 1500, attenuation factor of 60 dB for various interference signals. Also, the filter has a linear phase response, so this reduces the filtered signal distortions and makes the processing operation closed to the real case.

II. THE USED TOOLS AND SOFTWARE

In this research, the following tools and software are used:
-FPGA chips with highly accuracy, speed, and level specifications placed on education and development boards DE2-70 [4].
-DDFS which is considered as highly accuracy techniques in frequency synthesizing domain and they were designed on FPGA chips.
-Digital FIR filters of highly accuracy specifications in filtering and stability and linear phase response.
-VHDL programming language with Quartus II 9.1 design environment.
-MATLAB11 programming environment for digital filter designing and filter coefficients computing.
-GDS-1052U digital oscilloscope with Free Wave program to take the results.
-PC computer for designing and injecting the design in the chip.

III.THE BLOCK DIAGRAM OF THE PRACTICAL DESIGN

The block diagram of the practical design shown in Fig.1a [5] and the block diagram of the search and study system with Quartus II 9.1 design environment shown in Fig.1b, this diagram is carried out on digital chip using Cyclone II EP2C70F896C6 FPGA from ALTERA placed on education and development board DE2-70, and it consists

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of: a-Clock pulses generator F_{CLK}=50MHz to synthesize clock and sampling pulses for all designing components.
b-The base band signal simulator which consists of the following parts:
-Direct digital frequency Synthesizer DDFS_SIGNAL to synthesize the base band signal which is closed to real one with band width within the range from 0 to 3400Hz.
-DDFS_F_{sam} to synthesize sampling pulses with frequency of F_{sam}=50 KHz.
-DDFS_INTERFERENCE to synthesize the sinusoidal interference signals with frequencies of F_{sin1}=3500Hz, F_{sin2}=3900Hz.
-Digital pseudo noise generator DPNG to synthesize Gaussian white noise signal with band of 3400Hz within the base band signal band.
-Two DAC of 10 bits to convert the signal from digital to analog form before (DAC1) and after filtering (DAC2).

C-Digital filter of FIR LPF type with time convolution algorithm of 1500 order and bandwidth from 0 to 3400Hz.
d-PC computer to link DE2-70 board via USB and inject

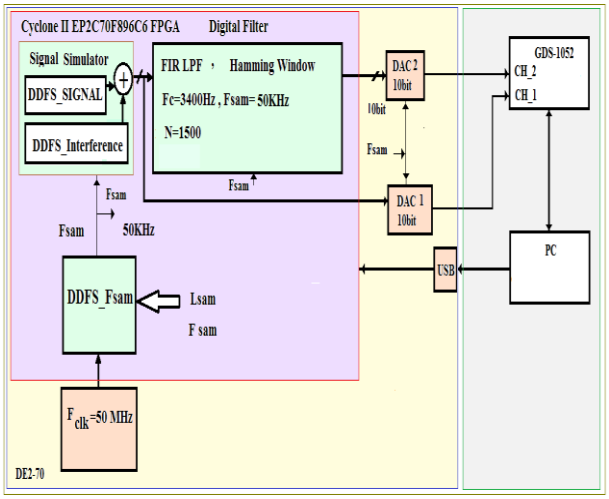

Fig.1a The diagram of studying and searching procedure of the base band signal

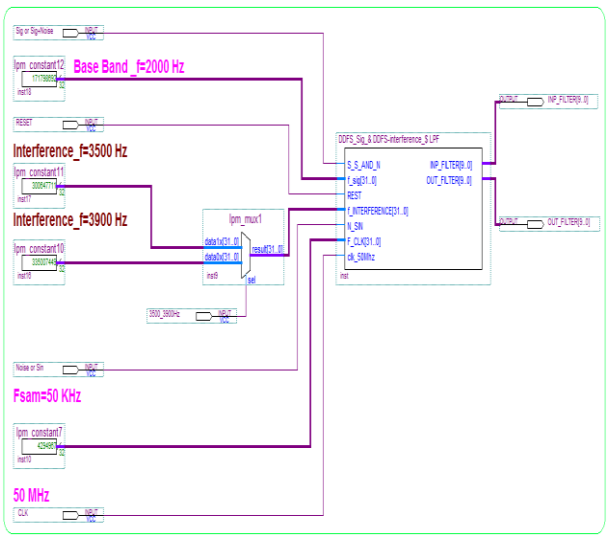

Fig.1b The block diagram of the search and study system with Quartus II 9.1 design environment

the design in the Cyclone II EP2C70F896C6 FPGA chip [4].
e-Digital oscilloscope GDS-1052U connected to PC via USB to show the input and output signals of the digital filters in time domain due to various interference signals, where (ON CH_1: Before Filtering, ON CH2 After Filtering).
This design is carried out for the Base Band signal and digital filter of type FIR LPF with specifications identified later.

IV. THE BASE BAND SIGNAL SIMULATOR

This simulator contains:

a-The base band signal generation algorithm (DDFS_SIGNAL)

To generate a base band signal, we use a DDFS_SIGNAL according to the diagram shown in Fig.2 which consists of the following parts:
-Phase Accumulator (PA) to synthesize the step of accessing address to the stored signal samples memory (ROM0) according to the frequency code (Lsig).
-ROM0 memory which contains the base band signal samples during one of its periods.
-Samples pulses generator (as a clock pulses) F_{sam} for reading from ROM0, the stored signal samples at every sampling pulse.
-The synthesizer operating frequency value, frequency code, and frequency accuracy are computed by the following mathematical relations [6]:

$$F_{Sig} = \frac{F_{sam}}{(2^n / L_{Sig})} = \frac{F_{sam}.L_{Sig}}{2^n}$$

$$L_{Sig} = \frac{2^n.F_{Sig}}{F_{sam}} \qquad (1)$$

$$\text{For } L_{Sig} = 1 \Rightarrow F_{min} = \frac{F_{sam}}{2^n}$$

Where:
F_{Sig}: output frequency, n: the number of phase accumulator bits, L_{Sig}: frequency code for synthesizer, F_{sam}: samples frequency (as a clock pulses), F_{min}: frequency accuracy.

Direct Digital frequency synthesizer specifications for the base band signal:
-F_{sam}=50KHz (is considered as a samples frequency).
-The number of phase accumulator bits 32 bits.
-The frequency accuracy for F_{sam}=50KHz:

$$F_{min} = \frac{F_{sam}}{2^n} = \frac{50000.10^6}{2^{32}} = 11.64 \quad \mu Hz$$

-Memory ROM0 contains 2^{14}=16384 words, the word length is 10 bits to store the samples of the base band signal.
-The base band signal samples are computed by programming environment MATLAB11 according to the following relation [7]:

X(i)=512+floor(511*sin(2*pi*i/16384)) ,
i=1,….., 16384 (2)
and stored in ROM0 memory for frequency synthesizer,

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this signal is shown in the Fig.3 which results from applying the previous relation.

-The frequency of the base band signal equals to 2000Hz so the frequency code is:

$$\text{for } F_{sam} = 50\ KHz \Rightarrow$$

$$L_{Sig} = \frac{2^{n}.F_{Sig}}{F_{sam}} = \frac{2^{32} * 2}{50} = 171798692$$

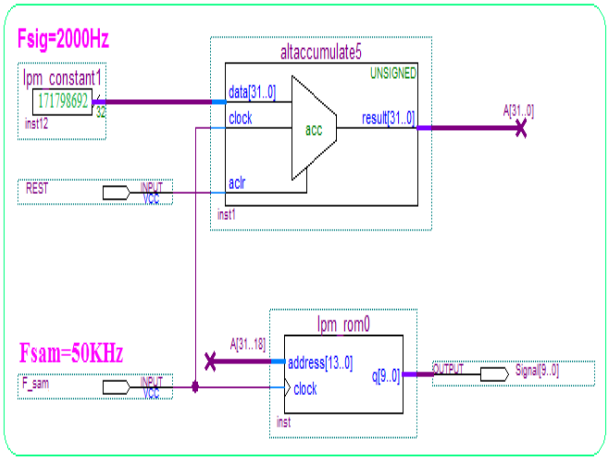

Fig.2 The diagram of direct digital frequency synthesizer of the base band signal

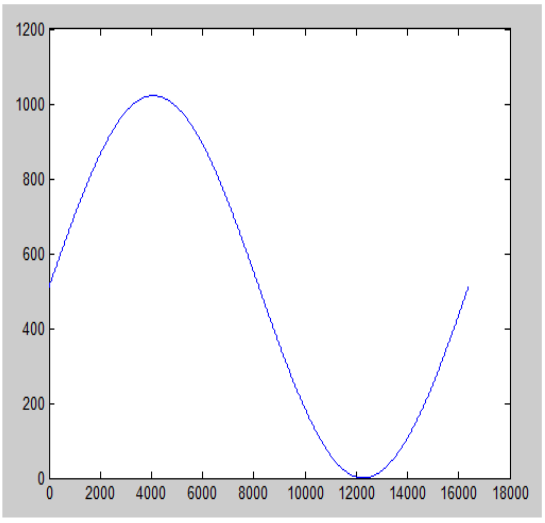

Fig.3 The base band signal samples which computed within MATLAB11 environment

The base band signal specifications:

-The frequency range of the base band signal is $(\Delta f_{Sig} = From \quad 0 \text{ to } 3400 \quad Hz)$

-The processing on the base band signal frequency of F_{Sig}=2000Hz.

-Sampling frequencies of all components: $F_{sam} = 50\ KHz \quad , T_{sam} = 0.02\ ms$.

-Samples number: M=1501.

-The processing word length of the sampling base band signal: Signed 10 bits.

-SNR_{INP}=1/1 for sinusoidal interference signals, SNR_{INP}=4/1 for white noise interference signals.

b-The algorithm of sinusoidal interference signals generation (DDFS_INTERFERENCE)

The sinusoidal interference signals will be generated as follows:

-The first is sinusoidal signal with frequency of 3500Hz and has amplitude equals to 100% from the base band signal amplitude and exists within the stop band and considered as the first interference signal.

-The second is sinusoidal signal with frequency of 3900Hz and has amplitude equals to 100% from the base band signal amplitude and exists within the stop band and considered as the second interference signal.

-To generate these sinusoidal signals, we use a DDFS according to the diagram shown in Fig.4 which consists of the following parts:

-Phase accumulator PA to form address step to access the memory of stored signal samples ROM1 according to frequency code (L_{sin}).

-ROM1 memory which contains the sinusoidal signal samples through one time period for it.

-Sampling pulses generator F_{sam} to read the stored signal samples from ROM1 memory with every sample pulse.

DDFS specifications of sinusoidal interference signal

-The frequency value of the synthesizer operating is computed due to equation (1) as in the base band signal frequency synthesizer.

-The sampling pulses frequency is 50KHz (clock pulses).

-The bits number of the phase accumulator is 32 bits.

-Frequency accuracy [6]:

$$F_{\min} = \frac{F_{sam}}{2^{n}} = \frac{50000.10^{6}}{2^{32}} = 11.64 \quad \mu Hz$$

-ROM1 memory contains 2^{14}=16384 words, the word length is 10 bits to store the sinusoidal signal samples.

-The sinusoidal signal samples are computed in MATLAB11 programming environment according to the relation (2), and stored in ROM1 memory for the frequency synthesizer, this signal is shown in Fig. 5 with frequencies of 3500Hz and 3900Hz in time and frequency domains.

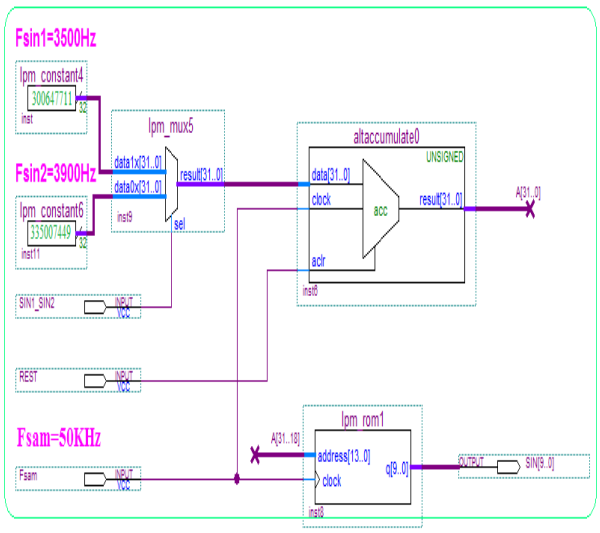

Fig. 4 The functional diagram of the DDFS_INTERFERENCE of the interference signals

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-The sinusoidal signal with frequency of 3500Hz has a frequency code equals to:

$$L_{\sin 1} = \frac{2^n . F_{\sin 1}}{F_{sam}} = \frac{2^{32} * 3500}{50000} = 300647711$$

The sinusoidal signal with frequency of 3900Hz has a frequency code equals to: -

$$L_{\sin 2} = \frac{2^n . F_{\sin 2}}{F_{sam}} = \frac{2^{32} * 3900}{50000} = 335007449$$

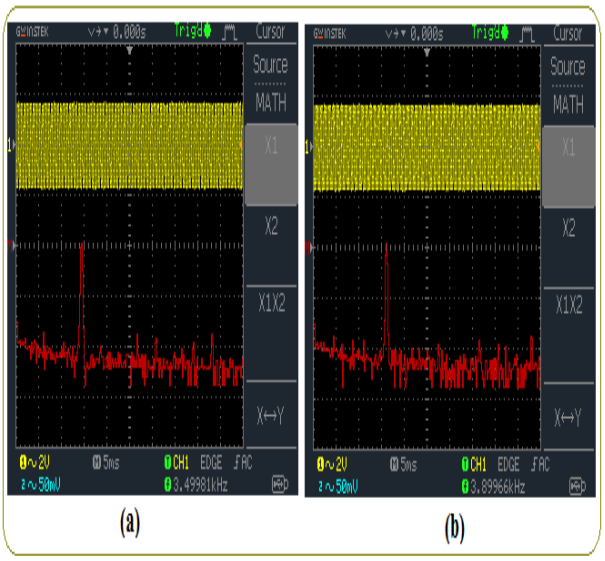

Fig. 5 the sinusoidal signal on the oscilloscope screen and spectrum analyzer with frequencies of 3500Hz and 3900Hz

c-The algorithm of noise interference signal generation (DPNG)

This signal is of white noise type and has amplitude equals to 25% from the base band signal amplitude and exists within the filter pass bands and is considered as the fifth interference signal.

To generate the white noise signal, a digital pseudo noise generator DPNG is used, which consists of a shift register of k=40 bits and clock pulses of frequency equals to sampling frequency of 50KHz with maximum periodic time for the generated series [8]:

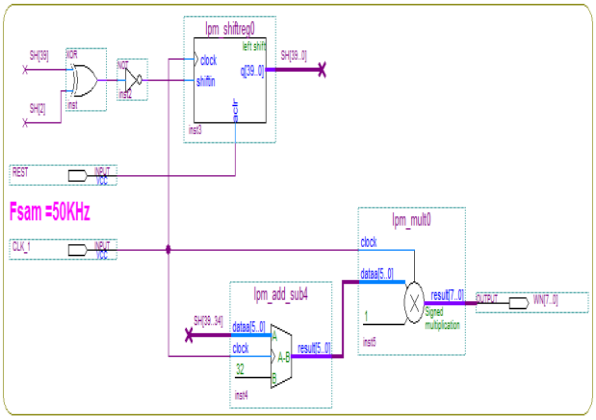

Fig. 6 The digital pseudo noise generator (DPNG) diagram

$$T = (2^k - 1) * T_{sam} \qquad (3)$$

For $k = 40 \Rightarrow$

$$T = \frac{(2^{40} - 1)}{(50000 * 3600 * 24 * 365)} \approx 0.7 \quad \text{Year}$$

Where k the number of shift register bits.

According to the diagram shown in Fig. 6, which consists of the following parts [11]:

-Shift register of 40 bits and clock pulses with sampling frequency of 50 KHz.

-Feedback circuit by using XOR gate and NOT gate.

The Fig. 7 shows the formed noise signal.

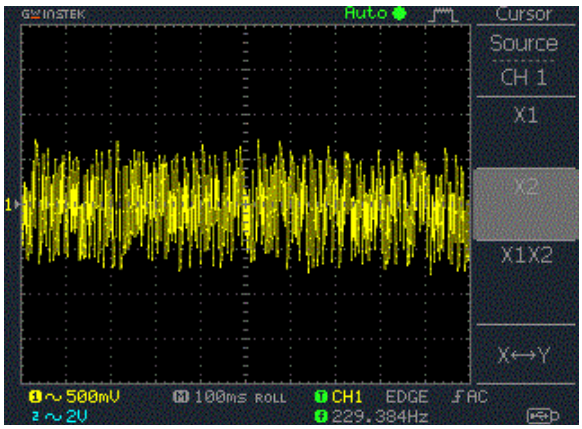

Fig. 7 The white noise signal of F_{sam}=50 KHz on the oscilloscope screen

d-The algorithm of samples pulses generation (DDFS_F_{sam})

To generate samples pulses, we use direct digital frequency synthesizer DDFS_F_{sam}according to the diagram shown in Fig. 8 which consists of the following parts:

- Clock pulses generator with F_{CLK}=50MHz.

-Phase accumulator PA to form the samples pulses with frequency computed by the following relation [6]:

$$F_{sam} = \frac{F_{CLK}}{(2^n / L_{sam})} = \frac{F_{CLK} . L_{sam}}{2^n}$$

$$L_{sam} = \frac{2^n . F_{sam}}{F_{CLK}}$$

Where: F_{sam} samples frequency, n the bits number of the PA, L_{sam} samples frequency code of the synthesizer, F_{CLK} clock pulses frequency. Fig. 9 shows the samples pulses of frequency 50KHz taken from digital oscilloscope screen.

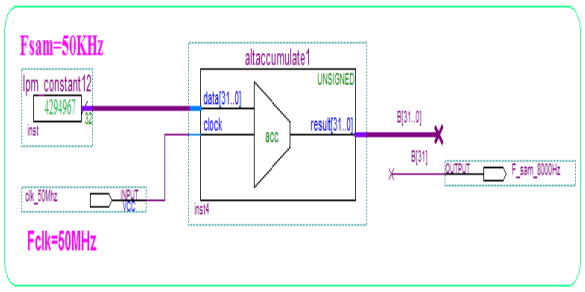

Fig.8 The block diagram of DDFS_F_{sam} of sampling signals

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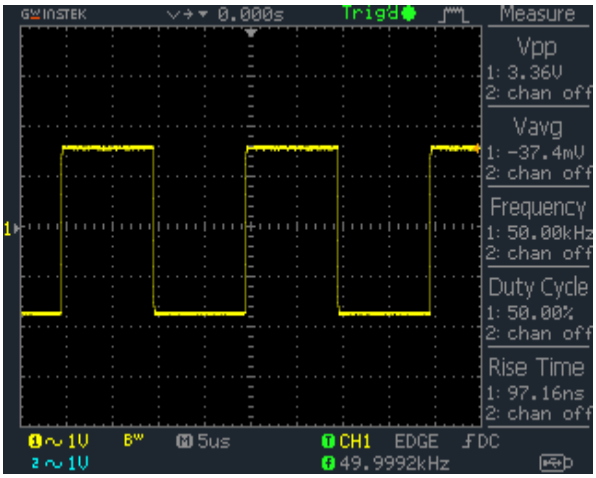

Fig. 9 Samples pulses with frequency of 50KHz on the oscilloscope screen

DDFS_F_{sam} specifications

-Clock pulses frequency F_{CLK} =50MHz.
-The bits number of phase accumulator is 32 bits.
-Frequency accuracy:

$$F_{\min} = \frac{F_{CLK}}{2^n} = \frac{50.10^9}{2^{32}} = 11.64 \quad mHz$$

-The samples pulses with frequency of 50 KHz have a frequency code equals to:

$$L_{sam} = \frac{2^n . F_{sam}}{F_{CLK}} = \frac{2^{32} * 50}{50 * 10^3} = 4294967$$

V. FILTERING ALGORITHM

The FIR filter output signal can be represented according to the following convolution relationship [9]:

$$y(n) = h(n) * x(n) = \sum_{m=0}^{M-1} h(m) . x(n-m) \quad (4)$$

Where: x(n) input signal samples in digital form,
m : the samples number of impulse response of the filter,
n: the samples number of input and output signal ,
h(n):the impulse response samples for digital filter and it is given to LPF according to the following relationship [9]:

$$h(0) = 2\frac{F_{CLPF}}{F_{sam}} \quad , \text{For } n = 0$$

$$h(n) = \frac{1}{\pi n}\sin(2\pi n \frac{F_{CLPF}}{F_{sam}}) \quad , \text{For } n \neq 0 \quad (5)$$

Where:

$$-\left(\frac{M-1}{2}\right) \leq n \leq +\left(\frac{M-1}{2}\right) \quad (6)$$

F_{CLPF} :cut off frequency of the LPF.
F_{sam} : sampling frequency of the input signal.
In this research, a digital filter was designed of FIR LPF type of 1500 order to get -60dB attenuation out of the pass band and 0.9Hz theoretic transition band width, the magnitude response for the proposed filter is shown in the Fig. 10 which consists of the following bands:

-Filter stop band is: (3400Hz… 25000Hz).
-Filter pass band is: (0,…, 3400Hz)
-This filter allows passing of the base band signal within the band (0,…, 3400Hz) and increasing the attenuation factor of the interference signals within the stop band by factor of -60 dB.
-The base band signal and the interference one are given to the digital filter and recorded the input and output signals for different values of interference signals frequency.
-The proposed filter algorithm was tested by the previous the base band signal simulator.

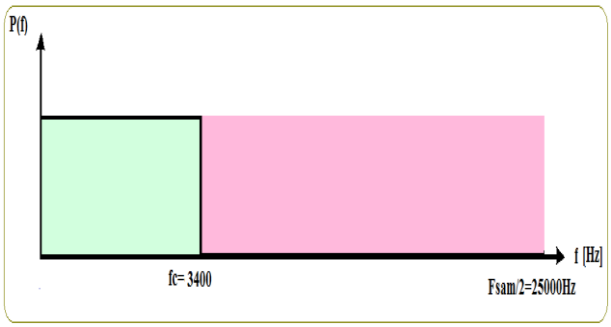

Fig. 10 Stop and pass bands of a digital filter of type FIR LPF

The coefficients of the designed multiband digital filter h(n), are computed in MATLAB11 programming environment and converted to signed values with length 10 bits and used in the filter design program by VHDL language where the digital convolution algorithm of the FIR LPF is implemented for input signal and impulse response samples of length M=1501 according to the diagram shown in Fig. 11 , where (Z^{-1}) represents a digital delay line of length 10bits and a delay time equal to sampling pluses period T_{sam}.

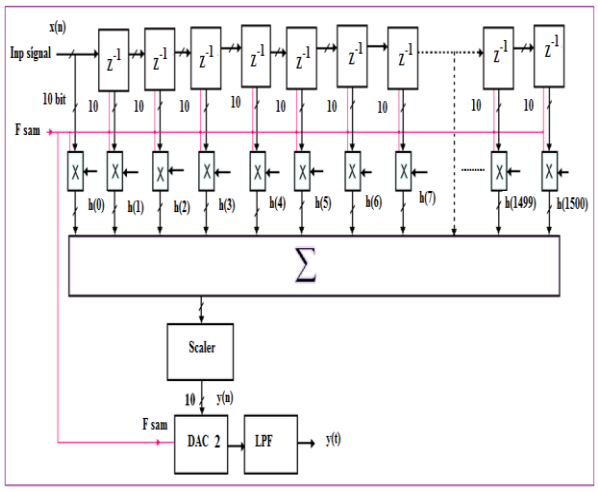

Fig. 11 Time convolution $\{y(n)\}$ for samples of input signal and impulse response of length M=1501

This filter is designed by VHDL[10]with Quartus II 9.1 programming environment according to the diagram shown in Fig.12 , Fig.13a shows the specifications of designed filter (type, order, pass-bands ,stop-bands, sampling frequency) and the magnitude and phase

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responses of this filter in MATLAB11 programming environment ,a typical impulse response FIR LPF with Hamming window for N=1500 , is depicted as Fig.13b below and a typical Hamming window function for N=1500 is depicted as Fig.13c below.

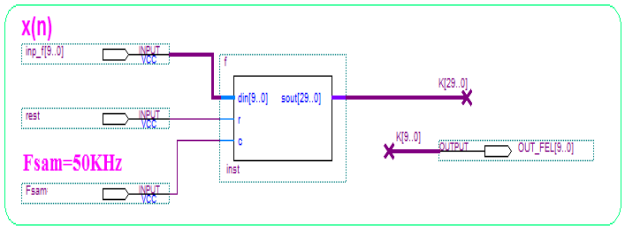

Fig.12 Digital FIR LPF diagram

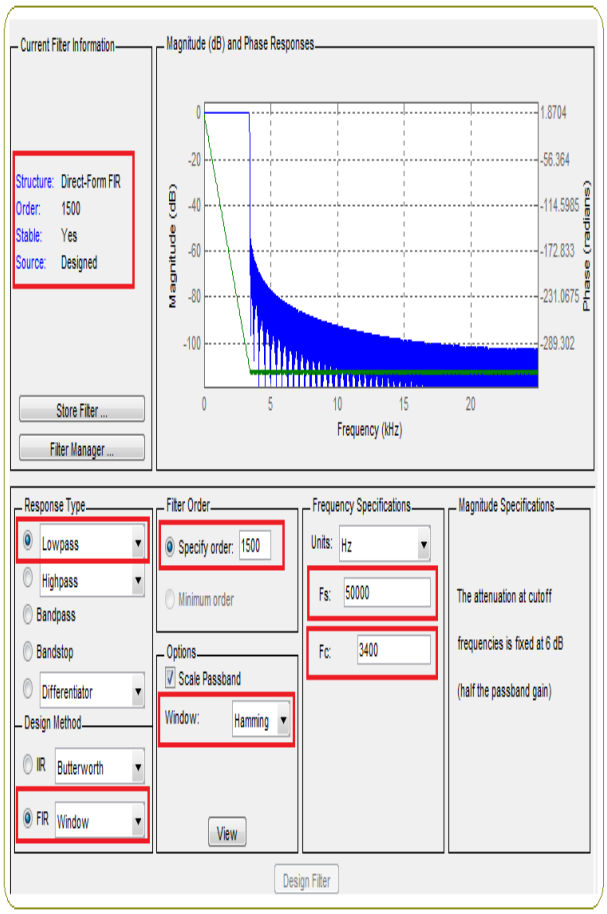

Fig.13a Specifications, magnitude and phase responses of FIR LPF

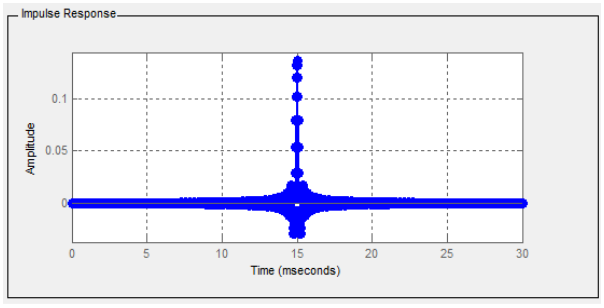

Fig. 13b Impulse response FIR LPF with Hamming window for N=1500

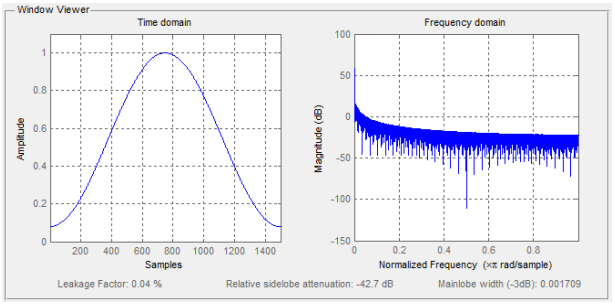

Fig. 13c Typical Hamming window function for N=1500

By the result a digital FIR LPF is obtained with the following specifications:

-Coefficients word length: signed of 10bits.

-The number of used digital multipliers: 1501 multipliers of 10×10bits.

-The number of the parallel shift registers (SR) of 10bits length is 1500SR (Z^{-1}).

-One adder of 20bits with 1501 inputs and one output of 30bits.

-The cut off frequencies of the filter are: $F_{CLPF} = 3400 \ Hz$

-Filter order is : N=M-1=1500.

-The filter samples frequency is: 50 KHz.

-Stop-band attenuation factor is: -60dB.

-Maximum theoretic transition band width is: 0.9Hz.

-Processing speed is 1500 multiplying, adding, shifting and conversion operations through 0.02 ms which equal 1500x50000=75000000 (75 million) operations per second by using parallel processing (adding, shifting, multiplying, and dividing 1500 digital samples with 10-bits length through one period for sampling pulses, that is, 0.02 ms), this equivalent to 75MHz processor clock frequency, so the processing is done simultaneously on-line, this speed may be doubled at serial connection of several filters (for two filter the processing speed becomes 150MHz).

-The possibility of developing this algorithm through serial connection for several filters in order to get high order of attenuation and low transition band width.

VI. THE PRACTICAL RESULTS

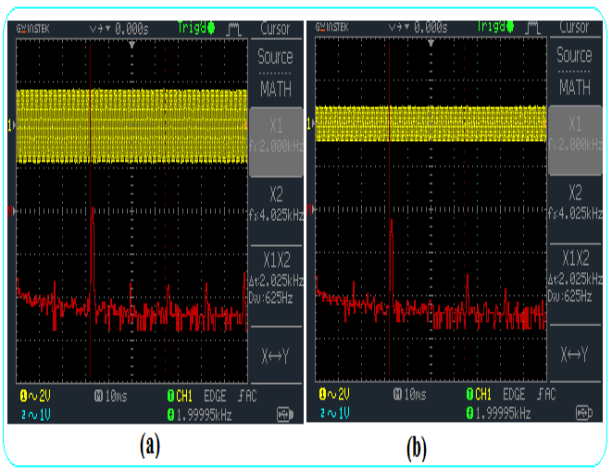

Fig. 14 Input (a) and output (b) signals of the digital FIR LPF in frequency domain without noise

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The practical design results of the filter were taken by digital oscilloscope of type GDS-1052U at different cases of interference signals effecting in time and frequency domains for the base band signal after and before filtering. Fig.14a shows the base band signal which is synthesized by DDFS_SIGNAL without the interference of signal effect before filtering, Fig14b shows the base band signal after filtering by digital FIR LPF in frequency domain, and this ensures that the filter must not distort the signal after filtering because it has a linear phase response.

Fig. 15a shows the base band signal which is under the white noise effect placed within the pass band of the filter which results from different sources (sampling, ,internal noise of the amplifiers, and different electronic elements in digital communication devices) and with SNR_{INP}=4/1 before filtering ,Fig.15b shows the base band signal after filtering by a digital FIR LPF in frequency domain, where the filter is considered as an average value filter where we note that the quantity of the interference signal attenuation is 5dB.

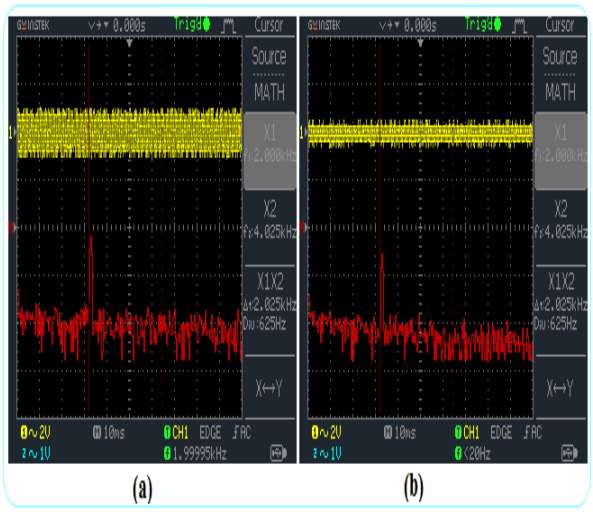

Fig. 15 Input and output signals of the digital FIR LPF in frequency domain in in case of white noise interference signal

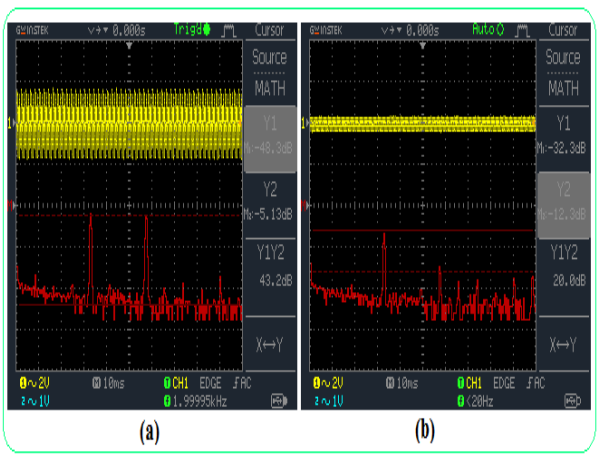

Fig. 16 Input (a) and output (b) signals of the digital filter in frequency domain in case of interference signal with frequency of 3500Hz

Fig. 16.a shows the base band signal which is under the sinusoidal interference signal effect placed within the pass band of the filter with frequency of 3500 Hz to check the stop band (3400Hz,…, 25000Hz), which results from different external sources and with SNR_{INP}=1/1 before filtering and Fig.16b shows the base band signal after filtering by digital filter, where the filter is considered as a LPF filter in frequency domain where we note that the quantity of the interference signal attenuation is 20dB.

Fig. 17a shows the base band signal which is under the sinusoidal interference signal effect placed within the pass band of the filter with frequency of 3900 Hz to check the stop band (3400Hz,…, 25000Hz), which results from different external sources and with SNR_{INP}=1/1 before filtering and Fig. 17b shows the base band signal after filtering by digital filter, where the filter is considered as a LPF filter in frequency domain where we note that the quantity of the interference signal attenuation is 60dB.

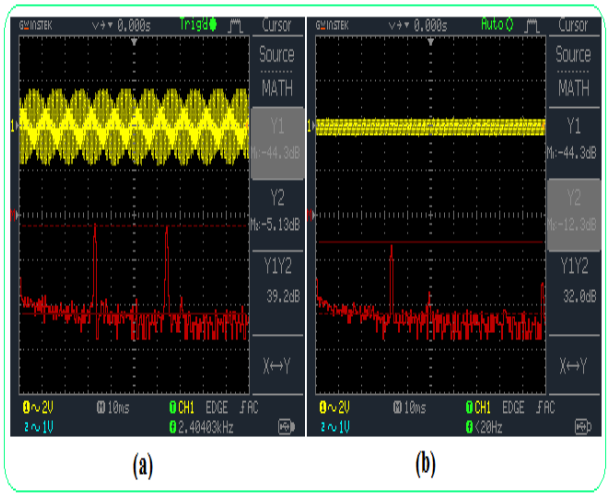

Fig. 17 Input signals (a) and output signal (b) of the digital filter in frequency domain in case of interference signal with frequency of 3900Hz.

VII. CONCLUSION

-Depending on the previous practical results, the digital FIR LPF successfully designed removes the various interference signals with keeping on the amplitude and phase specifications of the base band signal although they affect instantly together on different frequencies and with attenuation factor which reach to 60 dB, also the filter specifications can be improved through increasing, the filter order and this can be achieved by using FPGA chips which have large material resources, accuracy and high quality in performance.

-In this research, the base band signal simulator, different types of frequency synthesizers of interference signals, and the digital FIR LPF are successfully designed. The practical experiments ensure that the possibility of using this type of filters in the digital communication devices.

-To develop this research in the future, the real base band signal can be taken from a real source (from microphone after amplifying and samples taking) and implement the filtering by using the proposed filter.

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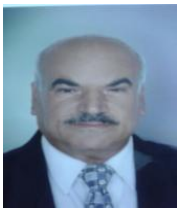

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