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Analysis and Comparison of Various Sense Amplifier Topologies for SRAM

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Abstract: Sense Amplifier are one of the most crucial circuits in the field of CMOS memories. Memory access time and overall memory power dissipation both are resultant by their performances. The existing Current Mode Sense Amplifier has ability to quickly to amplify a small differential signal Bit Lines (BLs) and Data Lines (DLs) to the full CMOS logic level without requiring a large input voltage swing. Here Analysis and Comparison done using 45nm CMOS technology shows Sensing Speed, Reliability, Power Consumption can be improved to a considerable extent. Power dissipation is improved.

Keywords: Current Controlled SA, Cache Memory, Low Power, Sense Amplifier.

I. INTRODUCTION

SRAM based cache is one of the crucial elements of VLSI designs systems for bridging divergence between CPU performance and DRAM based memory. These cache are responsible directly proportional to the speed of data flow. To have high clock rates processor must be fed with instructions and negligible delay data. These arise as the never ending market demands. The Sense Amplifier is one of the most important components in the circuitry of memory devices. Many types of Sense Amplifier have been implemented but Latch type SA is always prioritized as it has high sensing speed and low power consumption. Sense Amplifier strongly influences the memory access time. It amplify the small Differential signal on the bit lines without creating a high voltage swing. This ability makes Sense Amplifier widely used as one of the ways to reduce both sensing delay and power consumption.

This paper presents analysis and comparison of Current Mode Sense Amplifier of various designs to the previously existing designs, showing comparison which proves time and power reduction. Designs are simulated and graphically presented in comparison with widely used SA topologies.

Section I- Introduction is followed by Section II- showing Sense Amplifier designs. Section- III shows Simulation of various designs and their comparison. Section- IV shows the conclusion part while at last lists the references. Simulation results for Sense Amplifier are obtained from Cadence Virtuoso version 6.5.1 tool presented using 45nm CMOS technology.

II. SENSE AMPLIFIER DESIGNS

Sense Amplifier is one of the remarkable implementation in the world of CMOS technology. Bit line sensing, read speed, power factors are marked by the choice of designs. The fundamental functioning of Sense Amplifier states as to amplify a small differential voltage generated by read access cell to the full swing digital output signal which ultimately reduces time required for read operation. Current mode Sense Amplifier detects current difference between bitlines and checks whether memory cell contains '0' or '1'. Measurement of Read current and transfer to output circuit is done by these only. VLSI's field and battery backed up systems are limited by the power problem. A large portion of the total power is consumed by on chip memories and interface circuits.

A. Current Conveyor Based Sense Amplifier

There are four identical pMOS transistors in the conveyor based circuit. These are enabled by low level triggering of column select (CS) signal low. All the four pMOS transistors which are connected in feedback structure operate in saturation mode during the read cycles. It is due to the assumed fact that the complimentary bit lines (BL and BL') are precharged to VDD. The source-to-drain currents are only dependent on their gate-to-source voltages because the transistors are operating in saturation region. Due to this, voltage at the bit line terminals (VBL and VBL') is the same and equal to (V1 +V2). The discharging of the highly capacitive bit-lines has little impact on the circuit and current conveyor therefore has the ability to convey the differential current from the bit-lines to the data-line without any delay.

As a result there is a drastic improvement in the sensing speed as well as the power consumption is also reduced when compared to the conventional voltage mode designs in which large voltage difference must be developed between the bit-lines. This basic structure of current conveyor has received several improvements which mainly focus on the use of current mirrors for improved current drivability of current conveyor.

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In this paper new current mode sense amplifier will be compared with the high-speed design which consists of four additional nMOS transistors shown in Figure. 1. The output currents I1 and I2 to the data-lines are intensified by the two current mirrors formed by nMOS devices. This design will be used as the benchmark to evaluate the performance of other current mode sense amplifiers.

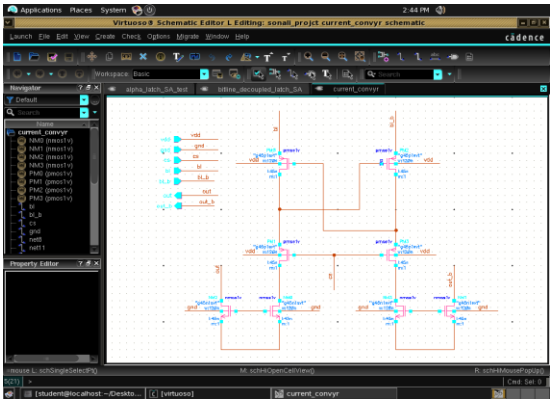

Figure1- Current-Conveyor-Based Sense Amplifier

B. Alpha-Latch Sense Amplifier

Figure 2 depicts the alpha latch. As soon as the enable signal (EN) activates the sense amplifier, a differential trans conductance in N3 and N4 by the differential input from the complementary bit-lines. Due to this, voltage and current differences will appear at the drains of N3 and N4, i.e., the sources of N1 and N2. Since the CS signal turns off N6, the flip-flop structure will latch and full swing voltages will be available at nodes A and B, turning one of the transistors N7 and N8 ON while the other is OFF. The nMOS transistor N5 is used to turn the amplifier off during standby thus saves power. During standby, EN' is kept high to turn P3 and P4 off. When the circuit is under operation only one current will flow to the data-lines to the output of SRAM, this is due to the fact that during operation, both P3 and P4 are turned on but one of N7 and N8 is turned off.

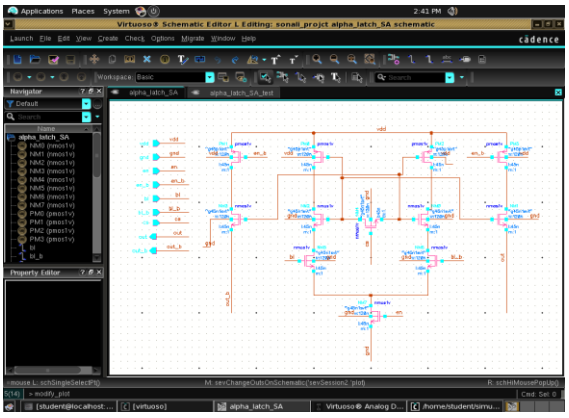

Figure2- Alpha-Latch Sense Amplifier

C. Bit line Decoupled Sense Amplifier

Figure 3 shows the decoupled-latch which consists of six nMOS and two pMOS transistors. Here also N3 is used to save power which is quite similar to the alpha-latch circuit. The property of nMOS occupying smaller area as compared to pMOS for same current strengths is utilised here, so a tail nMOS device is used in Figure.2 and Figure 3.

Another reason for using a tail nMOS device is because the bit lines BLs are precharged to VDD. It is in contrast with read only cycle memory systems design in Figure 3 where a tail pMOS device must be used because DL and DL' are pre-charged to ground. Two decoupled devices, i.e., P3 and P4 are used at the input ports of the amplifier for these heavily loaded bit lines.

Once the bit-line differential signal is induced at nodes C and D, the latch is enabled by turning off N4 but turning on N3. Concurrently, P3 and P4 are turned off to decouple the bit-lines from the high- swing output nodes.

The sensing delay and power consumption are significantly reduced because the impact of the bit-line capacitances on the switching activity is reduced by P3 and P4. Figure. 3 shows a pair of nMOS transistors transfers the full swing voltage at nodes C and D to the data line differential voltage. This is in close similarity to the alpha latch design.

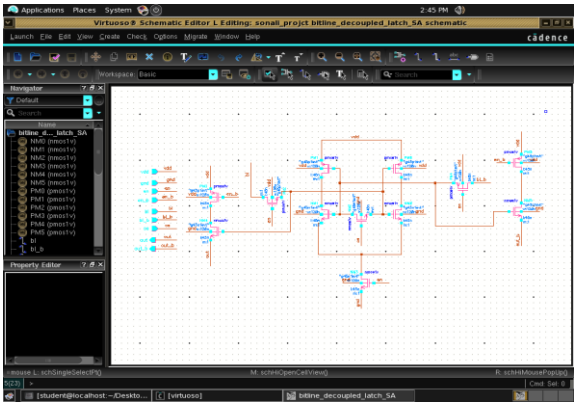

Figure3- Bit line Decoupled Sense Amplifier

III. PERFORMANCE COMPARISON AND ANALYSIS

The various designs of Sense Amplifier have been optimized and simulated using Cadence Virtuoso Spectre version 6.5.1 based on 45 nm CMOS technology.

Standard 6T SRAM cell have been used as instance with capacitance at bit line and bit line_bar while simulating. Each memory cell was alternatively activated by corresponding row select and column select and design is enabled by CS control signal.

Furthermore their average power consumption, total power dissipation, sensing delay with time have been measured over a range of C_{BL} and C_{BL_B} which lies from 100pf to 500pf.

The various existing designs simulated with instance cell have been shown below.

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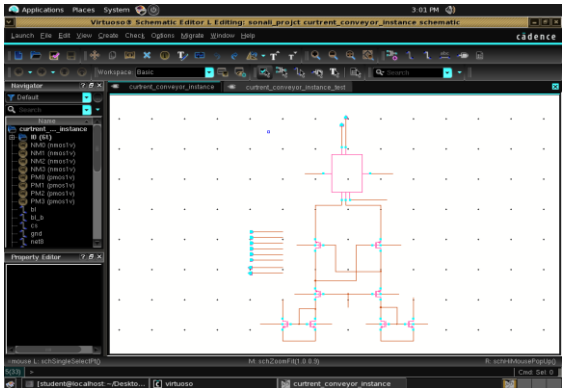

Figure4- Simulated Current Conveyor Sense Amplifier

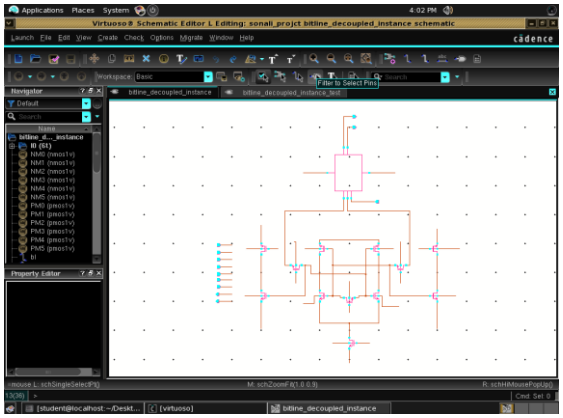

Figure 5- Simulated Bitline Decoupled Sense Amplifier

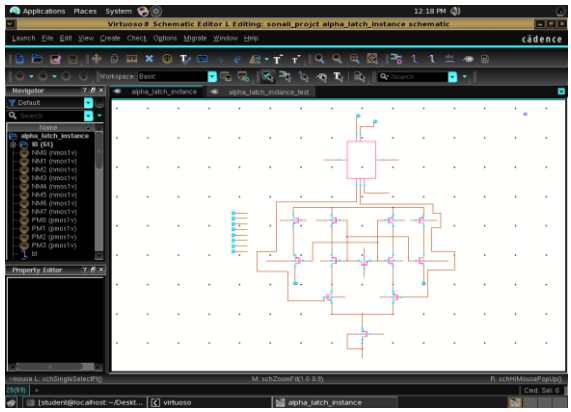

Figure 6- Simulated Alpha Latch Sense Amplifier

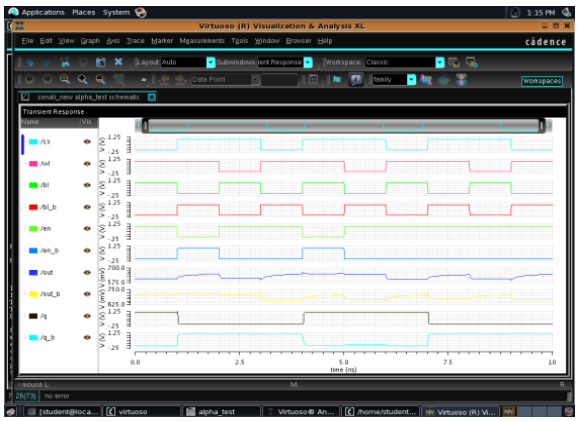

Figure 7- Waveform of Alpha Latch Sense Amplifier

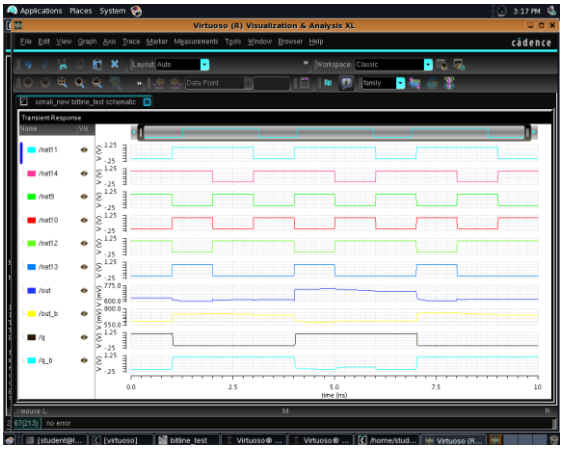

Figure 8- Waveform of Bitline Decoupled Sense Amplifier

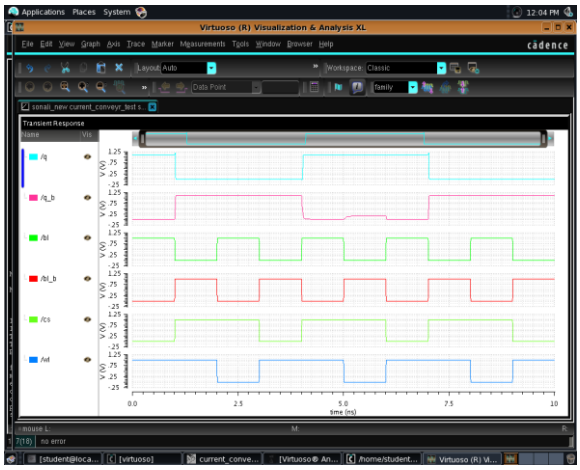

Figure 9- Waveform of Current Conveyor based Sense Amplifier

In this paper, we have seen the effect of capacitance on average power and average Leakage power when capacitance is kept variable and lies in the range of 100 pf to 500pf.

Given below is the table which clearly shows this effective analyses as well as the graph which clearly shows the up and down in power.

Table 1- Table showing power when capacitance is varying in range of 100pf-500p**f**

Capacitance versus Power where capacitance ranges 100pf – 500pf		
Design	**Average Power (uW)**	**Avarage Leakage Power (nW)**
Alpha Latch	9.236	0.223
Bitline Decoupled	1.447	0.172
Current Conveyor	5.663	0.121

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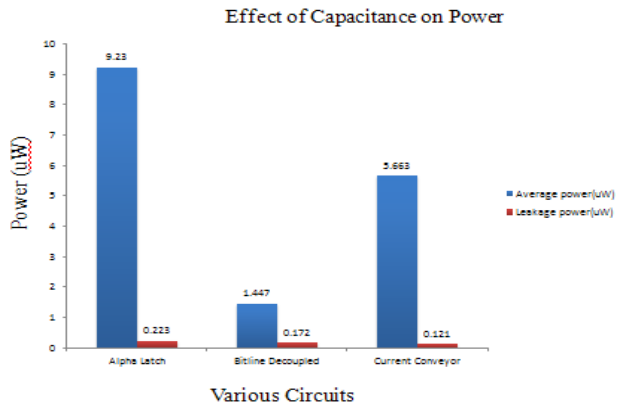

Figure 10- Effect of Capacitance on Power where capacitance ranges 100pf – 500pf

We also analyzed the total average power and total average leakage power of three circuits. Table 2,For this we kept capacitance at bl 100pf and bl_b 200pf.

Table 2- Power analysis of three circuits

Power Comparison of three circuits		
Design	**Average Power, (uW)**	**Power Dissipation, (nW)**
Alpha Latch	2.255	0.022
Bitline Decoupled	2.386	0.129
Current Conveyor	2.813	0.012

Table 3- Maximum and Minimum Power of three circuits

Maximum and Minimum Power of three circuits		
Design	**Y_{max}**	**Y_{min}**
Alpha Latch	$6.15E^{-05}$	$4.10E^{-08}$
Bitline Decoupled	$9.61E^{-05}$	$2.06E^{-07}$
Current Conveyor	$6.46E^{-05}$	$9.63E^{-09}$

The table clearly sum ups that Alpha Latch is more preferable when analyzing and considering average power consumed. If consider average leakage power then current conveyor seems to be preferable. Figure 11 shows the graph between different powers.

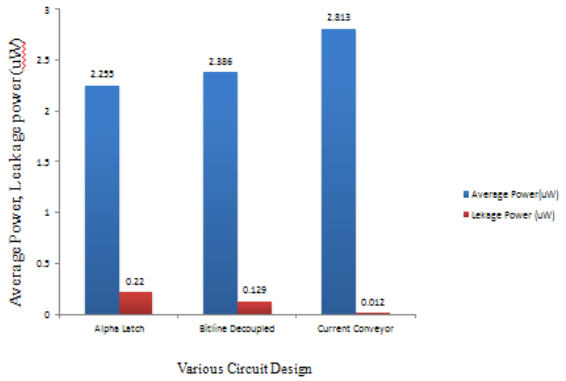

Figure 11- Power analysis of circuits

As we see in the Table3 below, it has clearly shown that if temperature exceeds the working room temperature (27°C), it effects the power of circuits too.

For this we varies temperature from 27°C- 150°C. Figure 12 graph clearly marks the ups in power as the temperature rises. Figure 12- Graph showing variation in average power with varying temperature ranges 27°C-150°C.

Table4- Average power with varying temperature ranges 27°C- 150°C

Temp (°C)	Bitline (uW)	Current (uW)	Alpha (uW)
27	1.45	2.81	2.26
40.67	1.47	2.84	2.29
54.33	1.49	2.86	2.31
68	1.50	2.88	2.33
81.67	1.51	2.89	2.35
95.33	1.52	2.90	2.35
109	1.53	2.90	2.36
122.7	1.53	2.90	2.36
136.3	1.50	2.89	2.39
150	1.43	2.86	2.38

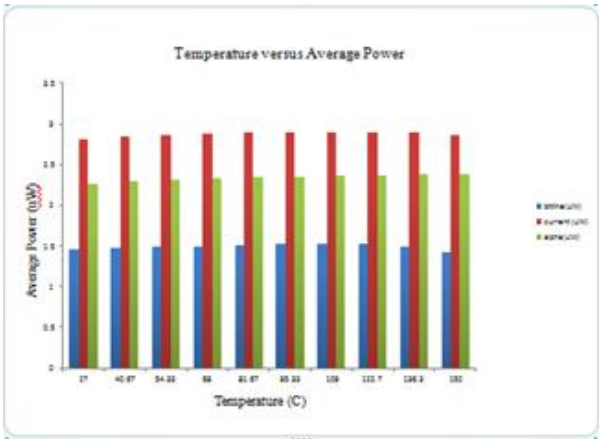

Figure 12- Graph showing variation in average power with varying temperature ranges 27°C- 150°C

IV. CONCLUSION

Static Random Access Memory designed with peripheral blocks to achieve operation low power consumption and high speed.. The simulation have been done offering both speed and power improvements. Furthermore it can operate with clock frequency as high as 1.25 GHz which is assumed to be highest in considered circuits. It provides better reliability at 1V supply voltage. Thus it can be concluded that existing SA are best suited where low power, high speed, stability and reliability are of crucial design considerations. This paper mainly focuses on analysis and comparison of various topologies of current mode sense amplifier.

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