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# Design and Implementation of FM0/Manchester Encoder using VHDL

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**Abstract**: The dedicated short range communication (DSRC) is an important technique to push the intelligent transportation system (ITS) into our daily life. The transmitted signal is anticipated to have zero mean for vigor issue and this is also referred as dc-balance. The FM0 and Manchester codes are used to reach the dc-balance in DSRC. The FM0 encoder and Manchester encoder structures are different, so that limited to reuse the VLSI architecture for generating both the codes. In this work, the similarity oriented logic simplification (SOLS) scheme is used to conquer this limitation. The hardware utilization rate (HUR) of FM0 and Manchester encoders are raised from 57.14% to 100% with SOLS technique. The SOLS technique based FM0 and Manchester encoder structure has better performance compared with existing structure.

**Keywords:** The dedicated short range communication, Manchester, FM0, VLSI Design.

## I. INTRODUCTION

The dedicated short range communication (DSRC) [2] is a etiquette for one way or two way medium range communication mainly for the intelligent transportation system (ITS). The automobile to roadside and automobile to automobile are two important categories in DSRC. In automobile to automobile, the DSRC sending and receiving messages from one automobile to other automobile for safety issues and public information pronouncement [3], [4]. The safety matters incorporate inter cars distance, collision alarm, intersection warning and blind spot. The automobile to roadside DSRC systems are mainly concentrating on the intelligent transportation service, such as electronic toll collection (ETC) system. Using ETC system, the toll collection is electrically consummate with the contactless IC-card platform. The payment for parking service also used the ETC system.

**Table I:** Profile of DSRC Standards for America, Europe and Japan

| Parameter | Europe | America | Japan |
|---|---|---|---|
| Organization | European Committee for Standardization | America Society for Testing and Materials | Associate of Radio Industries and Business |
| Data rate | 500kbps | 27Mbps | 4Mbps |
| Carrier Frequency | 5.8GHz | 5.9 GHz | 5.8GHz |
| Modulation | ASK,PSK | OFDM | ASK |
| Encoding | FM0 | Manchester | Manchester |

The DSRC standards have been recognized by several organizations in various countries. The Table I shows the DSRC standards of America, Japan and Europe. The transmitted signal is anticipated to have zero mean for vigor issue and this is called as dc-balance. But the transmitted signal contains an arbitrary binary sequence, which is difficult to obtain the dc-balance. So, the encoders are used in communication to convert one form of information into another form, which is suitable for transmission. Different types of encoders are available in communication systems. The FM0 and Manchester encoders are mainly used in DSRC to attain the dc-balance. This paper is organized as follow: Section II explains the coding principles of Manchester encoding. Section III explains the coding principles of FM0 encoding. Section IV explains the Hardware Utilization of FM0 and Manchester encoders. Section V describes the SOLS technique based FM0/Manchester encoder. Simulation and Synthesis Results are described in Section VI. Finally the Section VII gives the conclusion. In this work, CLK and X represents the clock signal and input data.

## II.MANCHESTER ENCODING TECHNIQUE

Manchester encoding is also referred as phase encoding. This encoding technique generally used for higher operating frequencies. In this coding, the signal is transmitted serially. The Manchester encoder is implemented with an exclusive OR (XOR) operation for X and CLK. The Fig.1. Shows the Manchester encoder structure.

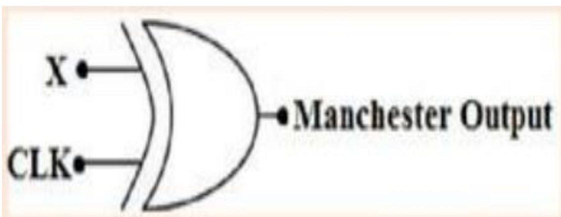


Fig.1.Manchester Encoder

$$Manchester\ Encoder = X \oplus CLK \qquad (1)$$

Example for Manchester encoding is given in Fig.2. For each X, Manchester code contains two parts: one for former half cycle of clock signal and other for latter half cycle of clock signal. Table II shows the operation of Manchester encoding.

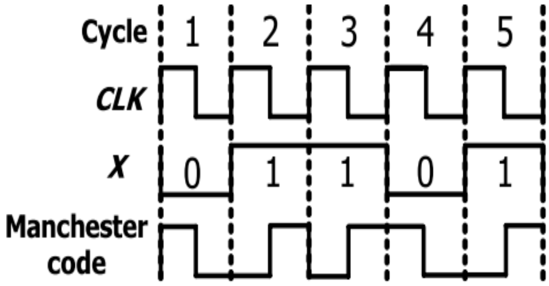


Fig-2: Example for Manchester encoding

**Table II:** Operation of Manchester Encoding

| Input Data | Clock Signal | Manchester Code |
|---|---|---|
| 0 | 1 | 1 |
| | 0 | 0 |
| 1 | 1 | 0 |
| | 0 | 1 |
| 1 | 1 | 0 |
| | 0 | 1 |
| 0 | 1 | 1 |
| | 0 | 0 |
| 1 | 1 | 0 |
| | 0 | 1 |

In Manchester encoding, if the input X is logic-0 and clock signal CLK is logic-1 then output signal is logic-1. If the input X is logic-0 and clock signal CLK is logic-0 then output signal is logic-0. If the input X is logic-1 and clock signal CLK is logic-1 then output signal is logic-0. If the input X is logic-1 and clock signal CLK is logic-0 then output signal is logic-1.

## III.FM0 ENCODING TECHNIQUE

FM0 encoding is also called as Biphase space encoding. The FM0 encoding contains the following three rules.

1. If input data X is the logic-0, the FM0 code must demonstrate a transition between former half cycle of CLK and later half cycle of CLK.
2. If X is the logic-1, no transition is permitted between half cycles of CLK.
3. The transition billed among each FM0 code, no affair what the X is.

Example for FM0 encoding is shown in Fig.3. For each X, the FM0 code contains two parts: one for former half cycle of CLK and other for later half cycle of CLK.

In Fig.3 at cycle-1, the X is logic-0, according to rule-1 their exhibits a transition on FM0 code. For simplicity, this transition is initially set from logic-0 to logic-1. According to rule-3 transition is billed among each FM0 code, so in the beginning of cycle-2 the logic-1 is changed to logic-0. According to rule-2, the entire cycle-2 holds the logic level without any transition.

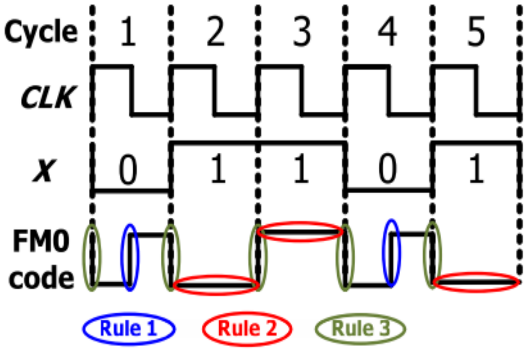


Fig.3. Example for FM0 encoding

## IV.HARDWARE ARCHITECTURE OF FM0 and MANCHESTER ENCODERS

The Manchester encoder hardware architecture contains an xor operation as shown in Fig.1. The Hardware Architecture of the FM0 encoder is designed using the finite state machine (FSM). The FSM of FM0 code contains four states that can be shown in Fig.4.

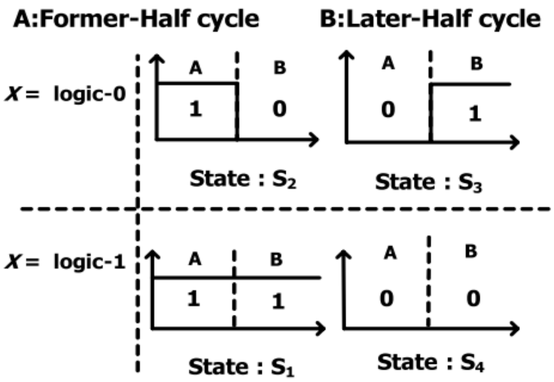


Fig.4.States definition for FM0 encoding

Each state is assigned to a state code and each state code contains A and B. Based on the FM0 contained coding principles, Fig.5 shows the FSM of FM0. Suppose the initial state is $S_1$ and its state code is 11 for A and B. If the input signal X is logic-0, the state transition must pursue both rules 1 and 3. If the X is logic-1, based on rules 2 and 3 the state transition is done.

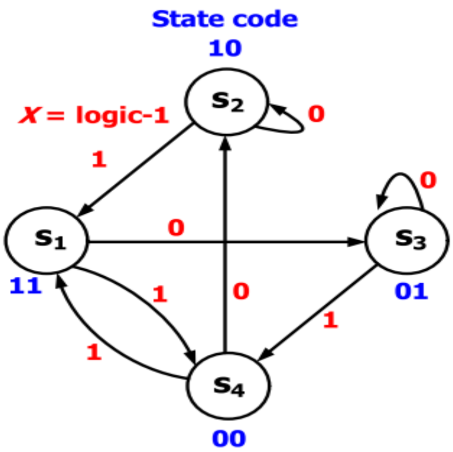


Fig.5. Finite State Machine (FSM) of FM0

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The Table III shows the state transition table of FM0. In Table III A(t) and B(t) represents the current states at time instant 't'. A(t-1) and B(t-1) represents the previous states.

Table III: State Transition table of FM0

| Previous State | | Current State | | | |
|---|---|---|---|---|---|
| A(t-1) | B(t-1) | A(t) | | B(t) | |
| | | X=0 | X=1 | X=0 | X=1 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |

From Table III, the Boolean operations for A(t) and B(t) are given as

$$A(t) = \overline{B(t-1)} \quad (2)$$

$$B(t) = X \oplus B(t-1) \quad (3)$$

The Boolean operations involved in FM0 code is given as

$$FM0\ code = CLK\ A(t) + \overline{CLK}\ \ B(t) \quad (4)$$

$$FM0\ code = CLK\ \overline{B(t-1)} + \overline{CLK}\ B(t) \quad (5)$$

From Equations (1) and (4) Fig.6. Shows the Hardware Architecture of FM0/Manchester encoders.

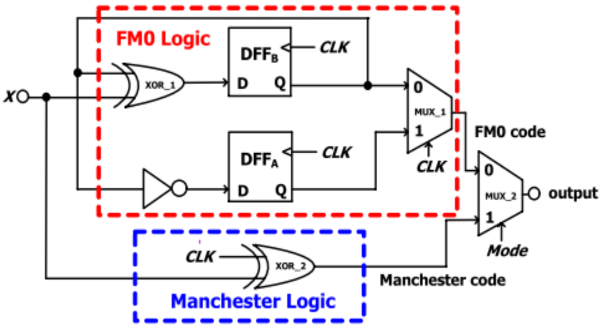


Fig.6.Conventional Hardware Architecture of FM0/Manchester Encoder.

FM0 encoder hardware architecture is shown in top part of the Fig.6. Manchester encoder hardware architecture is shown in bottom part of the Fig.6. The Manchester encoder simply performs the XOR operation between the input data X and clock signal CLK. The FM0 encoder depends on input data X and previous state of the FM0 code. From the Fig.6, the flip flops $DFF_A$ and $DFF_B$ are used to store the state code of the FM0 code. MUX_1 switch the A(t) to B(t) based on the selection of clock signal. A(t) and B(t) are implementing based on equations (2) and (3). Depending on mode selection of the MUX_2 the coding is performed. The FM0 code is obtained, when mode=0 and Manchester code is obtained, when mode=1. To estimate the Hardware Utilization of Fig.6.

The Hardware Utilization Rate (HUR) defined as

$$HUR = \frac{Active\ Components}{Total\ Components} \times 100\% \quad (6)$$

The component is referred as the hardware to perform a particular logic function, such as OR, AND, NOT and flip flops. The components that work for Manchester or FM0 encoding are defined as active components. The total components are the number of components in the complete hardware structure, no matter what encoding is performed. The Hardware Utilization Rate of Manchester and FM0 encodings are listed in Table IV. From the Fig.6, the total component are 7 including MUX_2 to specify which coding method is performed. The active components FM0 encoding are 6 and its HUR is 85.71%. The active components of Manchester encoding are 2 and its HUR is 28.57%. Average HUR of this hardware architecture is 57.14% which is low and roughly half of the total components are wasted.

Table IV: HUR of FM0/Manchester encoder

| Coding | $\frac{Active\ Components}{Total\ Components}$ | HUR |
|---|---|---|
| FM0 | 6/7 | 85.71% |
| Manchester | 2/7 | 28.57% |
| Average | 4/7 | 57.14% |

The coding diversity between the FM0 and Manchester codes acutely confines the prospective to design a fully salvage architecture.

## V.FM0 ENCODER AND MANCHESTER ENCODER ARCHITECTURE DESIGN USING SOLS TECHNIQUE

The intention of SOLS scheme is to design a fully salvaged VLSI architecture for Manchester and FM0 encodings. The SOLS technique is divided into two categories: 1) Area Compact Retiming 2) Balance logic operation sharing.

### A) Area Compact Retiming

The FM0 logic in Fig.6 is simply shown in Fig.7(a). The logic for B(t) and the logic for A(t) are the Boolean functions to obtain B(t) and A(t). For FM0, the $DFF_A$ and $DFF_B$ are used to store the state code of each state. From equations (2) and (3) the alteration of state code depends only on B(t-1) instead of both B(t-1) and A(t-1).

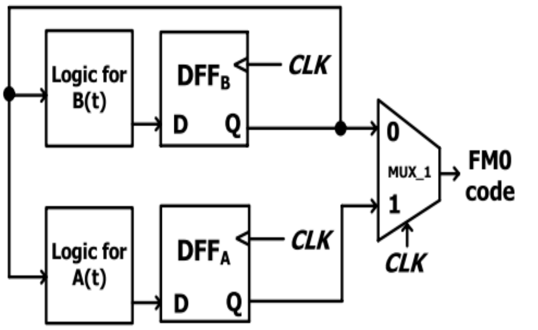


Fig.7(a). FM0 Encoder without Area Compact Retiming

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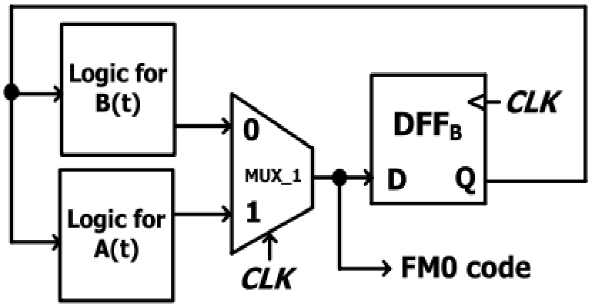


Fig.7(b).FM0 Encoder with Area Compact Retiming

A single one bit flip flop is only required for FM0 encoding to store the B(t-1). If the flip flop $DFF_A$ is removed directly, that presents non synchronization between A(t) & B(t) and causes the logic blunder of FM0 code. The logic fault is avoided by replacing the flip flop $DFF_B$ after the MUX_1 as shown in Fig.7(b), Where the $DFF_B$ is tacit to be positive edge triggered. At each cycle the FM0 code embracing A & B and obtained from the logic of A(t) and B(t).

The MUX_1 is used to switch the FM0 code alternatively between A(t) and B(t) with control signal CLK. In Fig.7(a) the output of flip flop $DFF_B$ is directly given to the logic for B(t) with one cycle latency. If the CLK is logic-0, the MUX_1 selects the B(t) and conceded to the D of $DFF_B$ . Then the impending positive edge of the CLK revises it to the Q of $DFF_B$.

The timing diagram of FM0 encoding with area compact retiming as shown in Fig.8.

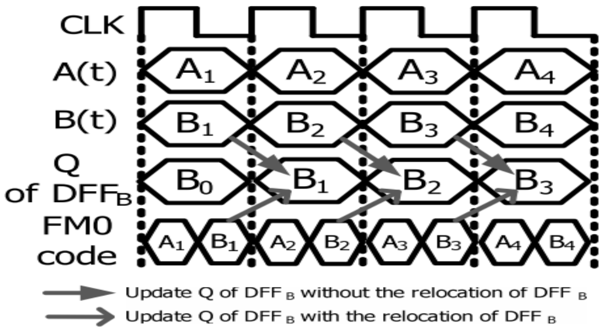


Fig.8.Timing diagram of FM0 encoder with Area Compact Retiming

**B) Balance Logic Operation Sharing**

The Manchester encoding can be obtained from X xor CLK and it is also given as

$$X \oplus CLk = X\,\overline{CLK} + \bar{X}\,CLK \tag{7}$$

The expression (7) can be realized using multiplexer as shown in Fig.9(a). It is fairly related to the Boolean function of FM0 encoding in expression (4). From the expressions (4) & (6) the Manchester and FM0 logics have a multiplexer with control signal CLK. The topic of balance logic operation sharing is shown in Fig.9(b), in that to incorporate the $\bar{X}$ into A(t) and X into B(t).

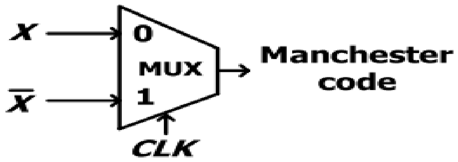


Fig.9(a).Multiplexer based Manchester Encoder

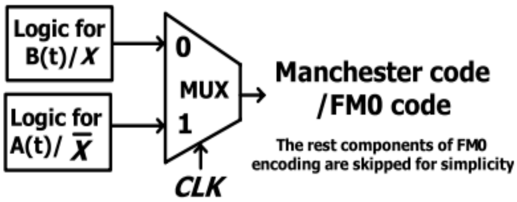


Fig.9 (b).Combines the logic operations of FM0 and Manchester Encoders

The fig.10 shows the logic for A(t)/ $\bar{X}$. The inverter of B(t-1) gives the A(t) and inversion of X gives the $\bar{X}$. The logic for A(t)/ $\bar{X}$ use one inverter and a multiplexer is sited prior to the not gate to switch the operands of X and B(t-1). Based on mode signal to perform either Manchester or FM0 encoding.

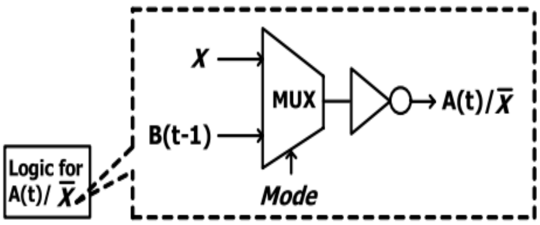


Fig.10.Balance Logic Operation Sharing of A(t) & $\bar{X}$

The logic for B(t)/ $X$ is also derived using similar concept, that can be shown in Fig.11(a). But the structure shown in Fig.11(a) has a drawback. The XOR gate is only used for FM0 encoding and not used for Manchester encoding. This results HUR of this architecture is decreases. The X can be interpreted as X ⊕ 0 and this XOR operation can be used for both FM0 and Manchester encodings. As a result, the Fig.11(b) shows the logic for B(t)/$X$ . In that multiplexer is used to switch the operands of B(t-1) and logic-0. Using area compact retiming technique the multiplexer in Fig.11(b) is replaced with $DFF_B$ as shown in Fig.11(c). The CLR is the clear signal used to reset the $DFF_B$ content to logic-0. The Manchester encoding is performed by activating the CLR, this can set $DFF_B$ content to zero. The FM0 encoding is performed by disabling the CLR and $DFF_B$ gives the B(t-1).

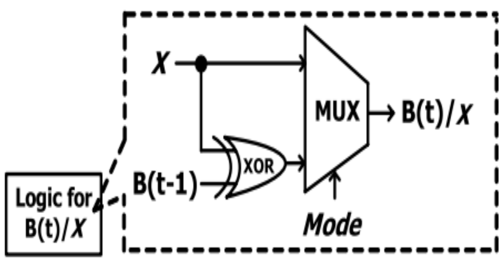


Fig.11(a).Balance Logic Operation Sharing of X and B(t) without XOR sharing

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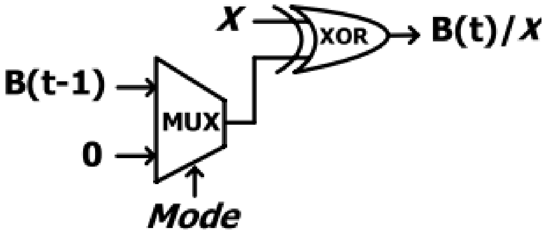


Fig.11(b).Balance Logic Operation Sharing of X and B(t) with XOR sharing

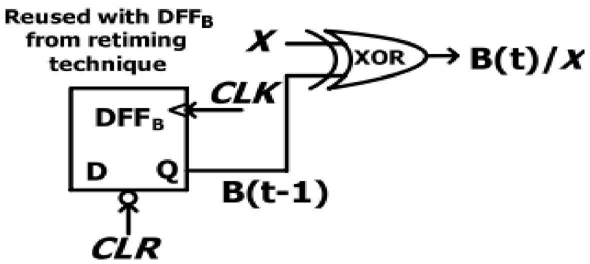


Fig.11(c).Sharing of the reutilized $DFF_B$ from Area compact retiming technique

The Modified architecture of Manchester/FM0 encoder with SOLS technique is shown in Fig.12.

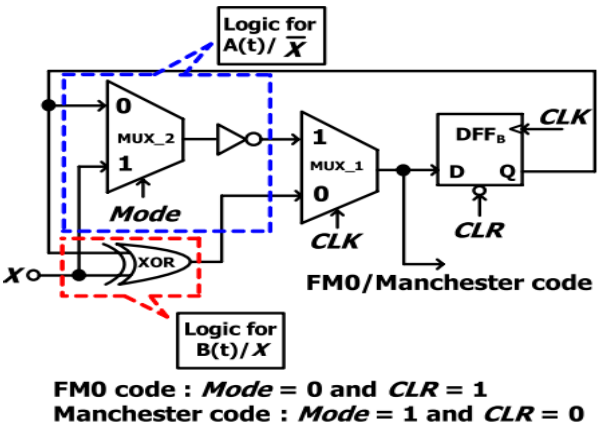


Fig.12. Modified structure of FM0/Manchester encoder with unbalance computation time between B(t)/X and A(t)/ $\bar{X}$

In Fig.12 the computation time of MUX_2 is same as the computation time of XOR operation. An inverter is placed after the MUX_2, this causes unbalance computation time between B(t)/X and A(t)/ $\bar{X}$ that results glitch to MUX_1.

To eliminate the unbalance computation time by using XNOR gate with an inverter in place of XOR in the logic for B(t)/X and an inverter is also used in logic for A(t)/ $\bar{X}$.

So that, an inverter is placed after the MUX_1 output. This balance the computation time between A(t)/ $\bar{X}$ and B(t)/X.

The architecture of FM0/Manchester encoder using SOLS scheme with balance computation time between B(t)/X and A(t)/ $\bar{X}$ is shown in Fig.13.

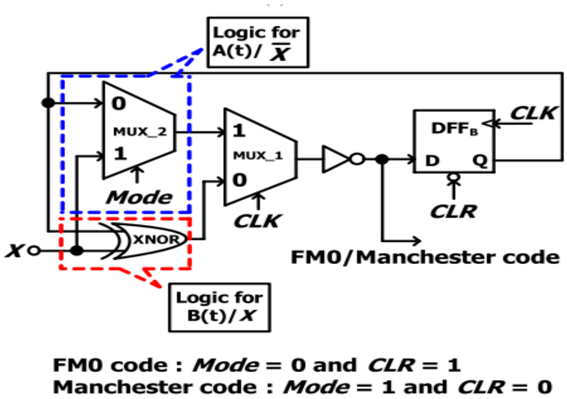


Fig.13. Modified structure of FM0/Manchester encoder with balance computation time between B(t)/X and A(t)/ $\bar{X}$

The FM0 or Manchester encodings are performed based on mode and CLR signals. Every Component of the Manchester/FM0 encoder architecture with SOLS technique is active for both Manchester and FM0 encodings, so that the HUR is 100%. The HUR of FM0/Manchester encoder architecture is shown in Table V.

Table V: HUR of Manchester/FM0 encoder architecture

| Coding | $\frac{\textit{Active Components}}{\textit{Total Components}}$ | HUR |
|---|---|---|
| FM0 | 5/5 | 100% |
| Manchester | 5/5 | 100% |
| Average | 5/5 | 100% |

## VI.RESULTS AND PERFORMANCE ANALYSIS

We have verified the FM0/ Manchester encoder architectures by writing the VHDL code, Simulated and Synthesized.

The Simulation Result of the FM0/Manchester encoder with SOLS technique in case of FM0 encoding is shown in Fig.14.

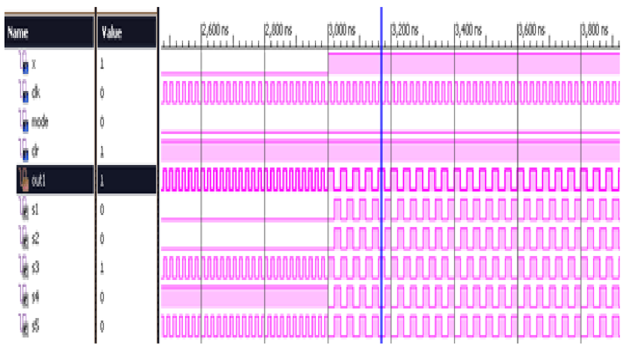

Fig.14. The Simulation Result of the FM0/Manchester encoder with SOLS technique in case of FM0 encoding

The Simulation Result of the FM0/Manchester encoder with SOLS technique in case of Manchester encoding is shown in Fig.15

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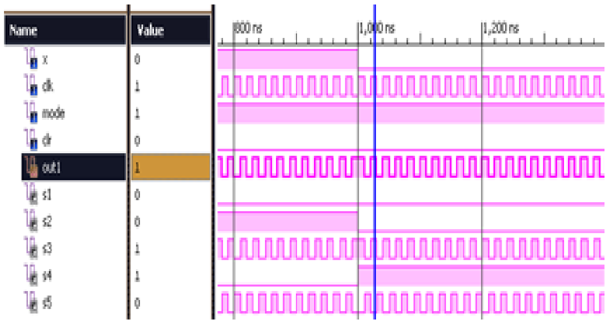


Fig.15.The Simulation Result of the FM0/Manchester encoder with SOLS technique in case of Manchester encoding

Table VI and Fig.16 shows the comparison between the FM0/Manchester encoder without and with SOLS technique in terms of Delay, Number of slices and Power Consumption.

Table VI: Comparison Table of FM0/Manchester encoder Structures

| Design | Delay (ns) | No.of Slices | Power consumption(mW) |
|---|---|---|---|
| FM0/Manchester encoder without SOLS technique | 2.250 | 3 | 38 |
| FM0/Manchester encoder with SOLS technique | 1.754 | 1 | 35 |

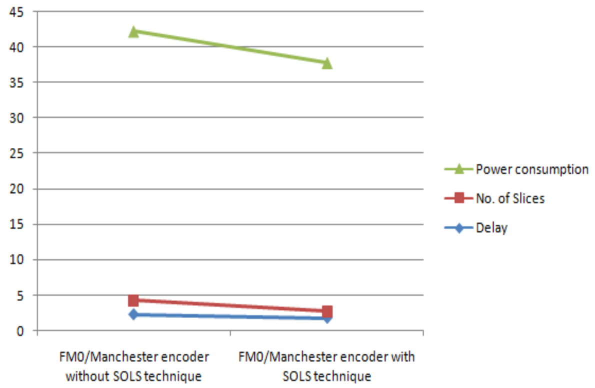


Fig.16.Comparison Graph of FM0/Manchester encoder Structures

## VII.CONCLUSION

The dedicated short range communication (DSRC) is an important technique to push the intelligent transportation system (ITS) into our daily life. The transmitted signal is anticipated to have zero mean for vigor issue and this is also referred as dc-balance. The FM0 and Manchester codes are used to reach the dc-balance in DSRC. The FM0 encoder and Manchester encoder structures are different, so that limited to reuse the VLSI architecture for generating both the codes. In this work, the similarity oriented logic simplification (SOLS) scheme is used to conquer this limitation. The hardware utilization rate (HUR) of FM0 and Manchester encoders are raised from 57.14% to 100% with SOLS technique. From the Synthesis results, the SOLS technique based FM0 and Manchester encoder structure yields significantly less Delay, Area and Power Consumption than the Conventional FM0 and Manchester encoder structure.

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## BIOGRAPHIES

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