IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

Comparison and Analysis of Combinational Circuit Using Different Logic Styles

Poonam Dhruwe[1], Chandrahas Sahu[2]

PG Student [VLSI], Dept. of ECE, Shri Shankracharya Group of Institution, Bhilai, Chhattisgarh, India[1]

Assistant Professor, Dept. of ECE, Shri Shankracharya Group of Institution, Bhilai, Chhattisgarh, India[2]

Abstract: This paper discusses a comparative study of combinational circuits with different logic style of designing. Logic style affects the switching capacitance, transition activity, power, delay. Various logic styles have been compared and taking AND, OR, XOR and FA as reference circuit. Different logic styles are compared with respect to transistor count, power dissipation and delay in 250nm technology. It is observed that less power is consumed in the m-GDI than the other logic styles.

Keywords: Complementary CMOS, GDI, M-GDI technique, low power, high speed, transistor count.

I. INTRODUCTION

As the density and operating speed of CMOS chips increase, power dissipation has become a critical concern in the design of VLSI circuits, especially in mobile and portable ASIC systems. In traditional CMOS circuits, low-power design includes the reduction of supply voltage, node capacitance, and switching activity. However, in recent years power consumption is important factor in circuit design. Fast advancement of VLSI CMOS circuit technology is satisfied by increased use of small sized and wireless systems with very low power consumption. Due to the continued scaling of supply voltage and technology, leakage power is becoming very significant in power dissipation of nano scale CMOS circuits. Consequently, the total power consumption is a critical factor while designing low power digital circuits. In order to reduce power dissipation different design techniques have been developed. Logic style that is popular in low power digital circuit is gate GDI technique. GDI technique overcomes the problems of other logic styles.

II. PREVIOUS WORK

Complementary CMOS logic style: CMOS structure consist PMOS pull-up and NMOS pull-down transistors.

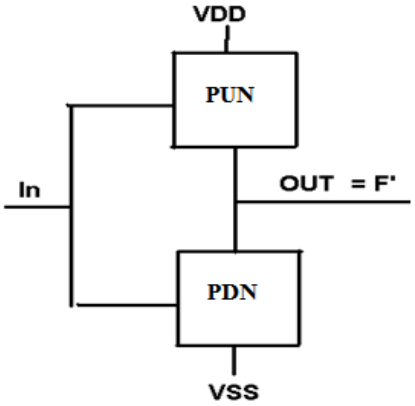


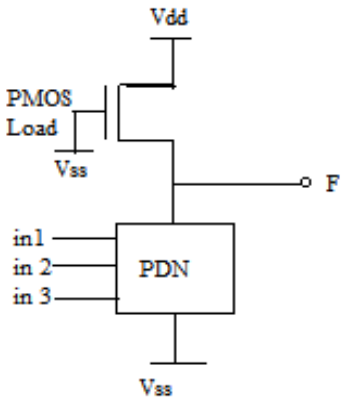
Fig.1 CMOS logic gate as a combination of pull up and pull down network

The layout of this type of logic gates is simple and efficient because of the complementary transistor pairs however due to employing large number of PMOS transistors in its structure, the input capacitance is large and also the existence of sized up PMOS transistors has direct impact on its area.

Fig.1 shows the basic structure of CMOS logic. It consist pull up network connected to high voltage terminal i.e. Vdd and pull down network connected to low voltage terminal i.e. ground (Vss).

Important characteristics of CMOS are high noise immunity and low static power consumption. There are certain drawbacks of CMOS logic such as it uses more number of transistors which increases the delay and area.

Ratioed logic: Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation.



pseudo-NMOS

Fig.2 Ratioed logic gate

The main use of the PUN in complementary CMOS is to provide a conditional path between Vdd and the output

DOI 10.17148/IJARCCE.2016.54122

IJARCCE
ISSN (Online) 2278-1021
ISSN (Print) 2319 5940
International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

when the PDN is turned off. In ratioed logic, entire PUN is replaced with a single unconditional load device that pulls up the output for a high output. Instead of a combination of active pull-down and pull–up networks such a gate consist of an NMOS pull-down network that realizes the logic function, and a simple load device. It uses grounded PMOS load and is referred to as a pseudo-NMOS gate.
The clear advantage of pseudo NMOS is the reduced number of transistors (N+1 versus 2N for complementary CMOS), so the number of components has reduced and area also reduced. It also reduces the complexities of the circuit. Because less hardware used so the capacitance becomes reduced. A major disadvantage of the pseudo NMOS gate is the static power that is dissipated when the output is low through the direct current path exist between Vdd and ground.

Pass transistor logic: A popular and widely used alternative to complementary CMOS is pass transistor logic which reduces the number of transistor required to implement logic functions by allowing the primary inputs to drive gate terminals as well as source/drain terminals.

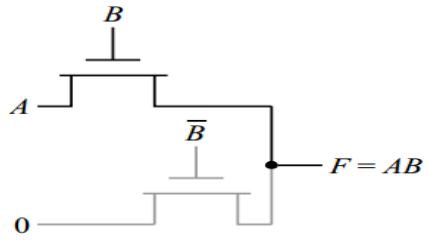


Fig.3 pass transistor implementation of an AND gate

Advantage of PTL include high speed, lower power consumption and lower interconnect effect. The main drawbacks of PTL logic is its slower operation and reduced voltage swing.

Gate diffusion input (GDI): The GDI is a new design technique which improves logic swing and less static power dissipation. Using GDI technique several logic functions can be implemented using less number of transistors. This method is suitable for design of a fast, low-power circuit, using reduced number of transistors, while improving logic level swing and static power characteristics.

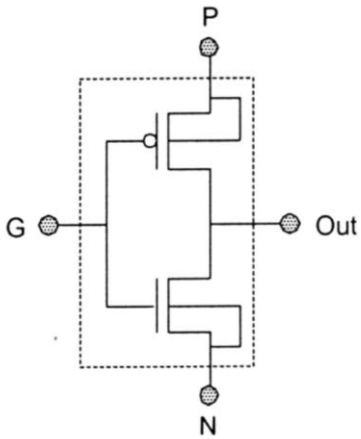


Fig.4 GDI basic cell

The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N or P (respectively).

GDI technique offers low power, less transistor count and high speed, the major challenges occurs in the fabrication process. The GDI technique requires twin-well CMOS or Silicon on Insulator process to realize a chip which increases the complexity as well as the cost of fabrication.

Modified Gate diffusion input: M-GDI logic style allows reducing power consumption, delay and area of digital circuits. M-GDI overcomes the limitation of GDI.

III. M-GDI

Power dissipation becomes most important restriction in high performance applications. Optimizations for basic logic gates are fundamental in order to get better the performance of a variety of low power and high performance devices. These limitations can be overcome by modified gate diffusion input (M-GDI) logic style. This technique allows reducing power consumption, delay and area of digital circuits.

Fig.5 shows basic M-GDI cell. In contrast with basic GDI cell, Modified GDI cell contains

- A low voltage terminal Sp connected to high constant voltage (i.e. power supply).
- A high voltage terminal Sn connected to a low constant voltage (i.e. ground).
-

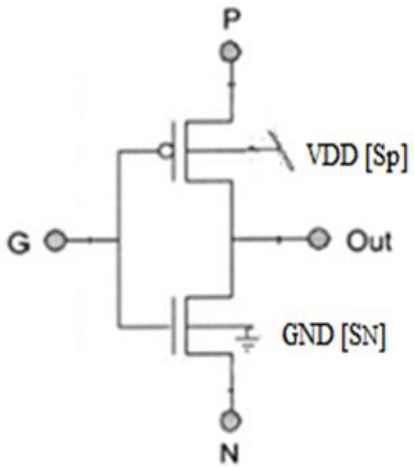


Fig.5 M-GDI basic cell

In the M-GDI cell, the bulk node of PMOS transistor is connected to the high constant voltage referred to as supply voltage or VDD and the bulk of NMOS transistor is connected to low constant voltage referred to as GND. By doing this the proposed MGDI cell is completely compatible for implementation in a standard CMOS process of fabrication. M-GDI is appropriate for design of low power, high speed circuit using less number of transistors.

IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 4, April 2016

Table 1 Logic function implemented with MGDI technique

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
A	B	A	A+B	OR
B	A	A	AB	AND
B	A'	A	A'B'	NAND
A'	B	A	(A+B)'	NOR
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B	B'	A	A'B+AB'	XOR
B'	B	A	A'B'+AB	XNOR

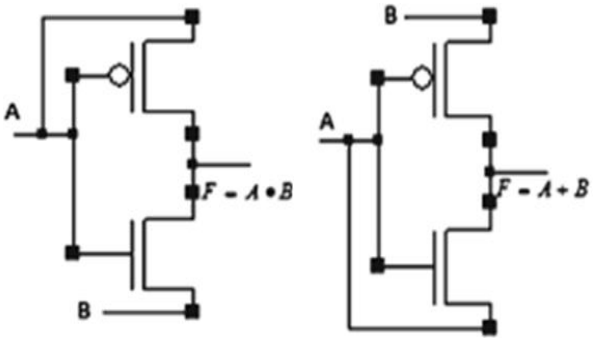


Fig.6 2-input AND gateFig.7 2-input OR gate

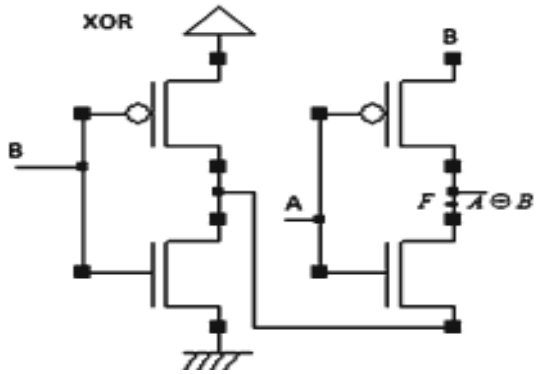


Fig.82-input XOR gate

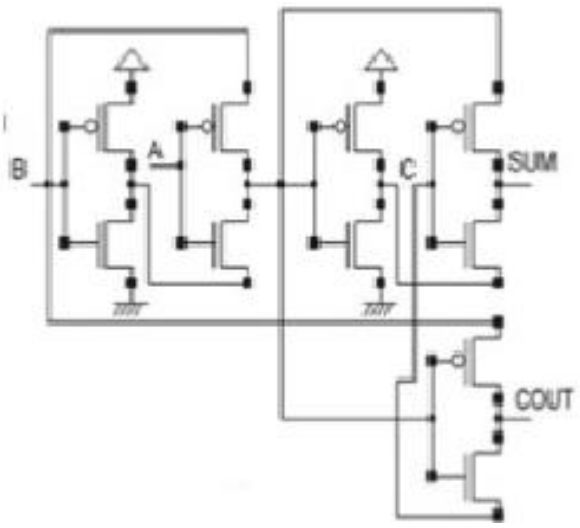


Fig.9 M-GDI Full adder

TABLE 2 Comparative analysis of CMOS, GDI and MGDI

Logic Gates	CMOS			GDI			MGDI		
	Transistor count	Power Dissipation (μW)	Delay (ps)	Transistor count	Power Dissipation (μW)	Delay (ps)	Transistor count	Power Dissipation (μW)	Delay (ps)
AND	6	1.698	0.240	2	1.286	0.200	2	0.986	0.180
OR	6	1.550	0.270	2	1.30	0.280	2	1.20	0.180
XOR	8	1.5	0.567	4	1.48	0.545	4	1.23	0.363
FA	38	12.8	35.1	18	12.5	33.1	10	12.1	32.3

IV. CONCLUSION

In this paper five different logic styles are discussed. The five logic styles are Complementary CMOS, Ratioed logic, Pass transistor, Gate diffusion input and Modified Gate diffusion input. The performance analysis of CMOS, GDI and MGDI is presented in table 2. It has been observed that Modified gate diffusion input design style exhibit better characteristic as compared to other design style. Overall the result shows that MGDI has least delay, low power consumption and less transistor count when compare to existing GDI and CMOS logic style.

REFERENCES

[1] SM.PEDRAM, R.MEHROTRA & XUNWEI WU (Oct 1997) "Comparison Between Nmos Pass Transistor Logic Style vs. CMOS Complementary Cells" , IEEE International Conference On Computer Design: VLSI In Computer & Processor.

[2] M. KONTIALA, M.KUULUSA & J NURAMI (2001) "Comparison Of Static Logic Styles For Low Voltage Digital Design", 8th IEEE International Conference On Electronics Circuit & System.

[3] A.MORGENSHTEIN, A.FISH& WAGNER (2002) "GDI- A Technique for Low Power Design of Digital Circuit: Analysis and Characterization", IEEE International Symposium on Circuit & System.

[4] P.BALASUBRAMANIUN & J.JOHN (Sep 2006) "Low Power Digital Design Using Modified GDI Method", IEEE International Conference On Design & Test Of Integrated System In Nanoscale Technology.

[5] A.K. AGRAWAL, S. MISHRA, R.K. NAGARIA (Dec 2010) "Proposing A Novel Low-Power High-Speed Mixed GDI Full Adder Topology", IEEE International Conference On Control & Embedded System.

[6] S.HIREMATH & D, KOPPAD (Oct 2012) "Low Power Full Adder Circuit Using Gate Diffusion Input Mux", 4th International Conference On Control & Embedded System.

[7] SHOFIA RAM & R.R. AHAMED (July 2013) "Comparison And Analysis Of Combinational Circuit Using Different Logic Styles", 4th International Conference On Computing, Communication & Networking Technologies.

[8] R.MEHRA & A. VERMA (Apr 2013) "Design And Analysis Of Conventional And Ratioed CMOS Logic Circuit", IOSR Journal Of VLSI And Signal Processing.

[9] P.MAGESH KANNAN & K. PRATHYUSHA (2011) "Implement ation Of Low Power Ram in GDI Technique with Full Swing", International Conference On Signal Processing, Communication.

[10] ZIMMENNAN R., FICHTNER W., "Low-power logic styles: CMOS versus pass- transistor logic", IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079-1090, 1997.

[11] K.DHAR, A.CHATTERGEE (2014) "Design Of An Energy Efficient, High Speed, Low Power Full subtractor Using GDI Technique", IEEE Conference On Technology Symposium.

[12] V.DUBEY, R.SAIRAM (2014) "An Arithmetic And Logic Unit Optimized For Area And Power", 4th International Conference On Advance Computing & Communication Technology.

[13] VIJAYA SHEKHAWAT, TRIPTI SHARMA & KRISHNA GOPAL SHARMA (2014) "2 Bit Magnitude Comparator Using GDI Technique", IEEE International Conference on Recent Advances and Innovations in Engineering.