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Implementation of Low power Level Shifter with Logic Error Correction Circuit for Extremely Low-Voltage Digital Circuits

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Abstract: This paper presents the design of low power level shifter that can convert extremely low and to higher output voltages. Level shifters are used to convert voltages from one level to other. In Conventional level shifter circuits the output voltage cannot be discharged at low input voltage. In this paper a Level shifter with lower power dissipation is proposed, it consists of a level conversion circuit and logic error correction circuit. Performance of proposed circuit performance is compared in terms of power dissipation and delay with other existing level shifter circuits. The proposed circuit and other existing level shifter circuits used have been simulated using cadence tool in gpdk180nm technology.

Keywords: Level Conversion Circuit, Level shifter (LS), Logic error correction circuit (LECC), Wide swing cascode current mirror.

I. INTRODUCTION

In System on chip (SoC) designs, distinctive component segments are fabricated on a single chip at different modules and needs diverse voltages to accomplish ideal execution among them To Interface Different modules Level converters are utilized in these designs. Intelligent system networks require countless sensor circuits that measures different physical information in our environment. These circuits need to work at ultra low power. For systems with ultra low-power levels, sub threshold circuits are needed. In order to provide the interface between normal part of the design and sub threshold part of design, Level shifters are used that shifts the voltages between these parts. Power dissipation is a major drawback in today's electronics world as it degrades performance and produces unwanted heat so it needs to be minimized for optimum performance of the design in VLSI circuits. Power dissipation can be reduced by reducing supply voltage. In reconfigurable circuits that contain peripheral circuits which operate at high supply voltage, the non critical circuit should be operated at low supply voltages to achieve advantages from low power dissipation. Level converters are used in these designs to interface the circuit which operates at higher Voltages and the circuit which operates at low Voltages. So due to this, LS had became an essential part of the design. A level shifter with low power dissipation required for low power applications. Level shifter has to operate with low power dissipation and with high speed for achieving the optimum performance in the designs. Interfacing becomes difficult when conventional Level shifters are used when supply voltage (sub threshold circuits) is under 0.5v due to reduction in the drive current. To moderate this issue, techniques like increase in the transistor channel width so the drive currents of LS are improved. Another one is to utilize inverters or multi stage level shifters with numerous supply voltages. These makes circuit configuration more complex. To take care of this issue, in this paper a LS circuit with low power dissipation is proposed that contains LECC and wide swing cascode current mirror.

II. CONVENTIONAL LEVEL SHIFTER

In general there are several level shifter circuits in electronics. But when it comes to basic level shifter the below mentioned conventional level shifter circuit is used Figure 1 shows a conventional LS circuit. As we can see IN and INB inputs are applied to the MN1 and MN2 transistors respectively, a cross coupled PMOS structure is also available.

Here when the input is high, INB is low. As input is high this makes MN1to ON. INB is low this makes MN2 to OFF. This pulls the OUTB node to ground making MP2 transistor to ON state, then OUT node is pulled to V_{DDH} and it makes MP1 transistor to OFF state. Similarly for other case also when input is low OUT is pulled to ground.

For the circuit to operate correctly, the pull up drive current of MP2 and pull down drive current of MN2 must be equal in order to discharge the output correctly. For sub threshold voltage, the on-current of MN2 turns out to be very low this makes the drive currents of nMOSFETs increasingly lower than those of pMOSFETs.

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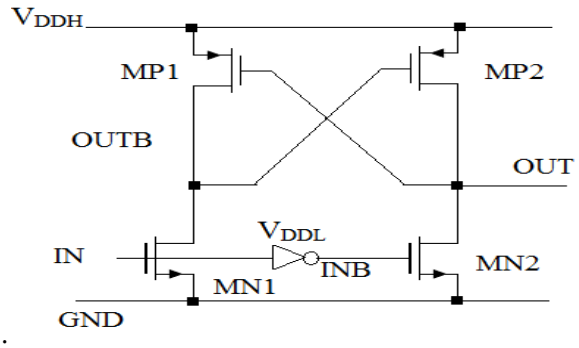

Fig 1.Conventional LS

So the output cannot be discharged properly. Here in this circuit as the MP2 drive current is more than the drive current of MN2, the OUT voltage can't be discharged. Therefore, a conventional LS circuit cannot work accurately in this circumstance of low voltage inputs. So LS cannot interface high voltage circuits and sub threshold operated circuits under 0.5V.

III. PROPOSED LEVEL SHIFTER CIRCUIT

In order to overcome the limitations in the conventional LS circuit a level shifter circuit with logic error correction circuit [1] is proposed to achieve better performance this architecture shown below.

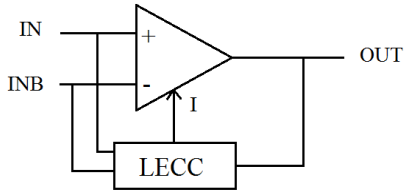

Fig 2.Architecture of proposed LS circuit

This architecture shown in figure 2 consists of a level conversion circuit and Logic error correction circuit (LECC).The Level conversion circuit consists of a wide swing cascode current mirror. The IN and INB signals are applied to the level conversion circuit and OUT is feedback through the LECC.LECC provides the current I when it detects the logic error between the input and output. The complete schematic of the existing level shifter circuit is shown in the figure 3.

i) **Level conversion circuit**

As shown in figure 3 the level conversion circuit is based upon the two stage conventional comparator circuit.It includes a wide swing cascode current mirror. Depending on the difference of the input voltages IN, INB, the output signal of the comparator is generated. The current flowing in the two transistors MN8, MP6 is dependent on the current flowing through MP2 as both these drive currents are given by the same current. So that eliminates the drawback in conventional LS. When both the input and output corresponds to each other the LECC will not detect any error and LECC will not operate, so the level conversion circuit itself is enough for the operation of the circuit. In the normal comparator designs a biasing circuit acts as a reference current circuit for the operation of circuit. But this reference current biasing circuit increases power dissipation of the overall circuit so this could not be used in the circuit. Hence a logic error correction circuit (LECC) has been used which generates operating current to the circuit only when input signal changes and reduces power dissipation.

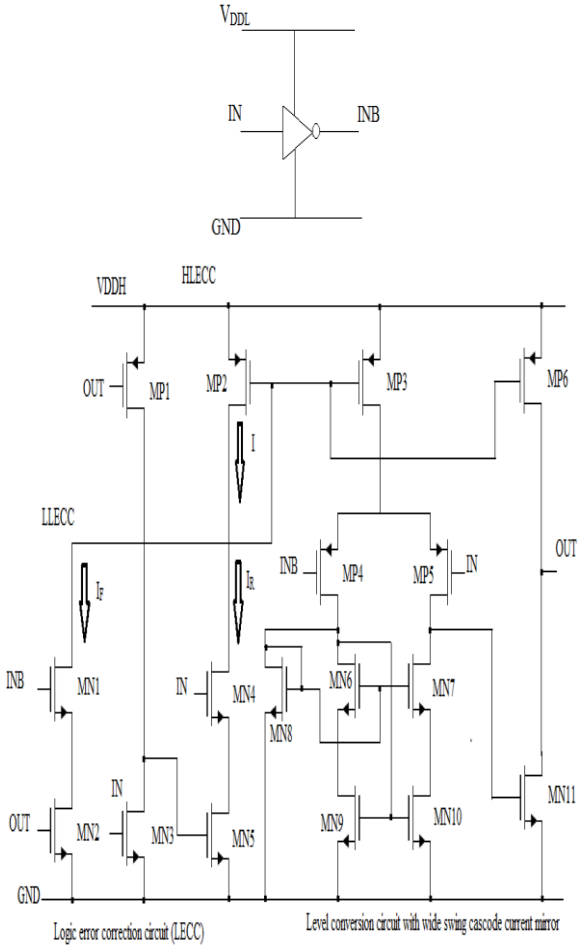

Fig 3.Proposed Level shifter circuit.

ii) **LECC**

As shown in figure 3 the LECC contains two circuit parts they are (LLECC) low logic error correction circuit and (HLECC) high logic error correction circuit. The IN, INB, OUT signals are given to the LECC. LLECC the low logic error correction circuit contains two transistors in series connection they are MN1, MN2. It operates only when low logic levels of input does not corresponds with output. As shown in figure 4 whenever input (IN) makes transition from high to low both MN1 and MN2 transistors are ON. During period at which output not corresponding with low logic levels of IN, a fall transition current I_F will be generated until low logic levels of input corresponds with OUT. When IN and OUT are low this will not supply any current to the level conversion stage as MN2 is OFF because of low logic level of OUT.

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HLECC a high logic error correction circuit contains three NMOS transistors MN3, MN4, MN5 and a PMOS transistor MP1. This HLECC circuit operates only when high logic levels of input differs from OUT signal. As shown in figure 5 whenever input (IN) makes transition from low to high there will be a period at which output not corresponding with high logic levels of IN. Here MP1, MN3, MN4 are ON as IN is high and OUT is low. As the effective voltage of MP1 is greater than MN3 this makes MN5 to ON state. So HLECC works out and a rise transition current I_R will be generated at this period until high logic levels of input corresponds with OUT. When IN and OUT are high HLECC wont supply any current to the level conversion stage as MP1 is OFF because of OUT logic level is high so first part of HLECC is low.

The difference to the normal level conversion circuit and to this conversion circuit in proposed LS is having a wide swing current mirror here instead of normal current mirror, whenever IN is high and INB is low MP4 transistor is ON which makes MN6 to ON resulting in MN8, MN7 to ON as gates are connected. The gates of MN9, MN10 are connected to drain of MP4 so they also will be ON resulting in MN11 to OFF as no gate current comes to this. OUT is pulled to V_{DDH}. Similarly when IN is low INB will be high making current to flow from MP5 and as current does not flow through MP4 which makes other transistors to OFF in current mirror, MN11 is ON as V_{GS} here is positive and pulls OUT to ground.

The LECC produces currents only during input transitions which help to reduce power dissipation. And also by using the wide swing cascode current mirror also power dissipation is reduced as it has higher impedance and lower currents through it. The leakage currents and static power dissipation components of the circuit is reduced on using the wide swing cascode current mirror. Thus by using this circuit we can be able to convert low level voltage input signal to high level output voltage with lower power dissipation. Amount of power dissipation depends on lower supply voltage V_{DDL}.

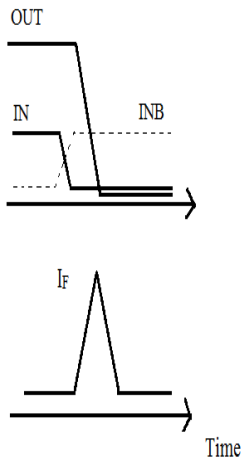

Fig 4.$I_F$current- Generation

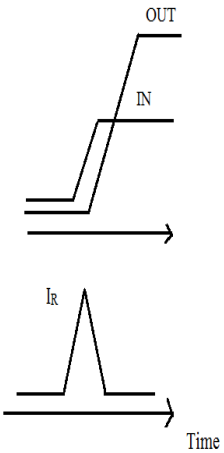

Fig 5.I_R current- generation

IV. SIMULATION RESULTS

The proposed circuit is simulated in cadence tool at different input voltages of V_{IN} and V_{DDL}. Here figure 6 shows the schematic diagram of proposed level shifter in cadence tool. The result shown in figure 7 converts a extremely low input voltage of 0.23V into 3V output at 10 KHz input signal frequency at 0.5V V_{DDL}, 3V V_{DDH}. Similarly figure 8 shows the result of proposed LS for a normal voltage input of 1.5V at 0.5V_{DDL} and at 10 KHz input signal frequency that gives output of 3V. The figure 9 shows the layout representation of the proposed LS circuit using cadence tool. The table 1 shows the power dissipation comparisons of proposed level shifter circuit with other LS circuit from references [1],[5] for various input voltages. The table shows that proposed circuit has less power dissipation than other LS circuits available.

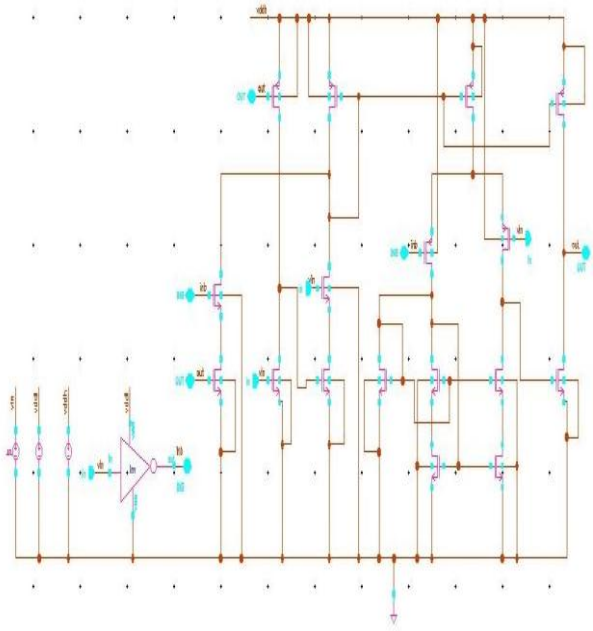

Fig 6.Schematic of proposed LS circuit in cadence tool

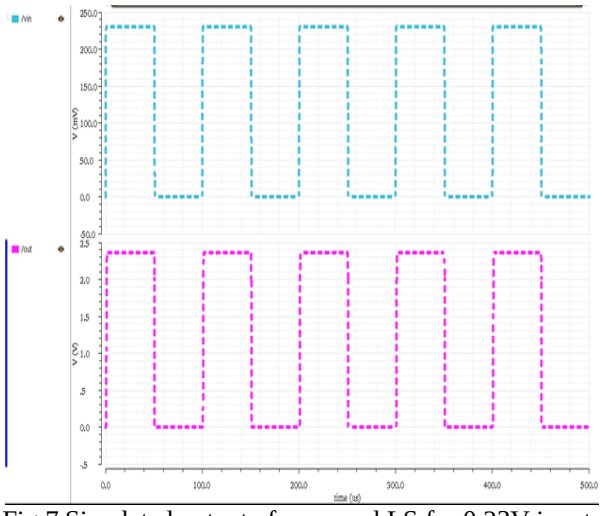

Fig 7.Simulated output of proposed LS for 0.23V input.

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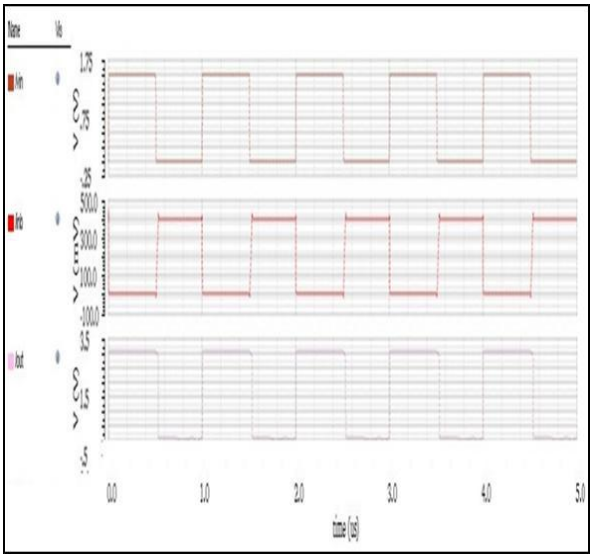

Fig 8.Simulated output of proposed LS for 1.5V input.

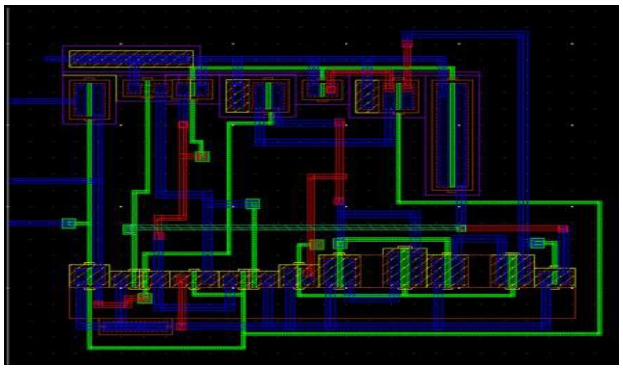

Fig 9.Layout representation of proposed LS circuit in Cadence tool

Table 1: Power dissipation comparison of various LS circuits

Voltages V_{IN},V_{DDL}(V)	**LS[1]**	**LS[5]**	**Proposed LS**
0.8v,1v	10.23pw	10.97pw	10.06pw
0.4v,0.7v	7.45pw	7.64pw	7.34pw
0.4v,0.6v	6.86pw	7.29pw	6.84pw
0.23v,0.5v	3.48pw	3.35pw	3.21pw

V. CONCLUSION

In this paper a new circuit is proposed that can convert extremely low input voltages from the range of 0.2V into high voltages at input signal frequency of maximum 200 KHz at lower power dissipation than compared to other level shifter circuits, it can also convert normal voltages into higher voltages up to a maximum input signal frequency of 1MHz. The proposed level shifter circuit has the best performance compared to other available LS in terms of lower power dissipation. Though the delay of proposed circuit is almost equal to existing LS circuit architecture the power delay product is least for proposed circuit. Hence proposed circuit has better performance than other level shifter circuits.

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