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High Performance Smart Routing for Network on Chip

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Abstract: With the advancement of Very-large-scale integration (VLSI) technology, research is going on to build more complex and robust computing systems in a single silicon chip. Interconnection requirements increase with a rapid pace with the increase of the number of components that appear on the chip thereby posing a limitation on overall on performance. Keeping this in mind we try to propose a Network on chip. The idea of a Network-on-Chip (NoC) borrows networking theory from the computer networking domain and considers each intellectual property (IP) core as a single node. In each node, a high-speed router connects with other routers of neighboring nodes. In a nutshell, the tradeoff between performance, area, and power is significant while designing routers of Network on chip. According to literature survey, the router architecture always contains buffers on the input ports. The buffer scheme is used to store packets; these packets must wait for the output resource due to contention with other packets. These designs have been widely adopted due to their improved performance. Finally, we propose a smart routing with low power, low area and improved performance. In our design Loop Back module is designed as old one, FSM is removed ,Routing Error detection , Logic, centralized Journal of data Packet are removed as our loop back module itself does the same functionality ,Ordinary Buffers are removed , instead of FIFO is used to achieve better performance.

Keywords: Hamming code, Loop Back Module, FIFO, Adaptive algorithm, dynamic reconfiguration, network-on-chip (NoC), reliability, performance, area, power, latency.

I. INTRODUCTION

The NoC features a high level of modularity, flexibility, and throughput. Network on chip comprises routers and interconnections allowing communication between the PEs and IPs [1]. The NoC relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm [6]. Therefore, the path that a data packet is allowed to take in the network depends mainly on the adaptiveness permitted by the routing algorithm (partially or fully adaptive routing algorithm), which is applied locally in each router being crossed and to each data packet To achieve a reconfigurable NoC[4], an efficient dynamic routing algorithm is required for the data packets. The goal is to preserve flexibility and reliability while providing high NoC performance in terms of throughput [3]. Fig. 1 illustrates a dynamic reliable NoC.[2] Fig. 1(a) So dynamic component placement and faulty nodes or regions are the main reasons why fault-tolerant or adaptive algorithms have been introduced and used in runtime dynamic NoCs [4].

Regarding adaptive or fault-tolerant routing algorithms, several solutions have been proposed [6]. Generally, these algorithms correspond to a modified XY [1] routing algorithm that allows faulty or unavailable regions to be bypassed.

The remaining of this paper is organized as follows.

Section II describes the literature survey,
Section III Presents approach and motivation involved [2]
Section IV. Our proposed smart RKT switch.
Section V. presents results as logical simulation results of proposed router, synthesis reports,
Section VI calculations.
Finally, in Section VII conclusion and future works are given.

II. LITERATURE SURVEY

N.O.C is the most hot topic for research in today's time, In [1] it describes about the communication between processing elements, and present NoCs designs, provide integrated solutions to challenging design problems in the communications between different IPs. After a deep survey we find different router architecture like in [2] it describes about a new network-on-chip (NoC) that handles accurate localizations of the faulty parts of the NoC. [3] Presents a new shared buffer based router architecture employing dual buffers. [4] Presents Network-on-Chip (NoC) suitable for Dynamically Reconfigurable Multiprocessors on Chip systems. This NoC is based on routers performing online error detection of routing

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algorithm [6] and data packet errors. These routers contain very important part buffers [5] which are having own advantages and disadvantages. Keeping all this in mind it is required to design a router with optimum performance , [8] discuss that power, area[7] , and performance of the NoC architecture are tightly integrated with the design and optimization of the link, router (buffer and crossbar), and topology.

In all the router architecture discussed so far suffered from drawbacks like more space utilized for buffers, low power but at the cost of more area. So in our work we try to get optimum performance by efficiently using buffers and by using modified error detection techniques.

III. APPROACH AND MOTIVATION

In this work, the proposed design is a new smart reliable dynamic router for NoC.

Our approach includes using FIFO for low area, low power and due to the FIFO logic used in the routing logic, which makes router to achieve better than the existing router. As well as low overhead.

IV. PROPOSED ARCHITECTURE

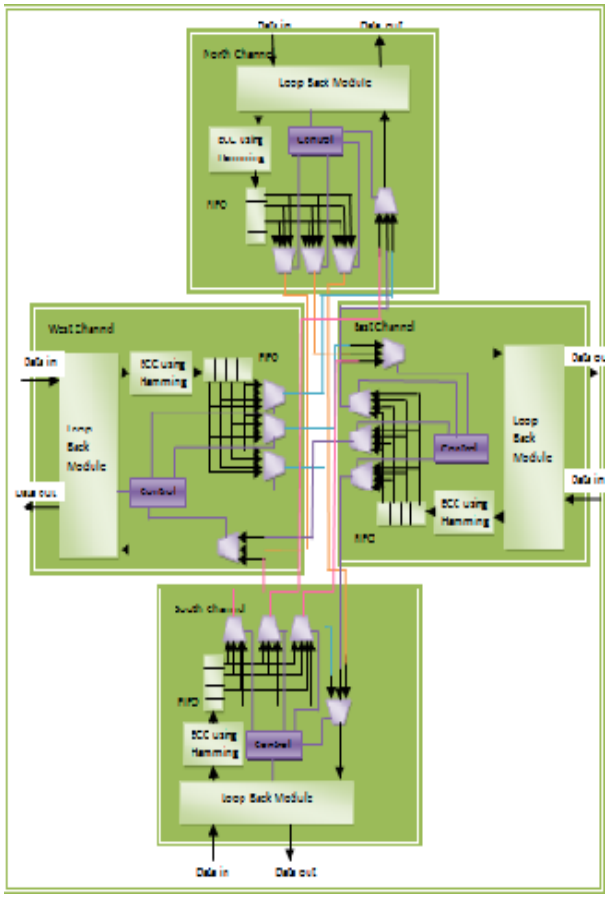

Fig. 1. Architecture of proposed router switch

The proposed architecture is modified version of router switch[2] by C.KILLIANS. The proposed one will overcomeme both dead and live locks. The figure of the modified router switch is shown in fig 1. This switch is appropriate for 2-d mesh NoC, with four directions (north, south, east, and west) and the PES and IPS can be connected directly to any side of a router. There is no need for specific connection port for a PE or IP. Each port direction is composed of two unidirectional data buses (input and output ports).The proposed algorithm having no of blocks, they are loopback module, Control Logic, ECC using hamming, F.I.F.O buffer.

A. DIFFERENCES BETWEEN PROPOSED AND ORIGINAL [2] ARCHITECTURE

In the proposed work Loop Back module is designed as old one, FSM is removed and Routing Error detection, Logic, centralized Journal of data Packet is removed, as our loop back module itself does the same functionality. Buffers are also removed, instead of FIFO is used to achieve better performance.

B. F.I.F.O

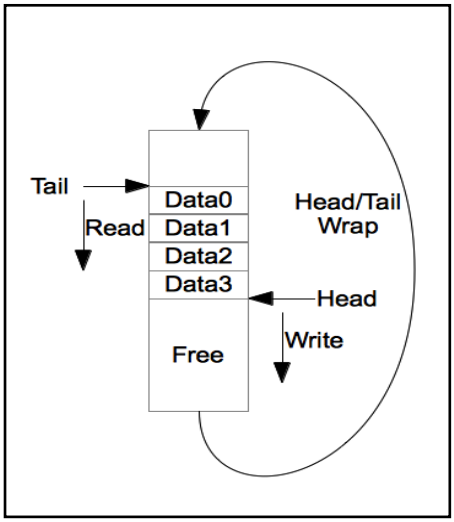

Fig.2. F.I.F.O Block Diagram

A FIFO buffer stores data on a first-in, first-out basis. The storage structure is typically an array of contiguous memory. Data is written to the “head” of the buffer and read from the “tail”. When the head or tail reaches the end of the memory array, it wraps around to the beginning. If the tail runs in to the head, the buffer is empty. But if the head runs in to the tail, the implementation must define if the oldest data is discarded or the write does not complete. In the example below, data is never discarded. FIFOs are a storage mechanism which operates on a first-in, first-out basis. They are useful for managing the arrival of asynchronous data.

C .LOOPBACK MODULE

A loopback module block[2] is used for altermate path for packets by looping back through another port.This happens when neighbour router to which data is supposed to be sent is found faulty by present router.Since it is a reconfigurable NoC, position and number of components

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in the network can change during the reconfiguration time. During reconfiguration, ell as faulty routers are made isolated from non faulty routers. If it is not done, data packet may get lost and never reaches its destination. To solve this problem there come loopback module which is associated with the router architecture contain output buffer. The work of loopback module is to empty the buffers of loopback module for each output port by looping back the data packet in to the input port of the router [2]. Then looped back packets are rerouted towards another output port of the router. The loopback module avoids data packet getting trapped or data packet loss. A loopback module is implemented in each of the four ports of the router. The architecture of the loopback module is depicted in Fig. 3.[2]

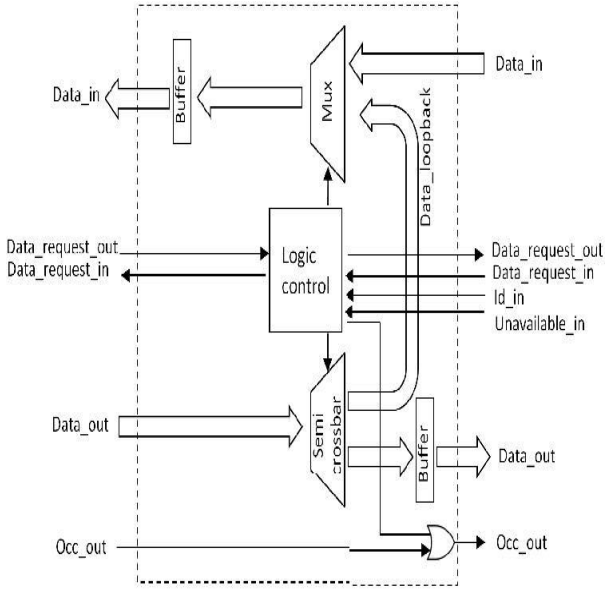

Fig.3. Loop Back Module [2]

D. E.C.C USING HAMMING CODE

In this work we have used modified hamming code [10] to reduce area than the normal hamming code.Error in data can be easily find out and retrieved back by using the reference parity bit associated with the original data bit. This method is composed of a Transmit matrix.

The Transmit matrix is a combination of an identity matrix and a parity matrix. The input data (8-bits) is multiplied and with the identity matrix and this data bits are encoded and sent to the next router along with the parity bits. By using the parity matrix the received code word is decoded and hence the original data can be retrieved back.

The decoder and encoder circuit structure is formed from the Transmit and Parity matrix. The encoding process is done with the help of Transmit matrix multiplied with the original data. The output of this is associated with the parity bit for the encoding reference. This method is carried out by Xor gate for each row of Parity matrix. Fig.4 and 5 show RTL view of hamming encoder and hamming decoder.

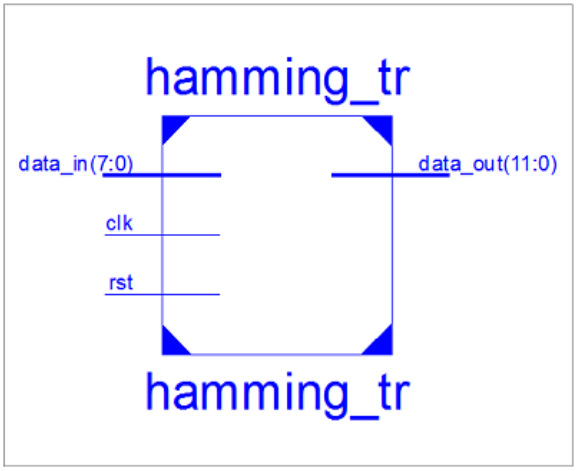

Fig.4. Hamming Encoder

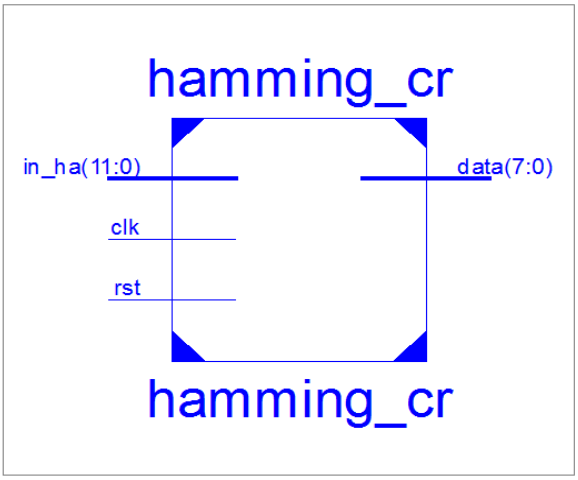

FIG.5. Hamming Decoder

E. CONTROL LOGIC:

In addition to this physical connection infrastructure, the router also contains a logic block that implements the flow control policies (routing, arbiter, etc.) and defines the overall strategy for moving data though the NoC.

A flow control policy characterizes the packet movement along the NoC and as such it involves both global (NoC-level) and local (router-level) issues. One can ensure a deadlock-free routing, for instance, by taking specific measures in the flow control policy (by avoiding certain paths within the NoC for example). Also, the optimization of the NoC resources usage (channels, bandwidth, etc.) and the guarantees on the communication can be ensured as part of the flow control policy (for instance, by choosing a routing algorithm that minimizes the path or by implementing virtual channels to reduce congestion, etc.). The routing algorithm [6] (should avoid deadlock and livelock) is the logic that selects one output port to forward a packet that arrives at the router input. This port is selected according to the routing information available in the packet header.

According to XY routing algorithm Fig.6. That we use in paper.

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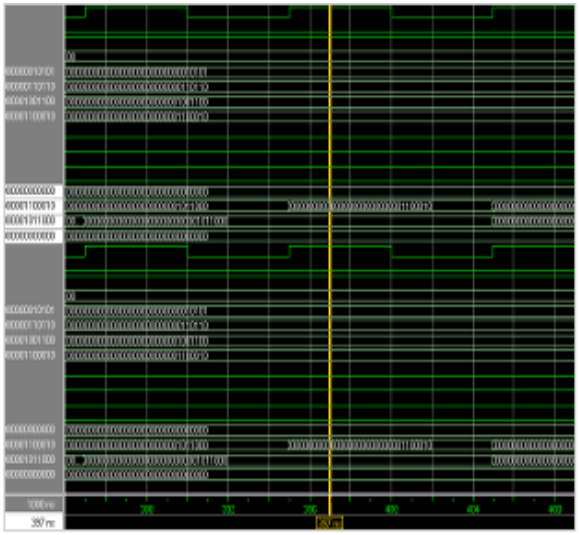
Algorithm Condition	Direction Selected
X destination < X previous	NORTH
X destination > X previous	SOUTH
Y destination < Y previous	WEST
Y destination > Y previous	EAST

Fig.6. XY Routing Algorithm

V. RESULTS

A. SIMULATION OF TOP ROUTER



Fig,6.. Simulation of Proposed Router

Fig.6. shows the simulations of proposed router, It is seen that all then, N, S, W, E modules send a data packet simultaneously and similarly receive the data packets simultaneously. It is also observed that all the data packets do not make any loopback and bypass as there is no fault present. Here it is showimg that the data is input in four directions and after routing data is out from four directions N,S,E,W according to XY algorithm.

B. RTL VIEW OF PROPOSED ROUTER

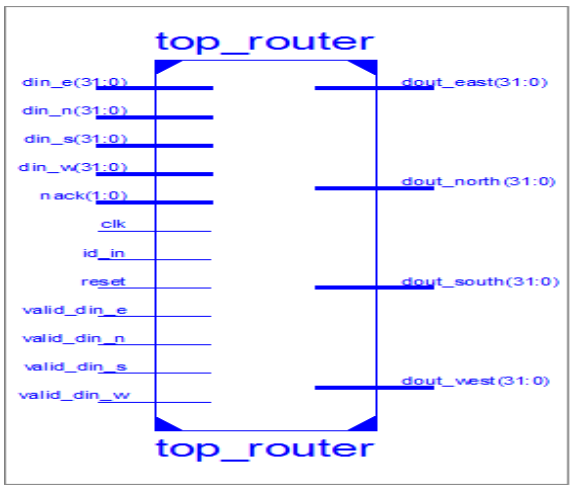


Fig .7. Top Level Architecture

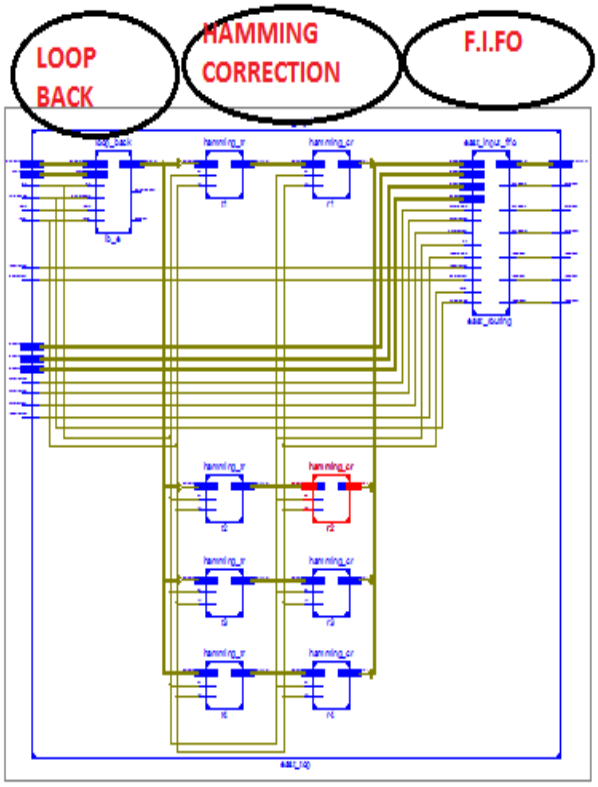


Fig.8. RTL view of Top Router

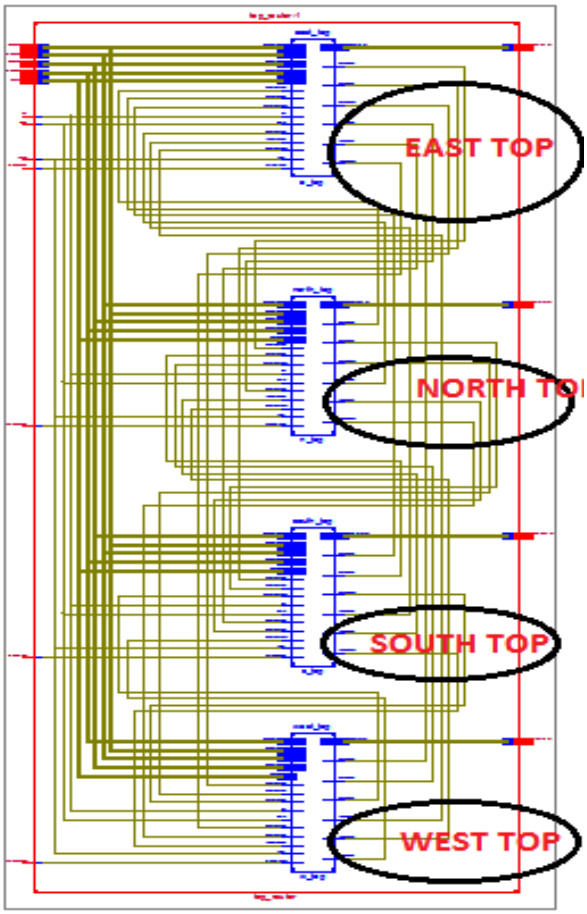


Fig.9. RTL view of EastTop Router

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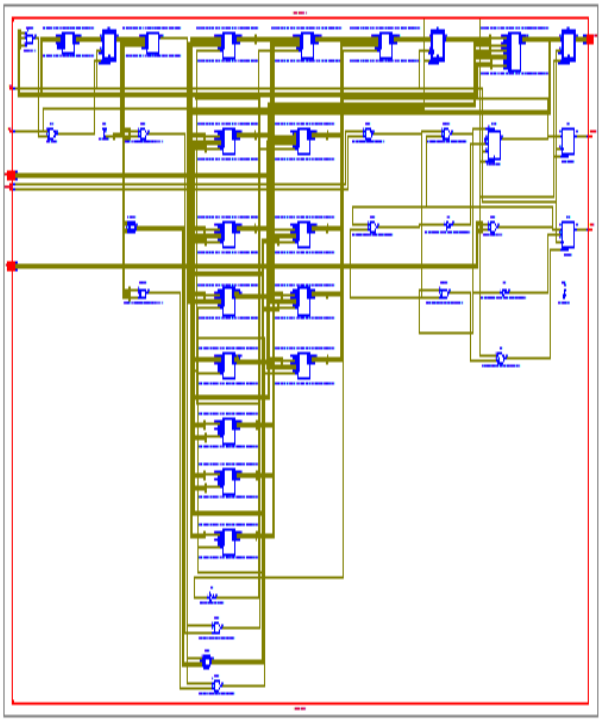

Fig.10.. RTL view of Loopback of EastTop Router

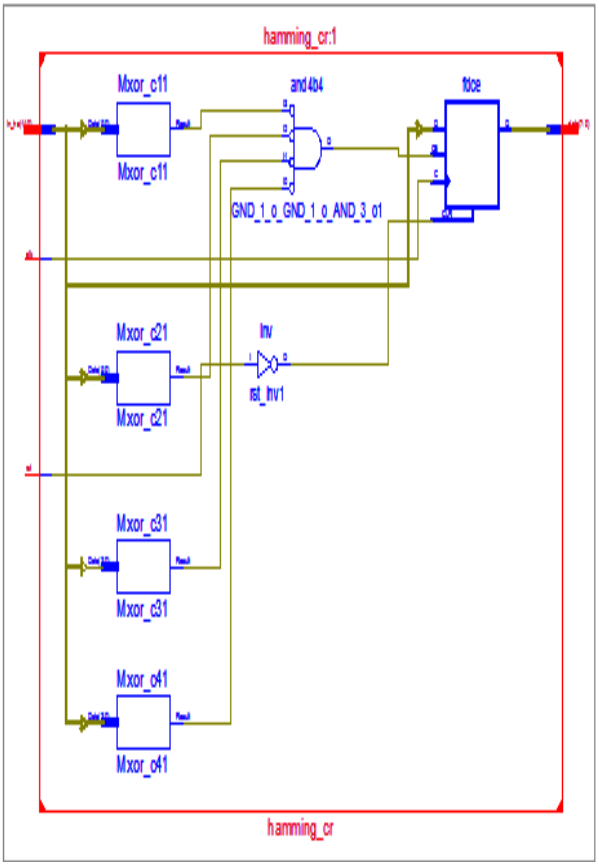

Fig12.. RTL View of Hamming Decoder of East Top

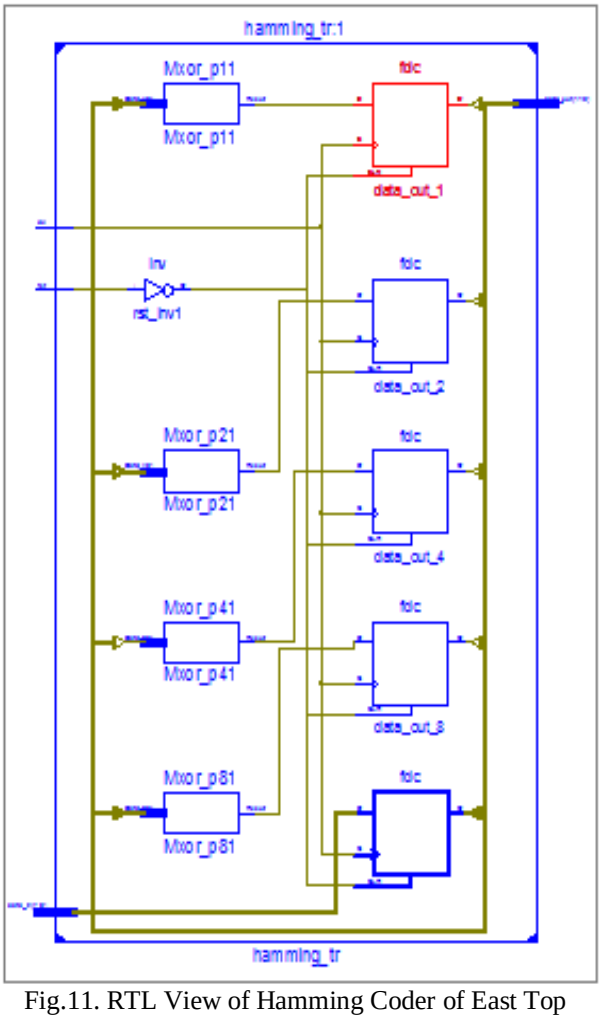

Fig.11. RTL View of Hamming Coder of East Top

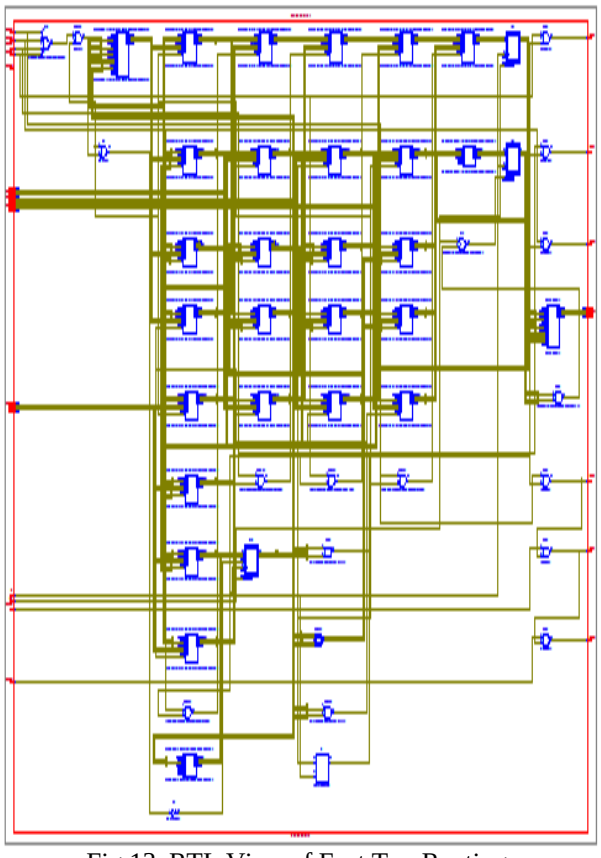

Fig.13. RTL View of East Top Routing

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C. DELAY

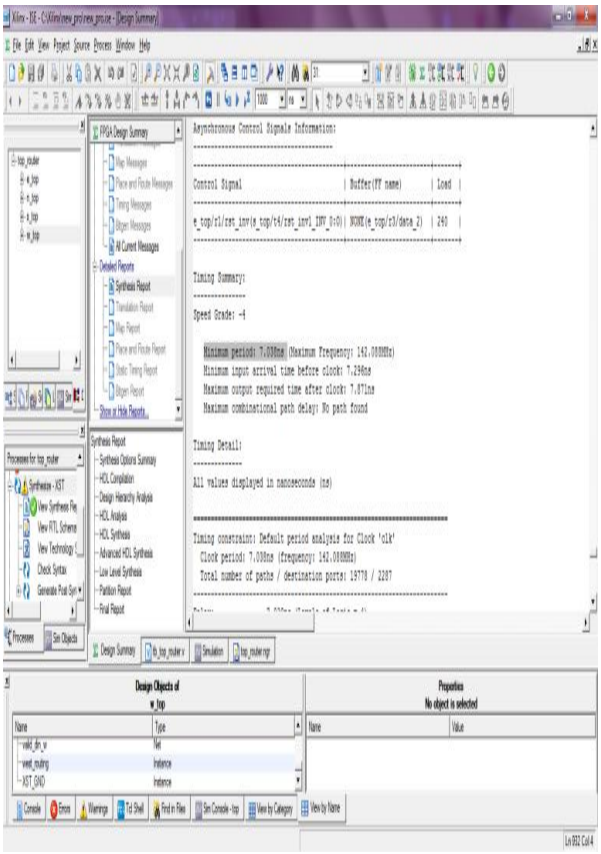

Fig.14. Total Delay

D. FREQUENCY

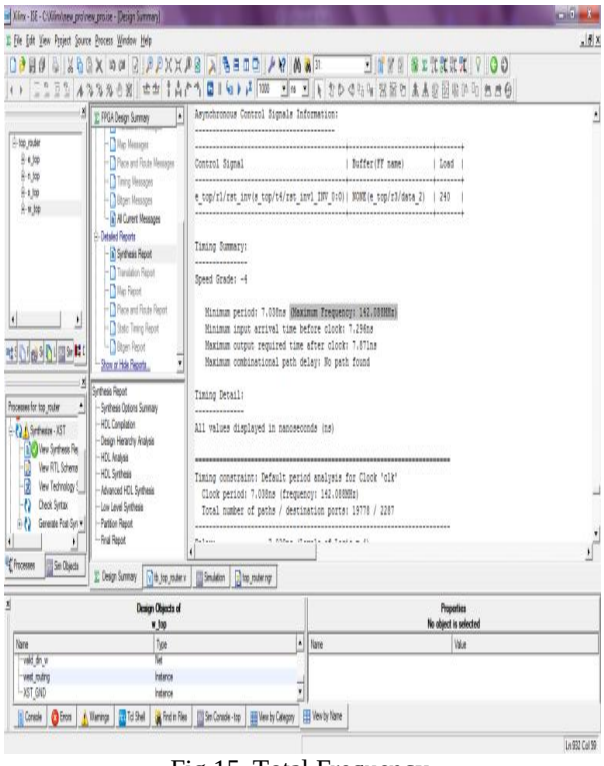

Fig.15. Total Frequency

E. AREA UTILISED

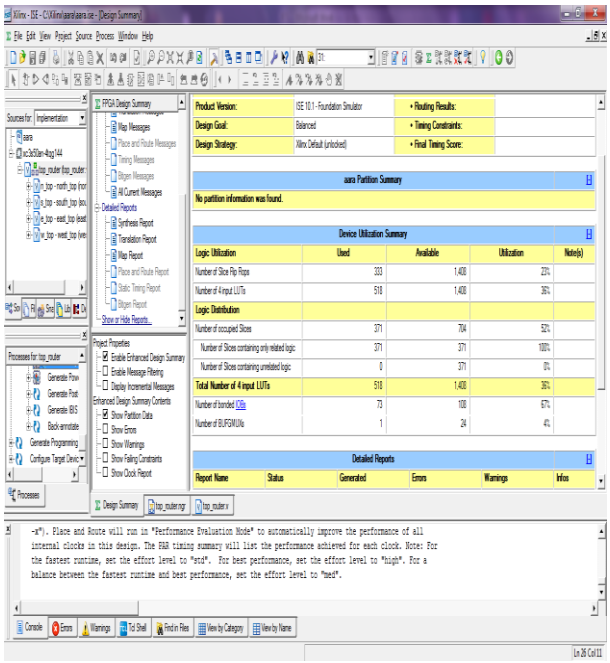

Fig16. Area utilized of Proposed RKT switch

F. POWER REPORT

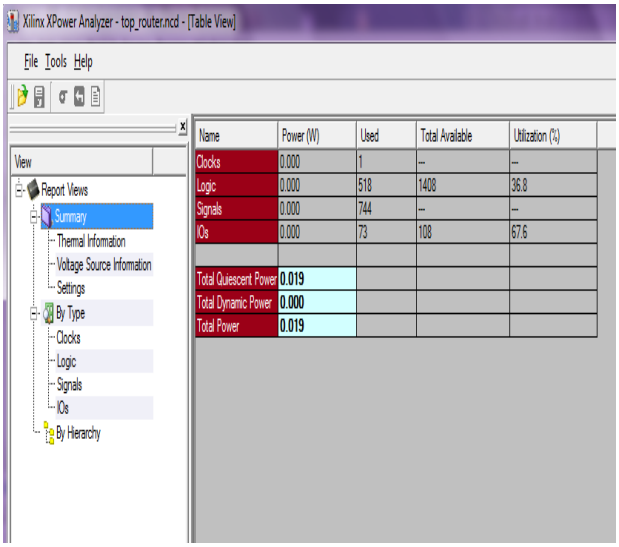

Fig. 17. Total Power Delay

VI. CALCULATIONS

The proposed reconfigurable router is simulated and synthesized using Xilinx ISE tool. Fig.2 gives the synthesis results in terms of Slices Registers, Slices LUTs and maximal working frequency for 32 data bus size. It is seen from synthesis result of Fig. That the 32-bits Router-Switch require 330 Registers, 518 LUTs and can operate up to 142.08 MHz on the XYLINX tool. This gives a low area when we compare it with original router results [9] which states that the 32-bits original RKT-Switch requires 4340 Registers, 6542 LUTs and can operate up to 459.6

MHz.. Moreover, an estimation of the power consumption of 0.019 W is given through the Xilinx XPower Estimator tool if Fig.22. The results explicits that our proposed architecture shows better performance in terms of area and low power consumption. Low area is directly proportional to decrease in latency.

VII.CONCLUSION

Hence our modified and optimized RKT is comparatively Low Area, Low Power; and due to the FIFO logic used in the routing logic, which makes router to achieve higher performance than the existing RKT. as well as low overhead.Low area is responsible for low latency .

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