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Design of optimized Proposed 9T SRAM Cell

Tejashwanth Polavarapu[1], Sai Krishna D[2], R Manikant Reddy[3], Sai Shreya Madabhushi[4]

GITAM University, Hyderabad, India[1,2,3,4]

Abstract: For SRAM power, stability, delay and area are the major concerns. And they are trade-offs to each other. But all are important and should be in acceptable range. In this paper we mainly concentrated on power and stability and we designed an optimized proposed 9T-SRAM for low power consumption by placing an NMOS transistor between supply voltage V_{DD} and the latches formed by cross coupled inverters. This NMOS transistor is in diode connected mode and it scales down the V_{DD}. So total power is reduced by 98%. Because power is directly proportional to square of V_{DD}. But this effect the stability, as stability decreases when supply voltage decreases. In order to increase stability an extra PMOS transistor is placed in between access transistor and pull down transistor. This PMOS transistor separate's the storage node and writing node of data. It also scales the bit line voltage and prevent the flipping the contents of cell at low voltages. So stability parameters like SINM, SVNM, WTI and WTV also increased by 93%, 45%, 86% and 56% respectively. In this proposed cell static power is also reduced by 55% due to stacking effect. This all values are when compared with Sub-threshold 10T SRAM cell. This proposed circuit is also tested by giving 0.3 V power supply. Cadence Virtuoso tools are used for simulation with gpdk-90nm CMOS process technology.

Index terms: SRAM, SINM, SVNM, WTI, WTV.

I INTRODUCTION

The usage of digital memory's increasing very much and the there is no digital system without memory [1]. For example to store program instructions, initial values, intermediate data results etc. The usage of battery operated devices and portable electronics devices are also increased very much. In order to increase the battery life of devices we should concentrate on power consumption and power dissipation of the device [2]. The memory present in the device also contributes to the power consumption or dissipation of it, mainly SRAM (Static random access memory) which is used as cache memory.

For SRAM we have to give continuous power supply to each SRAM cell in order to hold the data in it. Because of this the power dissipation in SRAM is very large. To reduce the power dissipation the supply voltage is scaled down to a great extent. Along with supply voltage, threshold voltage also reduced to increase the performance but it exponentially increases the subthreshold leakage current which leads to increase power dissipation in standby mode.

$$I_{subthresho\quad ld} = I_0 e^{\frac{V_{gs}-V_{th}}{\eta V_T}}\left(1 - e^{\frac{-V_{ds}}{V_T}}\right) \qquad (1)$$

Where $I_0 = \left(\frac{W \mu_0 c_{0x} V_T^{\,2} e^{1.8}}{}\right)$, $V_T = \frac{KT}{q}$ is the thermal voltage, V_{ds} and $V_{gs}$are the drain to source and gate to source voltage respectively. $V_{th}$is the threshold voltage. C_{ox} is the gate oxide capacitance, μ_0 is the carrier mobility and η is the sub-threshold swing coefficient [3].

Along with the static power dissipation the stability of the SRAM cell decreases with scaling of supply voltage. So a conventional 6T cannot give reliable results at voltages as low as threshold voltage [4]. Therefore there is a need for designing a robust SRAM cell which operates at such low voltages and dissipates less static power. To achieve this we design a SRAM cell with different structures.

II CONVENTIONAL 6T SRAM CELL

In conventional 6T SRAM cell as shown in figure 1, there are two NMOS transistors N1 and N2 which acts as driver transistors and two PMOS transistors which acts as load transistors. These four transistors combine and form cross coupled inverters to store and force values continuously to each other. N3 and N4 act as pass transistors and called as access transistor which helps to write data from bit lines to node Q and QB. Modes of working [5].

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A. Write mode:
To write the data in to the cell we first enable write line (WL). Then for writing '1' pass '1' to bit line (BL) and '0' to bit line bar (BLB). As WL enabled N3 and N4 are ON and pass data through them. This data is stored at node Q and QB as '1' and '0' respectively. After writing the data WL line is disabled. To write '0' we pass '0' to bit line (BL) and '1' to bit line bar (BLB).

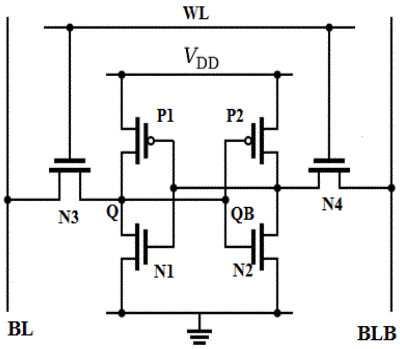

Fig. 1 Conventional 6T SRAM cell

B.Hold mode:
In hold mode WL remains disabled and disconnects the cell from bit lines. Cross coupled inverters force values continuously to each other and stores the written data at Q and QB nodes.

C.Read mode:
To read the stored data from the cell, first pre-charge both the bit lines to '1' and then enable WL. If stored data is '1' then N1 is OFF and N2 is ON. Pre-charged BL line has no path to ground, so it remains as '1' at node Q and pre-charged BLB is discharged through N4 and N2 to ground, so it reads '0' from node QB. If stored data is '0' then N1 is ON and N2 is OFF. BL discharged through N3 and N1 to ground, so it reads '0' from node Q.

III SUB-THRESHOLD 10T SRAM CELL

In this structure we have four access transistors N1, N2, N3 and N4. Two word lines WL2 and WL. And a control signal VGND [4] as shown in figure 2.

A. Write mode:
In this mode both WL2 and WL are enabled to pass data from bit lines to cell node. VGND signal line is connected to V_{DD} to compensate the problem of threshold drop due to two series access transistors. Here positions of BL and BLB are exchanged because of the cell structure. To increase the write ability the two word lines can be boosted but it effect the read stability as they both are inversely proportional.

B. Hold mode:
In this mode both WL2 and WL are disabled and VGND is connected to V_{DD}.

C. Read mode:
In this mode WL2 is disabled and WL is enabled due to this the storage nodes are disconnected from bit lines and the read noise margin increases. VGND is connected to ground to form a discharging path from bit line through node storing '0' to ground.

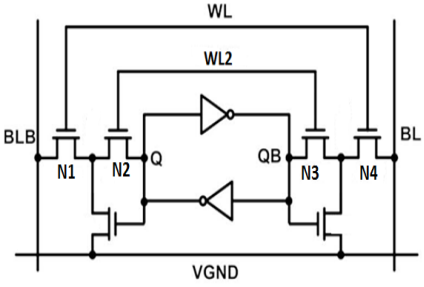

Fig. 2 Sub-Threshold 10T SRAM cell

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IV PROPOSED 9T SRAM CELL

In our proposed 9T SRAM cell there is a diode connected NMOS (N5) as shown in figure 3.This NMOS scales the V_{DD} which reduces the dynamic power to great extent as [6]

$$P = \alpha F C V_{DD}^2 \qquad (2)$$

Where, α = switching factor, F = frequency, C = capacitance, V_{DD} = supply voltage.
The stability of cell is decreased due to scaling of V_{DD} because there is probability of flipping the contents of storage nodes because of pre-charged bit lines while read operation (mainly when cell operating at very low supply voltages).
The stability decreased due to scaling of V_{DD} is compensated by the extra PMOS transistors P3 and P4 which are always ON are added in between driver and access transistors. This structure increases the read stability [7]. For example while reading '1' QN is at '1' and QNB node is at '0'. When WL is enabled the voltage divided in series along N4 access transistor, P4 conducting PMOS and N2 driver transistor suppress rising of QNB voltage to V_{DD}-V_{TN4}-$|V_{TP4}|$, Where V_{TN4} and V_{TP4} are threshold voltages of N4 and P4 respectively. So this suppressed voltage cannot flip the contents of cell. While writing the data if node QN is at '1' and QNB is at '0' to write '0' at node QN, BL is connected to ground and BLB is raised to V_{DD} and WL is enabled. The node Q changes from V_{DD} to '0' and node QNB is discharged from '1' to '0' state. The node QN cannot be dropped below $|V_{TP3}|$ because PMOS is not perfect passer of '0'. But falling of QN causes P2-N2 inverter to trigger and cross coupled inverters bring flip of state.

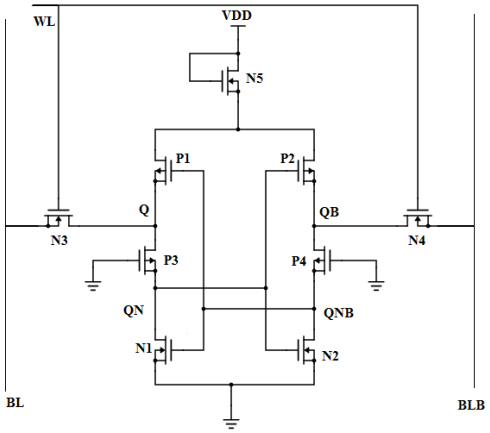

Fig. 3 Proposed 9T SRAM cell

The static power dissipation is also reduced due to stacking of MOSFETS (PMOS, PMOS and NMOS).The working modes of proposed SRAM are same as conventional 6T SRAM cell.

V RESULTS AND DISCUSSION

A. Transient response:
Here we discuss the transient response of above explained cells. This shows the write and hold modes of SRAM cell.

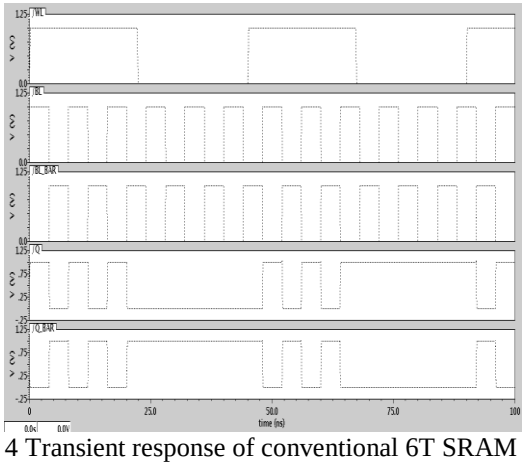

Fig. 4 Transient response of conventional 6T SRAM cell.

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When WL signal is high, the data on BL and BLB are written into the storage nodes Q and QB respectively. And when WL signal is low the Q and QB nodes store the recent written data before WL going to low as shown in fig. 4,5 and 6.

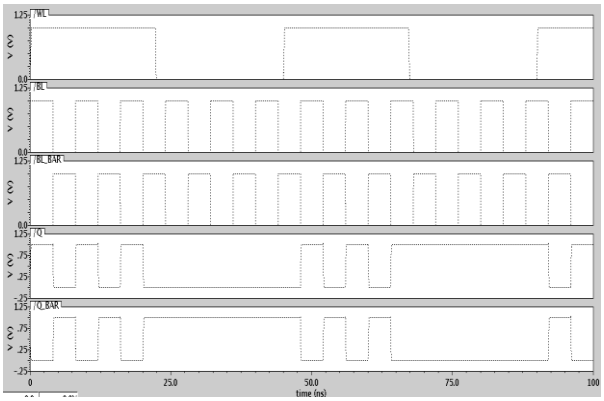

Fig. 5 Transient response of Sub-Threshold 10T SRAM cell.

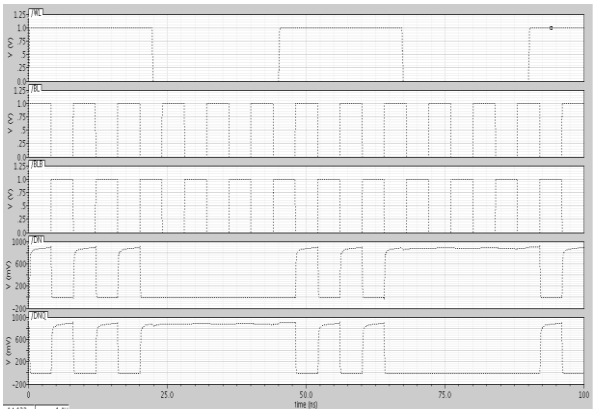

Figure 6.Transient response of proposed 9T SRAM cell.

In proposed 9T SRAM cell the data at Q and QB are not reached to 1V because of the threshold drop of diode connected transistor as shown in figure 3. But it doesn't effect the reading of data because differential sense amplifier is used while reading the data from SRAM cell.

B. Static and Total power dissipation:

Plots of Static and Total power dissipation of above explained SRAM cells are shown in fig. 7,8,9,10,11,12 and 13.

Static power dissipation of proposed cell is reduced by 55% due to decrease in leakage currents because stacked transistors share the same leakage currents from top to bottom which reduces V_{DS}[8]. Total power of proposed cell is reduced by 98% because both Static and Dynamic power is reduced.

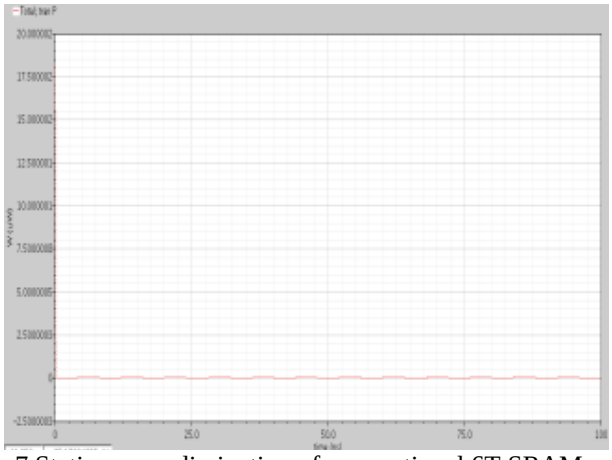

Fig. 7 Static power dissipation of conventional 6T SRAM cell.

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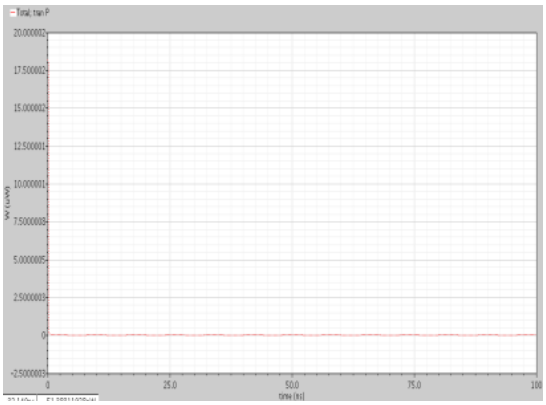

Fig. 8 Static power dissipation of Sub-Threshold 10T SRAM cell.

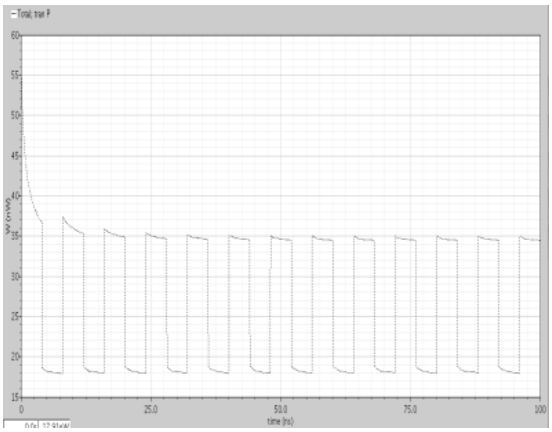

Fig. 9Static power dissipation of proposed 9T SRAM cell.

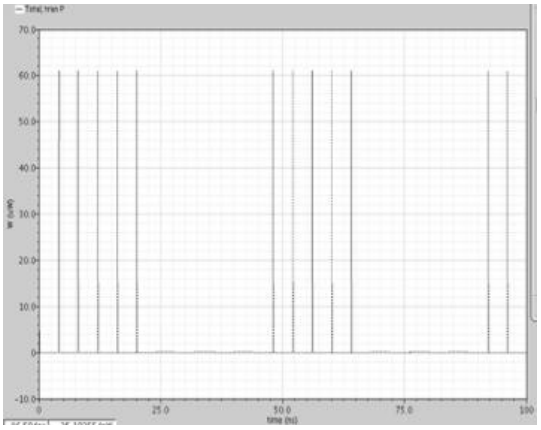

Fig. 10Total power dissipation of conventional 6T SRAM cell.

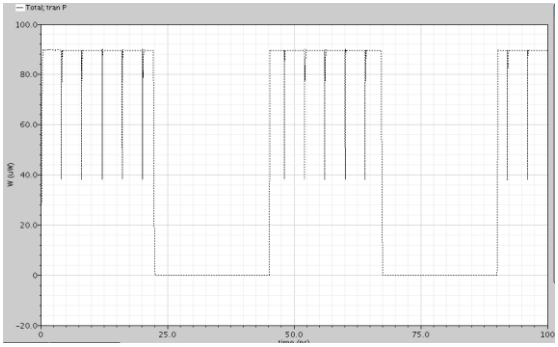

Fig. 11 Total power dissipation of Sub-Threshold 10T SRAM cell when VGND = V_{DD}

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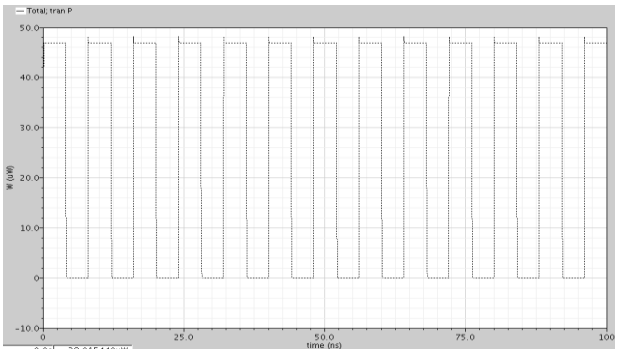

Fig. 12 Total power dissipation of Sub-Threshold 10T SRAM cell when VGND = GND

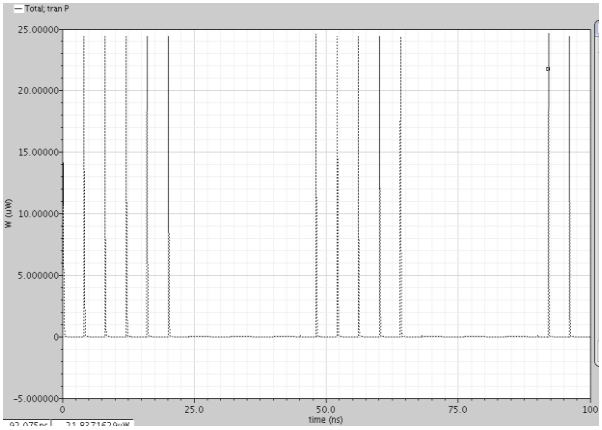

Fig. 13 Total power dissipation of proposed 9T SRAM cell.

TABLE I Comparison table of Static and Total power dissipations

Power dissipation	6T SRAM	Sub-threshold 10T SRAM	Proposed 9T SRAM
Static	65.7n	60.8n	27.1n
Total	0.234u	18.41u	0.236u

C. Stability analysis:

Here stability parameters like Static Current Noise Margin (SINM), Static Voltage Noise Margin (SVNM), Write Trip Current (WTI) and Write Trip Voltage (WTV) are calculated using N-curve analysis [9][10].

Pull Up Ratio (PUR) and Cell Ratio (CR) [10] are kept '1'. The conventional 6T SRAM cell can't give reliable stability values for this CR and PUR as shown in fig. 14.

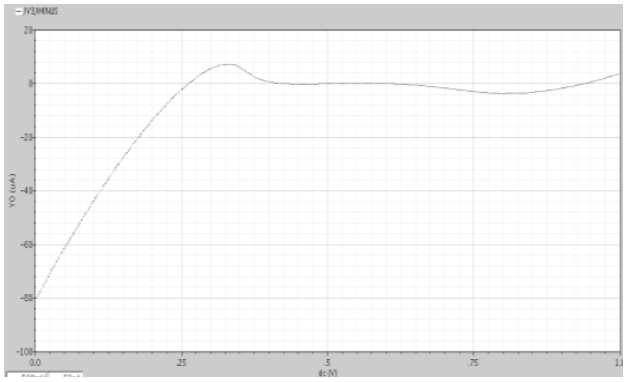

Fig. 14 N-curve analysis of conventional 6T SRAM cell

N-Curve should cross X-axis only at three points but in-case of 6T SRAM cell it crossed four times which indicates that the cell is not stable. Stability parameters are calculated for Sub-Threshold 10T cell and Proposed 9T cell and results are noted in table II.

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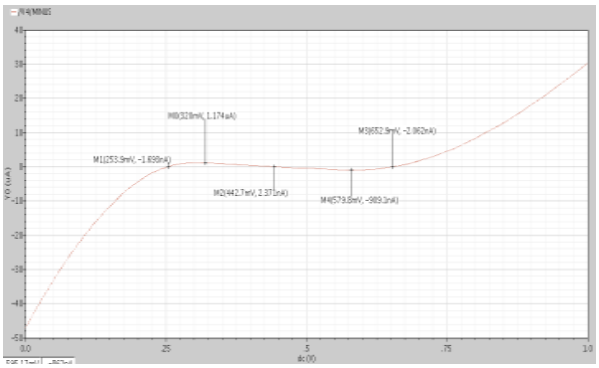

Fig. 15 N-curve analysis of Sub-Threshold 10T SRAM cell

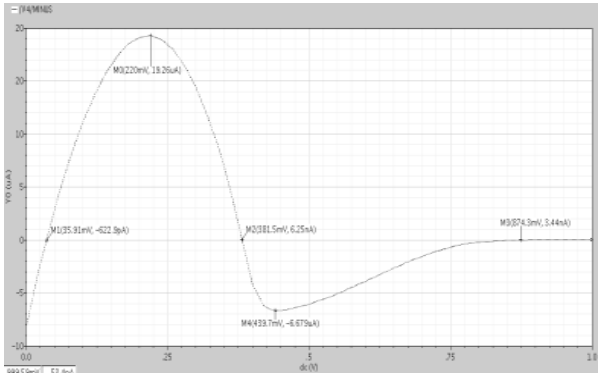

Fig. 16 N-curve analysis of proposed 9T SRAM cell

TABLE II Comparison results of SINM, SUNM, WTI and WTV

	6T SRAM	Sub-threshold 10T SRAM	Proposed 9T SRAM
SINM	-	1.17	19.26
SVNM	-	188.5	345.59
WTI	-	0.90	6.68
WTV	-	210.5	489.4

VI CONCLUSION

In this paper designed an Optimized 9T-SRAM for low power consumption by reducingtotal power by 98% and static power by 55% than the Sub-Threshold 10T SRAM cell. And total power is increased by 0.8% and static poweris reduced by 58% than the conventional 6T SRAM cell. Stability parameters like SINM, SVNM, WTI and WTV also increased by 93%, 45%, 86% and 56% respectively when compared to Sub-Threshold 10T SRAM cell.The benefits of proposed SRAM cell is not having any extra control signals, so it can be directly replaced in place of conventional 6T SRAM cell. Area is also not a concern, even though three transistors increased. Because a conventional 6T SRAM can't give stable values at low voltage operations. For 6T SRAM to work at this lower voltageswe have to increase cell ratio and pull up ratio which ultimately increases the area of 6T SRAM cell.This proposed circuit is also tested by giving 0.3 V power supply and it gave reliable stability values.

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