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Design of High-Speed and Low Power Carry Skip Adder

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Abstract: In this paper we present high speed 8-bit Carry Skip Adder (CSA) compared with Ripple Carry Adder (RAC) and conventional Carry Skip Adder (CSA). This is more efficient in terms of power consumption, area usage and speed. Instead to make multiplexer logic, the propose architecture made of AND-OR-Inverter (AIO) combination gate for carry skip adder. The propose architecture are evaluated by comparing their speed, power and area with those of other address using 180nm, 90nm and 45nm static CMOS technology.

Keywords: Ripple Carry Adder (RCA), Carry Skip Adder(CSKA), CI-CSKA, high performance, incrimination.

I. INTRODUCTION

The main component of arithmetic logic unit (ALU) is adder which has capability to reduce the power consumption and increase their speed .These factor also effect the speed and power consumption of microprocessor. The power and performance along with dynamic voltage and frequency which depend on the supply voltage have become the motivation for the designing of circuit. This circuit consist of a system which may change the voltage and frequency of the circuit to reduce the power consumption. The power consumption of digital circuit is reduce by many method but most effective technique is to reduce the supply voltage due to the quadratic dependence of the switching energy on the voltage .The main leakage component in OFF device in the threshold current which has exponential dependency on the supply voltage level through the drain-induced barrier lowering effect. The ON device operation may present in the super-threshold, near-threshold, or sub-threshold region. When the working in the supper-threshold region lower delay and higher switching and leakage power are produced compared with near/sub-threshold regions, if the circuit operates in the sub-threshold region ,cause a large delay for the circuit with a small change in the sub-threshold current. Along with the knob of the supply voltage different adder structures/families can be chosen for speed and power optimization. Example including ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSA).

II. PRIOR WORK

In this paper the main focus on to reduce the carry propagation delay in RCA. The RAC is to consider to be a simplest adder with smallest area and power consumption but with the worst critical path delay .The speed, power consumption and area usages are considered to be larger than those of RCA for CSKA.

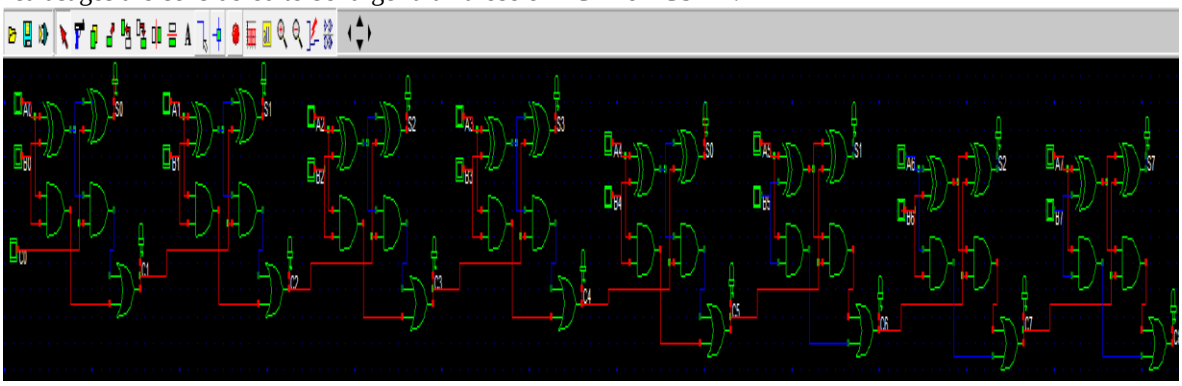

Fig. 1 8-bit ripple carry adder (RAC)

The conventional structure of ripple carry adder is made of simple full adder in which carry out off each full adder is the carry in of the succeeding next most significant full adder. The N cascaded FAs of an RAC, the worse propagation delay calculated by the summation of two N-bit numbers, A and B belong to logic there by the FAs are in the propagation mode. It mean that the worse case delay belong to the propagation mode

Pi=Ai X-OR Bi=1 for i =.....N

Where Pi is the propagation signal related to Ai and Bi. This shows that the delay of the RAC is linearly related to N. In that case, a group of cascaded FAs is in the propagation mode, the carry output of the chain is equal to the carry input. The diagram of 8-bit ripple carry adder is shown in figure 1.Critical path delay is generated by 8-bit ripple carry

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is 34.00ns this delay is calculated between input A0 and output C8 as shown in figure 2. This graph is drawn between voltage vs time, time scale is consider as 200ns.

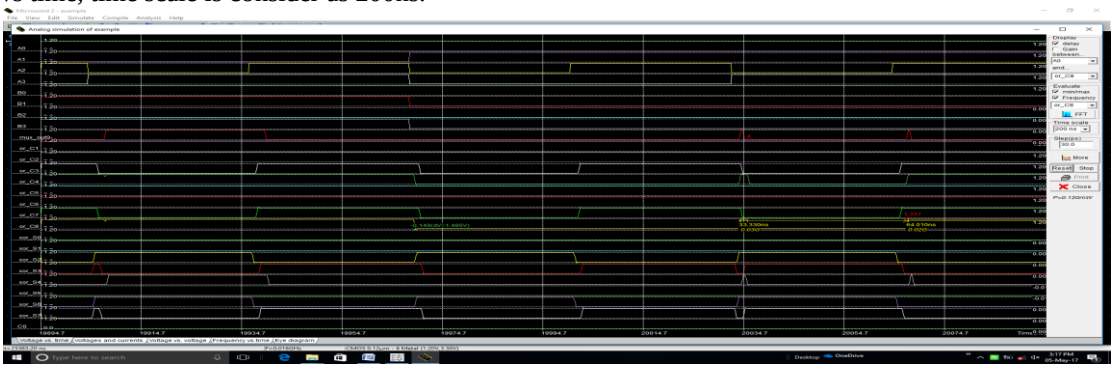

Fig. 2 Carry propagation delay of 8-bit ripple carry adder (RAC)

The CSKA, which is efficient adder in terms of power consumption and area usage and the critical path delay of the CSKA adder, is much smaller than the one in RCA, where the area and power consumption is similar to those of the RAC. The structure of 8-bit conventional CSKA, which is based on the Ripple carry adder logic as shown in figure 3 .A chain of full adder along with 2:1 multiplexers (Carry skip logic) is present in form of stage in the conventional structure of CSKA. 2:1 multiplexer can be used to connect RAC block and can be placed into one more level structure.

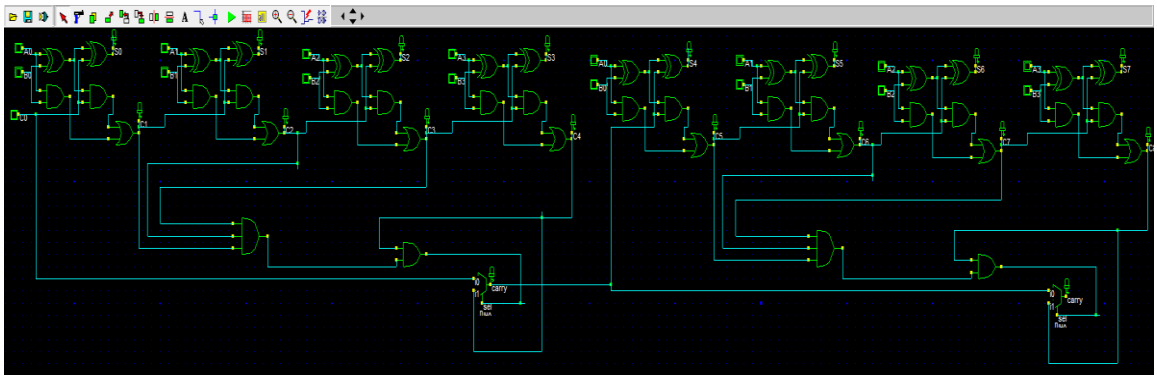

Fig. 3 8-bit carry skip adder (CSKA)

The CSKA configuration (i.e., the number of full adder per stage) has a great impact on the speed of this type of adder. We can compare between figure 2 and figure 4 the carry propagation delay of carry skip adder is less as compare ripple carry adder .carry propagation delay of carry skip adder is 8.00ns as shown in figure 4.

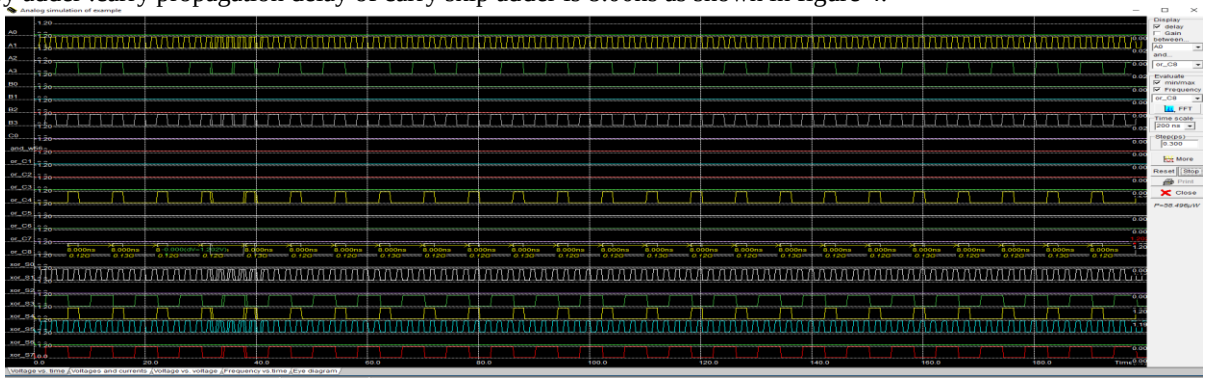

Fig. 4 Carry propagation delay of 8-bit carry skip adder (CSKA)

III.PROPOSED CSKA STRUCTURE

As per the discussion made, the propagation delay of the CSKA can be lowered by reducing the delay of the skip logic for the reducing of delay, a modified CSKA structure has been presented in this paper.

The propose structure comprises of concatenation and the incrimination scheme with the conv-CSKA structure, which can be denoted by CI-CSKA. The ability to use simple carry skip logic can be represented from the propose structure. As 2:1 multiplexer have more delay, area and low power consumption they can be replaced with AOI/OAI compound gate(figure 5).As the carry propagate through the skip logic, it can be complemented.

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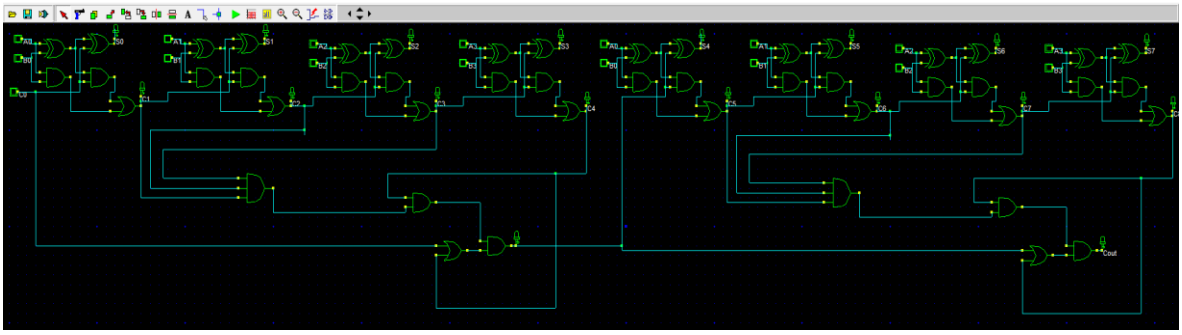

Fig. 5 8-bit Proposed CI-CSKA structure

The complemented carry can be generated at even stage skip logic's output. compressed with the conventional one ,the propose structure has lower propagation delay with a small area .Note that while that power consumption of the AOI or OAI gate are smaller than that of multiplexer. The internal structure of CI-CSKA is shown in figure 5.

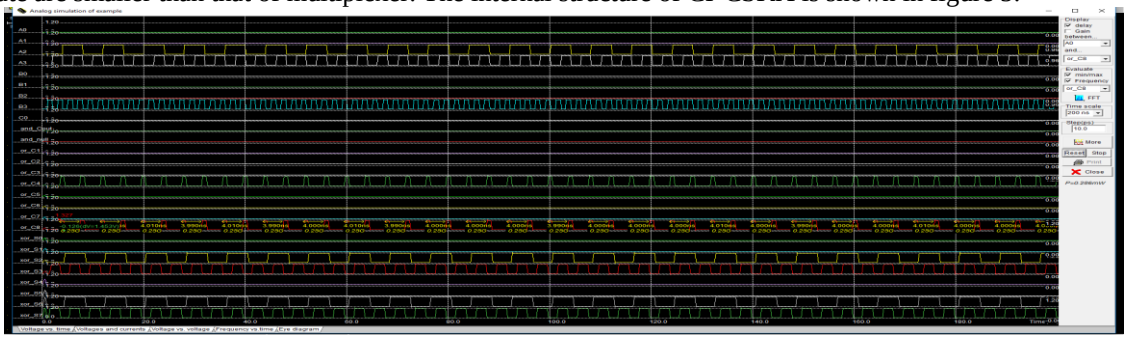

Fig. 6 Delay of CI-CSKA structure

By the use of the static AOI and OAI gates (six transistors) measure with the static 2:1 multiplexer (12) transistor, causes to reduce in the area and delay of the skip logic. As shown in figure 6 the delay generated by CI-CSKA is 4ns as shown in figure 6, it is just half of delay generated by CSKA. In addition, except for the first block of RCA, the carry input to all other block is zero, and for the other blocks, we can also the change the first adder cell in the RCA chain is a HA. So that FAs in the conventional structure are change with the same number of HAs in the propose structure decreasing the area uses and delay of the skip logic. These incrimination blocks may be implemented with the same logic gate as those use for generating the select line of the multiplexer in the conventional structure. Therefore, the area usage of the proposed structure of CI-CSKA decreased compared with that of conventional one. The critical path of the proposed CI-CSKA structure shown in figure 6 .

IV. RESULTS

In this section , we assess the efficacies of the proposed structures by comparing their delays, power, and area with those of some other adder .All the adder are considered here had the size of 8-bit and were designed, simulated and synthesize using a 180nm, 90nm and 45nm technology. The simulations and synthesis were performed using microwind tool environment. Table 1 reports the Technology, Power and Delay usages of 8-bit of RCA, CSKA, CI-CSKA adder structures.

TABLE I COMPARISON OF DIFFERENT TECHNOLOGIES, DELAY AND POWER OF RCA, CSKA AND PROPOSED CI-CSKA

S.NO.	Design	Technology (nm)	Delay (ns)	Power (µw)
1	RCA	180	64 ns	120 µw
		90	60ns	150 µw
		45	60ns	167 µw
2	CSKA	180	08ns	58 µw
		90	05.98ns	57 µw
		45	05.0ns	37 µw
3	CI-CSKA	180	04.0ns	26 µw
		90	2.48ns	25.56 µw
		45	1.89nsI	23. µw

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V. CONCLUSION

A static CSKA structure called CI-CSKA was proposed in this paper, which present the high speed and lower power utilization estimated with those of conventional one. By modified the structure with concatenation and incrimination techniques, the speed enhancement was achieved.In addition, AOI and OAI compound gate were utilized for the carry skip logics. Again, the recommended structure presented the lowest delay and PDP making itself as a better candidate for high-speed low-power application.

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