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Carry Select Adder with Multi- Threshold CMOS Logic

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Abstract: The focus of VLSI technology is to increase the speed by reducing the propagation delay from input to output. Carry propagation is also one of the reason for sequential generation of the sum for each bit after the arrival of the previous carry. But some of the adders like ripple carry adder which have less area, more delay and the carry select adder of less delay and more area the carry select adder circuitry is which has replaced many circuitry in different processing system to get faster application. There are two ripple carry adders in carry select logic adder to generate the sum for carry input equal to zero and carry input equal to one. Multiplexers are used to select the sum based on the previous carry being propagated to previous stages. In linear carry select adder, mismatch of speed between input and propagated signals creates delay problem which can be reduced by using the square root carry select adder. In square root carry select adder the ripple carry adder is divided into different block to the different bits to reduce the arrival time of previous carry bit. Ripple carry adder delay when large number of bits are considered for design. So replacing ripple carry adder for carry input equal to one with the binary to excess one converter, minimizes area and power but with slight increase in delay. D latch based square root ripple carry adder is used. To improve the performance of this system MTCMOS D latch is used.

Keywords: SQRT CSLA, BEC, MTCMOS D LATCH.

I. INTRODUCTION

Area and power plays a major role in the designing of integrated circuits because of increase in demand of portable system and rapid growth of power density in VLSI circuits. Addition usually influence the overall performance of the digital system and arithmetic operation. There are wide verities of adders such as half adders, full adders etc. Among them carry select adder is one of the fastest adder. It is used in multipliers, FIR filters, DSP processers etc. The area of carry select adder is more due to the repeated blocks of ripple carry adder for carry input equal to zero as well as carry input equal to one. Thus, the number of logic gates needed to implement this system is more. So, power consumption and delay will increase. Thus, we have to implement a carry select adder with efficient logic to reduce the area, power and delay of the system. Our objective is to study the performance of carry select adder with different logic, compare them and propose a suitable solution to reduce the power consumption, area and delay. Our goal is to design a carry select adder which satisfy these design constraints.

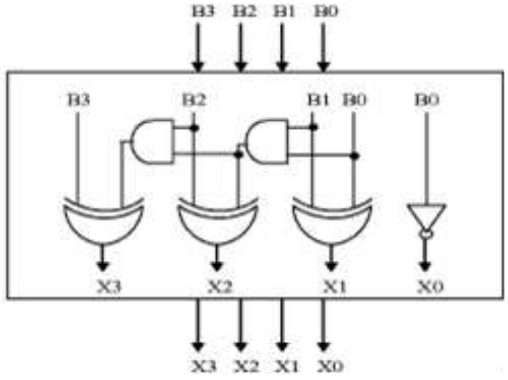
II. CARRY SELECT ADDER WITH BEC LOGIC

Binary to excess one converters is used to improve the speed of addition. Binary to excess one converter replaces the ripple carry adder for carry input equal to one in the regular square root carry select adder. The main advantage of BEC logic is that it reduces the number of logic gates than the full adder structure. Ripple carry adder will produce the sum and carry when carry input equal to zero and BEC will produce the sum and carry when carry input equal to one. Multiplexer will select the required output as per the previous. 16-bit Carry select adder with BEC logic

BEC Logic

B [3:0]	X [3:0]
0000	0001
0001	0010
-	-
-	-
1110	1111
1111	0000

Function table of 4 bit BEC



4-bit BEC Logic

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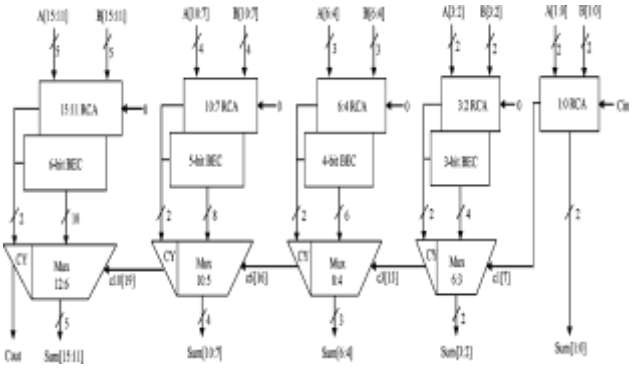
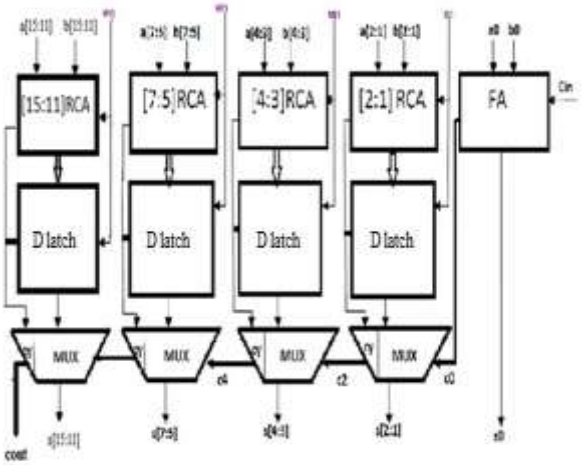


The basic of carry select adder is obtained by using the 4 bit BEC together with the multiplexer. One input of the multiplexer gets as its input (B3, B2, B1 and B0) and another input of the multiplexer is the BEC output. This produces the two possible partial results in parallel and the multiplexer is used to select either the BEC output or the direct inputs according to the control signal carry input. The Boolean expression of the 4 bit BEC is listed as (note the functional symbols ~ NOT, & AND, ^ XOR). [5]

X0 = ~B0
X1 = B0^B1
X2 = B2 ^ (B0&B1)
X3 = B3^ (B0&B1&B2)

III.CARRY SELECT ADDER WITH D LATCH

This method replaces the BEC circuit by D latch. Latches are used to store one bit binary information. The latch is one of the sequential circuits so their outputs depends on present and previous inputs. Latch is sensitive, when latch is enabled, the operation of latch changes according with the input signal of the latch. When enable equal to zero, the last state of the D input is trapped and held in latch and the output from the ripple carry adder is directly given as input to the multiplexer without any delay.



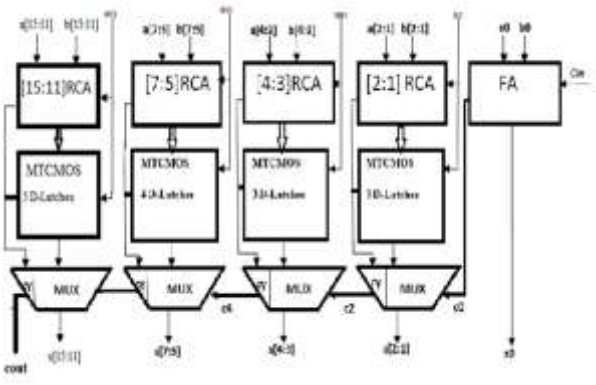
16-bit carry select adder with Dlatch

IV.PROPOSED WORK CARRY SELECT ADDER WITH MTCMOS D LATCH LOGIC

The performance of the D latch based square root carry select adder can be improved by using MTCMOS D latch logic. For implementing n bit adder require n bit MTCMOS D latch. In this only one ripple carry adder is used. It will add the input for carry input equal to zero and also for carry input equal to one. MTCMOS D latch will reduce the leakage power dissipation in the standby state by removing its supply voltage. Multi threshold CMOS logic provides low leakage and high performance by using high speed, low threshold voltage for logic cells and low leakage, high threshold voltage as sleep transistors. Sleep transistors disconnect logic cells from power supply or ground to reduce leakage in sleep mode. It can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each block to create a virtual ground and power supply.

In active mode the sleep transistor is on, so the circuit function as usual. In the standby mode, the transistor is turned off, which disconnects the gate from the ground. Additional power saving will be achieved if the width of the sleep transistor is smaller than the combined width of the transistors in the pull down network. Transistors with a low threshold voltage are used to implement the logic where as high threshold voltage devices are used as sleep transistors.

When enable equal to one the ripple carry adder will add the input for carry input equal to one and stores the result in MTCMOS D latch.. Multiplexer will select the output according to the carry output from the previous stage.



16-bit carry select adder with MTCMOS D latch

MTCMOS Logic

Multithreshold CMOS circuit technology are used for reducing the leakage currents in low voltage circuits in stand by mode with the use of two different threshold voltages in the circuit.Low threshold voltages are used to provide high switching speed and high threshold voltages are used to isolate the logic gates in stand by mode to prevent the leakage desssipation in the circuit. In active mode, high threshold voltage transistors are on so that the

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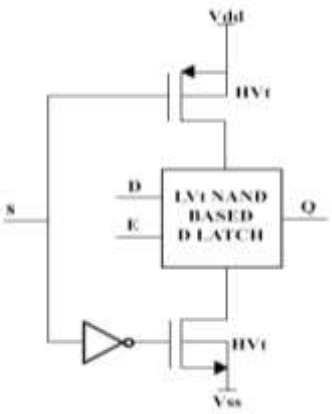
circuit with low threshold voltage operate in less switching power dessipation. When the circuit is in stand by mode, high threshold voltage transistors are turned off.

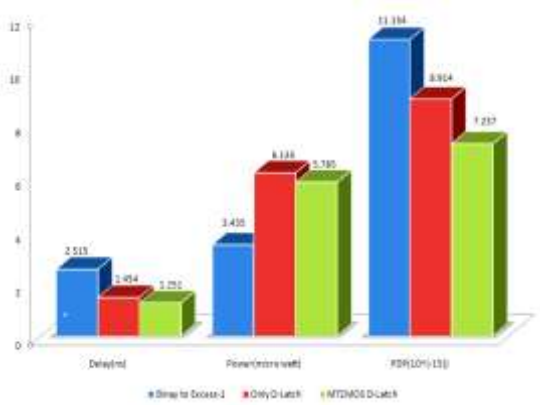


MTCMOS D latch

The enable line act as a control signal basing on which the output can be predicted. Using high threshold and low threshold voltage, MTCMOS based D Latch can be designed. When enable line is zero, output reflects same as input. Enable line one makes the output to be in the previous value. Sleep transistors when on, internal circuit is in direct contact with the power supplies ($V_{dd}$and V_{ss}) and for standby mode internal circuit get power from virtual power supplies.

V. RESULT AND DISCUSSION

In this proposed structure, the gate count is more when itCompared to the BEC based SQRT CSLA. This analysisshows that the proposed structure has although more power due to the increment in gate count but the delay is around half and hence the Power-Delay Product (PDP) is also reduced which is around 35.11% less as compared to previous architectures. When the area and power are not the constraints, this proposed structure is taken to be the efficient one for high speed data path design.



Comparative Analysis

VI.CONCLUSION

Adder has wide varieties of applications in microprocessors, digital signal processors etc. In this project, we proposed to develop a new low power carry select adder using multi threshold technology. Different types of carry select adder were studied and compared their performance. This comparison help us to choose the multi threshold CMOS technology. It will achieve our all goals such as reducing the area, delay and power with better performance.

In this we are concentrated on the reduction of area, power, and delay of the ordinary carry select adder. To remove this, we can use this MTCMOS technology to a great extent. We can use this technology to implement many more adders with same problem as that of carry select adder. And adder is an unavoidable Circuit in many devices, so that as the speed and performance of the adder increases the chances also increases. So, we can use this technology to implement more adders with low area, power and with high efficiency.

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BIOGRAPHIES

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