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Fault Coverage Analysis Of VLSI Circuits

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Abstract: Identifying the faults in the electronic circuits is a hard process. As the complexity of Very Large-Scale Integration (VLSI) is growing testing becomes complex and harder. A malfunctioning circuit is a result of design flaw, manufacturing defects or both. Testing is used as a measure to estimate the quality of design. Hence detecting a flaw more than one time has high degree of fault coverage. Earlier fault models are used to test the digital circuits at gate level or below that level. This project focus on creating a Register Transfer Level (RTL) modeling for the digital circuit and finding out the fault coverage of given test patterns. Fault models are taken based on the observed failures or by analyzing various types of faults. Fault coverage reflects the quality of test vectors with respect to the fault models. For a VLSI system consisting of different modules the overall coverage is a weighted sum of RTL module coverages[17]. Here a device under test is created and fault modelling and simulation is done to obtain the fault coverage. Device under test taken here is an adder circuit which is used to analyze the process, where single Stuck-at-faults are introduced arbitrarily and the test process is carried out using 3- bit sequence pattern. These patterns, which are generated randomly flow through the entire circuit, and compare it with the faults that are present in the components, either at the input or output. During the comparison if the component response and the pattern response are same, then it is considered as a fault free component. If the response differs, they are considered as fault and are recorded. In this manner many patterns detect the same faults or different faults. The fault coverage is then analyzed for the circuit from the simulated result[13]. This entire testing process is analyzed by using tools like MODELSIM & System Verilog. Analysis can be performed on other high-speed adder and multiplier circuits to get the fault coverage.

Keywords: VLSI, RTL (Register Transfer Level), DDS, Gates.

1.INTRODUCTION

All VLSI manufactured chips are tested for identifying defects.Stuck-at fault is widely accepted fault model .Identifying the faults in the electronic circuits is a hard process. Hence, detecting a flaw more than one time has high degree of fault coverage. An RTL fault simulator; which is the core of the methodology, is developed to support RTL testability analysis. It is able to generate quantitative RTL fault Coverage and provide information for test pattern improvement at the RTL level[15].RTL fault coverage and gate level fault coverage are quite similar to each other is.The RTL description is more readable and the gate level combinational circuits implemented by synthesis tools usually contain no redundancy.

Functional testing and structural testing are the two types of testing commonly used. Functional testing is the verification of the functional operation of the design and Structural testing is the actual verification for proper construction of each element in the circuit.[3]

1.1 Fault modeling

Fault modeling can be done in both logical operators and sequencial circuits. When RTL constructs contain logical operators, faults are injected on variables that constitute inputs of such operators. Hardware description languages support both types of sequential elements, latch as well as flip-flop. In both cases, RTL faults are placed on input ports of these components. The basic testing environment is shown in fig 1.1

1.2 Fault simulation

Fault simulation is mainly done to calculate the efficiency of test patterns to detect the faults. There are three types parallel fault simulation, its fault injection and treatment are carried out in parallel, deductive fault simulation, Deductive fault simulation circuit can be deduced the normal state of lead on each circuit can be measured fault,concurrent fault simulation, it is completing the true value in the simulation as well as complete fault simulation, critical path tracing method, the fault simulation is from primary output to primary input ,from the top in the end of the so called critical line tracking[4]

1.3Fault coverage, Testing and verification

Fault coverage is the ability to check how much percentage of fault can be detected during testing.there are different types of coverages ,code coverage,branch coverage ,statement coverage,fsm coverage ,functional coverage. code

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coverage is a measure used to describe the degree to which the source code of a program is executed when a particular test suite runs. Testing is a mechanism to assure quality of a product ,system ,or capability. Verification is the process for determining whether or not a product fulfills the requirement or specification[15]

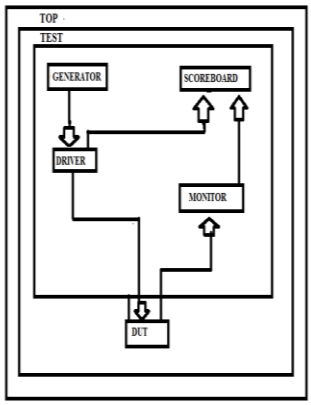

Fig1.1 Basic Testing Environment

2.DESIGN UNDER TEST

It is important to achieve very high fault coverage (in the 95-100% range) for given circuit with a minimum number of test patterns. The test generation cost depends on the complexity of the circuit. Methods of reducing the complexity of a circuit for testing purposes are referred to as design-for-testability techniques.the dut considered here is ripple carry adder,baugh wooley multiplier,finite state machine.[7]

2.1 Ripple carry adder

A ripple carry adder in fig 2.1 is a digital circuit that produces the arithmetic sum of two binary numbers. It. can be construct with full adders connected in cascaded with the carry output. from each full adder connected to the carry input of the next full adder in the chain .It needs a good circuit and a faulty circuit for testing.

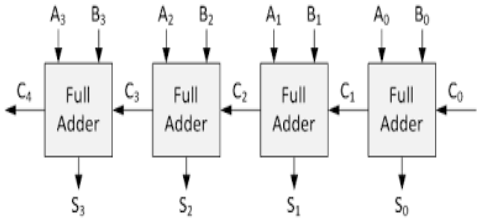

Fig 2.1 Ripple Carry Adder

2.2 Baugh Wooley Multiplier

Baugh wooley multiplier was developed to design direct multiplier for twos complement number .Its used for signed numbers multiplication.When multiplying twos complement number directly each of the partial product to be added is a signed number.

2.3 Finite State Machine

A finite-state machine (FSM) in fig 2.3 or finite-state automation, finite automaton, or simply a state machine, is a mathematical model of computation. It is an abstract machine that can be in exactly one of a finite number of states at any given time.

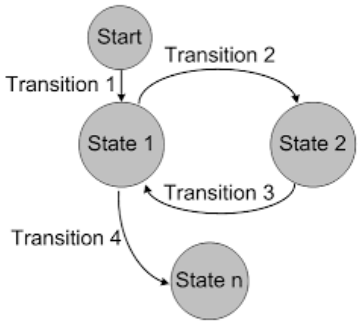

Fig 2.3 State Transition Diagram

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Moore and Mealy machines are both types of finite-state machines, they are equally expressive. a Moore machine is a finite-state machine whose output values are determined only by its current state. This is in contrast to a Mealy machine, whose output values are determined both by its current state and by the values of its inputs.here what I have choosen is the mealy machine. Pattern detector is considered as the mealy machine here. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected.the pattern 1101 has been detected through fsm .

2.4 DDS Verification

Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators mixers, modulators sound synthesizers and as part of a digital phase-locked loop. A DDS has many advantages over its analog counterpart, the Phase-Locked Loop (PLL), including much better frequency , improved phase noise, and precise control of the output phase across frequency switching transitions. Disadvantages include spurs due mainly to truncation effects in the NCO, crossing spurs resulting from high order (>1) Nyquist images, and a higher noise floor at large frequency offsets due mainly to the Digital-to-analog converter.

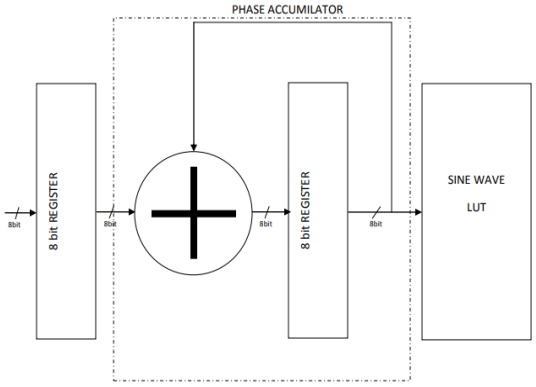

Fig 2.4 Block diagram representation of DDS

3 . EXPERIMENT RESULTS

```
inside DUT
 design is ok
                    1a=000 b=010 s=010 c=0
inside DUT
 design is ok
                    2a=111 b=010 s=001 c=1
inside DUT
 design is ok
                    3a=100 b=110 s=010 c=1
inside DUT
 design is ok
                    4a=011 b=101 s=000 c=1
inside DUT
 design is ok
                    5a=101 b=000 s=101 c=0
inside DUT
 design is ok
                    6a=000 b=111 s=111 c=0
inside DUT
 design is ok
                    7a=000 b=001 s=001 c=0
inside DUT
 design is ok
                    8a=110 b=101 s=011 c=1
inside DUT
 design is ok
                    9a=011 b=111 s=010 c=1
inside DUT
 design is ok
                   10a=100 b=001 s=101 c=0
```

Fig 3.1 Simulation result of Ripple carry adder

```
inside DUT
 design is ok
                    1a=000 b=010 s=010 c=0
inside DUT
 design is not ok
                    2a=111 b=010 s=111 c=0
inside DUT
 design is not ok
                    3a=100 b=110 s=110 c=0
inside DUT
 design is not ok
                    4a=011 b=101 s=111 c=0
inside DUT
 design is ok
                    5a=101 b=000 s=101 c=0
inside DUT
 design is ok
                    6a=000 b=111 s=111 c=0
inside DUT
 design is ok
                    7a=000 b=001 s=001 c=0
inside DUT
 design is not ok
                    8a=110 b=101 s=111 c=0
inside DUT
 design is not ok
                    9a=011 b=111 s=111 c=0
inside DUT
 design is ok
                   10a=100 b=001 s=101 c=0
```

Fig 3.2 Simulation result of Ripple carry adder

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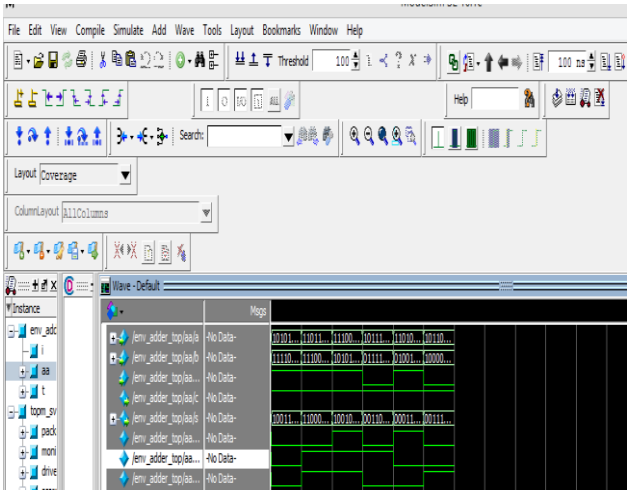

Fig 3.3 Waveform of Ripple Carry Adder

Coverage Summary by Structure:

Design Scope	Coverage (%)
env_adder_top	100.00%
i	100.00%
aa	100.00%
t	100.00%
top_sv_unit	47.56%
generator	62.50%
driver	100.00%
monitor	100.00%
scoreboard	42.59%
environment	100.00%

Coverage Summary by Type:

Weighted Average:				60.93%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	48	45	3	93.75%
Branch	4	2	2	50.00%
FEC Condition	2	0	2	0.00%
Toggle	40	40	0	100.00%

Fig 3.4 Fault coverage of Environment

Weighted Average:				100.00%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	3	3	0	100.00%
Toggle	20	20	0	100.00%

Fig 3.5 Fault coverage of Ripple Carry Adder

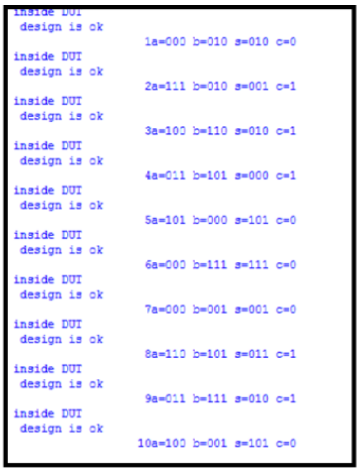

Fig 3.6 Simulation result of Baugh Wooley Multiplier

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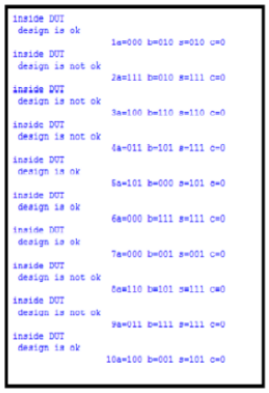

Fig 3.7 Simulation result of Baugh Wooley Multiplier

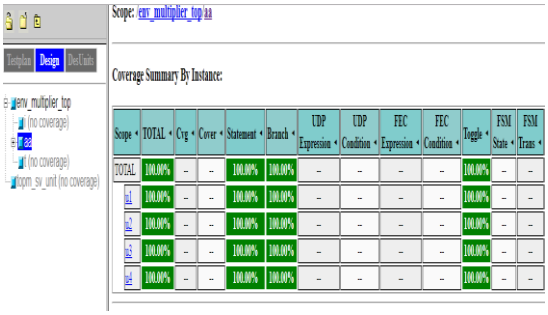

Fig 3.8 Fault coverage of Environment

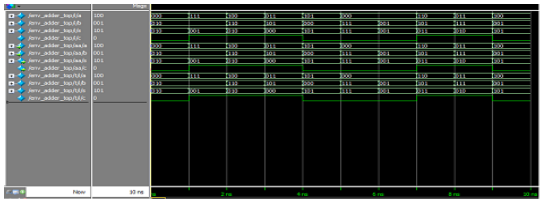

Fig 3.9 output waveform of baugh wooley multiplier

Weighted Average:				100.00%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	4	4	0	100.00%
Branch	24	24	0	100.00%
Toggle	152	152	0	100.00%

Fig 3.10 Fault coverage of Baugh Wooley Multiplier

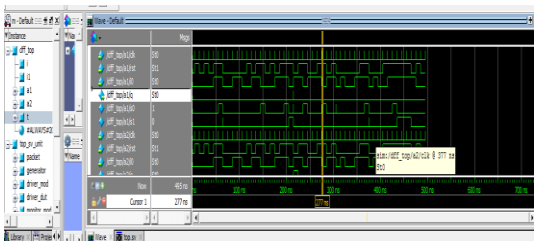

Fig 3.11 Simulation graph of Pattern Detector

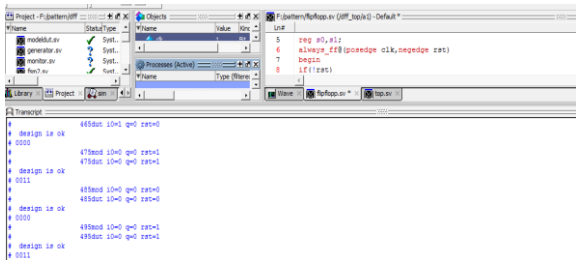

Fig 3.12 Simulation report of Pattern Detector

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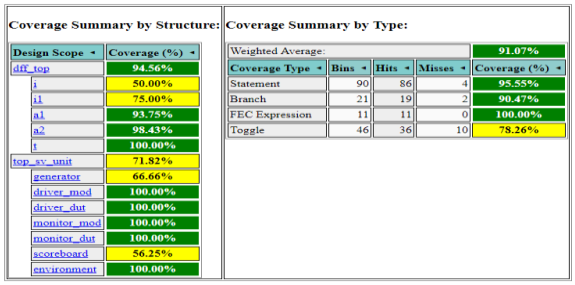

Coverage Summary by Structure:

Design Scope	Coverage (%)
dff_top	94.56%
i	50.00%
i1	75.00%
a1	93.75%
a2	98.43%
t	100.00%
top_sv_unit	71.82%
generator	66.66%
driver_mod	100.00%
driver_dut	100.00%
monitor_mod	100.00%
monitor_dut	100.00%
scoreboard	56.25%
environment	100.00%

Coverage Summary by Type:

Weighted Average:				91.07%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	90	86	4	95.55%
Branch	21	19	2	90.47%
FEC Expression	11	11	0	100.00%
Toggle	46	36	10	78.26%

Fig 3.13 Coverage of the Environment

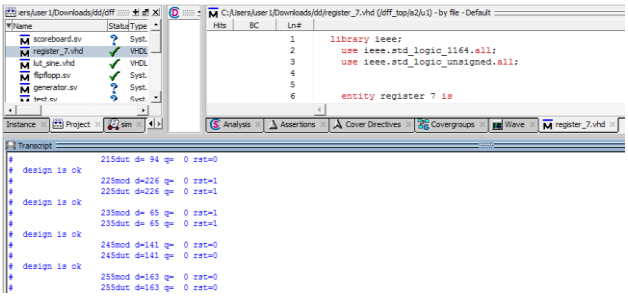

Fig 3.14 Simulation report of DDS

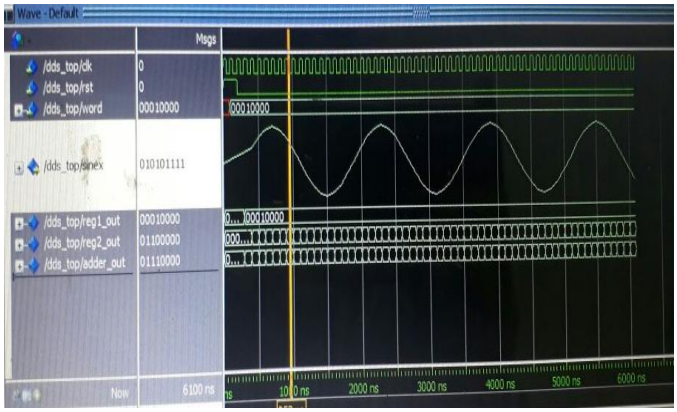

Fig 3.15 Output Waveform of DDS

Coverage Summary by Structure:

Design Scope	Coverage (%)
dff_top	99.61%
a1	99.61%
a2	99.61%

Coverage Summary by Type:

Weighted Average:				99.61%
Coverage Type	Bins	Hits	Misses	Coverage (%)
Statement	16	16	0	100.00%
Branch	12	12	0	100.00%
Toggle	172	170	2	98.83%

Fig 3.16 Coverage analysis of DDS

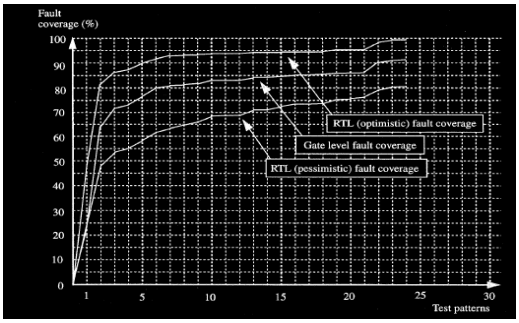

Fig 3.17 Parameter showing the variation of RTL and GATE level coverage

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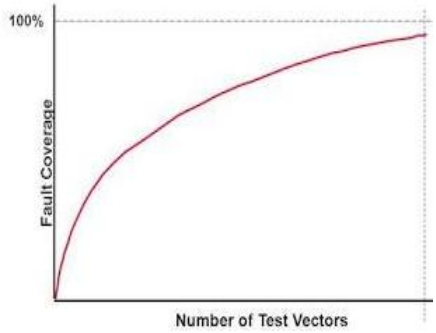

Fig 3.18 Graph showing the variation of coverage with test vectors.

Ripple Carry Adder	100%[RTL]
Baugh Wooley Multiplier	100%[RTL]
Pattern Detector	98%[GATE]
Direct Digital Synthesizer	99%[GATE]

Fig 3.19 Analysis table of Circuits

CONCLUSION

A behavioral and structural fault model for an adder circuit,multiplier circui ,finite state machine and an application circuit is designed in this project. The circuit is tested for different test patterns by introducing the concept of fault injection and fault simulation. Fault modeling can be performed on the circuit depending on the type of fault occurring at the input or output side. Simulation is performed using MODEL SIM and different types of coverage can be taken as seen in the output waveform. With this approach an RTL designer can have an estimation of the achieved fault coverage and also it is possible to locate faults at higher level of abstraction. This approach is applied to combinational and sequential circuits. A comparative analysis of fault coverage can be done for these circuits in future.

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