Solid State Transformer Interfaced Squirrel Cage Induction Generator Wind Turbine using Interleaved SEPIC Converter

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Abstract: In ac/dc Power Factor Correction (PFC) applications, wherever a good vary dc link voltage is needed, boost derived topologies are not any longer the foremost appropriate circuit topologies for universal grids. During this paper associate degree interleaved SEPIC device and SST capable of providing a good vary dc link voltage is investigated. The interleaved converter is able to process more power with reduced circuit ripples and harmonics distortion, and current stresses. Additionally, because the coupled inductors share a common magnetic core, the count of magnetic devices is kept the same as the single-phase topology. Moreover, using coupled inductors effectively solves the current sharing problems caused by the duty cycle mismatch. The SVM provides the phase of gate signals among different phases can be artificially shifted by a certain degree which would contribute to reduce the circuit harmonics as well as the current ripples. The output is optimized by BCO algorithm for better response from SST model.

Keywords: PFC (Power Factor Correction), SEPIC (Single-Ended Primary Inductor Converter), BCO (Bacterial Colony Optimization), SST (Solid state Transformer).
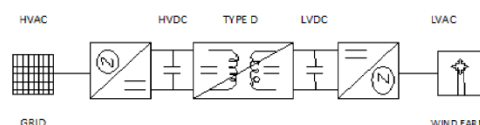
INTRODUCTION

Many of the industrial as well as residential applications require dc-dc converters and these converters should be capable of providing higher power density, high Conversion efficiency and low electromagnetic interference (EMI) and low noise level. In solar applications and wind turbines the generated voltage and current will exhibit a non-linear v-i characteristics and the maximum power point will vary with solar insolation in case of p-v cells and wind speed in case of wind turbines. So the intermediate DC-DC converter should be capable of adjusting the voltage and current levels and vary the load so as to extract maximum power from the load. Also many of the electrical equipment will require front end ac-dc converters which will consists of a diode bridge rectifier. This rectifier action will cause a non-linear current to be drawn from the ac line which causes wave form distortion, harmonic generation and related problems. So a dc-dc converter with power factor correction should be employed between the rectifier and reservoir capacitor. In this paper, an analysis of an interleaved sepic converter was carried out. An interleaved converter with two sepic converters connected in parallel was considered for this work. The performance of the conventional sepic and interleaved sepic were compared by means of simulation. Simulation of the system was carried out using MATLAB/Simulink.

EXISTING SYSTEM

SST MODELING AND CONTROL

Different topologies are of the SST are completed to reach the considered tasks and proposed applications. Four basic SST configurations are identified: A) A single-step with transformer isolation that provides an AC conversion, from a high range of voltage to a lower one. It has no DC link. B) A two-step conversion with isolated AC/DC and DC/ AC steps that provides the low voltage of both DC and AC, respectively. C) A two-step conversion with ACIDC and isolated DC/AC steps, with no DC link of low voltage. and D) A three-step conversion with DC/AC, DCIDC, and ACIDC steps that provides all kinds of high and low voltages of AC and DC.
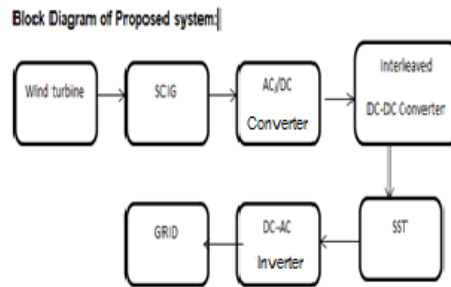

Type D Topology

A comparison of representative topologies for the implementation of SST is performed. Surely, the most suitable topology to support the required functionalities is Type D, i.e. three-stage conversion, which provides all the functionalities expected from a Solid State Transformer, it can be interfaced DC micro grids (PV, Fuel Cell, Batteries,

and etc.,) via its low voltage DC link. Beside the HVDC absorbs some part of ripple coming from AC sides so L VDC link will have smaller ripple. It provides reactive power compensation, voltage conversion, active power flow and voltage regulation that are investigated in the following. In order to perform SST for the suggested tasks, a variety of topologies can be adopted. In spite of different kinds of SST, the overall control objective intrinsic to its operation is the same, irrespective of their circuit topology. For the purpose of compensating/transferring reactive/active tens of power, AC and DC voltages are used, respectively.

PROPOSED WORKS

The SST used in this paper is a cascaded type three phases SST that its configuration and control are adopted. It consists of three stages:
1) A three-phase AC/DC rectifier
2) A DCIDC stage, which is named as the Dual Active
Bridge (DAB) and use a high-frequency transformer
3) A DC/AC Inverter

Block Diagram of Proposed system:

ADVANCING POWER RATING OF PFC CONVERTER
The power level of a power electronic converter is limited due to several factors. Increasing current increases stresses on switching devices, diode reverse recovery current and parasitic resonance currents become greater than the main switch can handle, and the size of the boost inductor should be increased to avoid saturation and overheating problems. The component stresses can be reduced by controlling the turn off rate of the boost diode current by implementing passive or active snubber circuits and the power level can be slightly advanced, but in order to advance the power level significantly the methods including device paralleling, module paralleling, power stage paralleling, and interleaving are widely utilized.

A. Interleaving
Interleaving of DC-DC converters is a well-established concept. It is widely used in power supplies and power factor correction circuits. In interleaved operation of dc converters also known as multiphase operation, several identical converters all switching at the same frequency are operated in parallel but with a uniform phase shift between them. This causes the ripple at the input and the output terminals of the converter to have a frequency that is a multiple of the switching frequency of each individual converter and the number of interleaving branches. Mathematically there is no limit for the number of interleaved power branches. But, in practice as the phase number increases, the system complexity increases and control and maintenance becomes difficult. The main advantage of interleaving is the reduction of input current and output voltage ripples with smaller magnetic material volume than other methods. The input EMI filter size and output capacitor size are reduced in proportion with the ripple reduction. The disadvantage of the interleaving method is increase in the gate driving logic complexity, but necessarily the size and cost of the gate drive. Logic signals to all the gates are equally phase shifted by the amount defined as

$$PS = k \frac{2\pi}{N}$$

N denotes the number of interleaved branches and k denotes the order of discrete interleaved branches (k = 1.2… N).According to the operating requirements, duty cycle of the converter should be varied. Therefore the degree of ripple cancellation is also varying parameter. The most optimum cancellation of ripple may be a perform of the duty cycle of the convertor and therefore the range of phases. A way of activity the variation of the ripple cancellation as duty cycle is varied is by exploitation the issue Fc. The factor Fc is a ratio of the ripple magnitude of the interleaved converter to the magnitude of the ripple in one individual phase or converter. From the fig.1 it can be seen that, maximum ripple cancellation is obtained for a duty ratio of 0.5 and the percentage of ripple content increases when duty ratio moves towards zero and one.
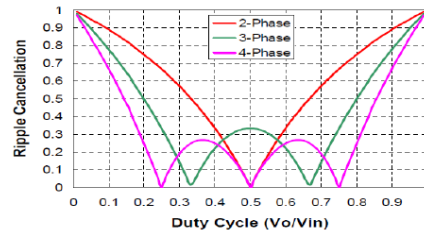
Fig.1. Ripple cancellation Factor Fc Vs duty cycle

Circuit Configuration and Operation Principle

Single-Ended Primary Inductor Converter (SEPIC) is a derived dc-dc converter whose output voltage can be more, less, or equal to the input voltage depending up on the duty ratio. That is the sepic can provide buck boost operation without polarity reversal. Interleaving technology has been employed in the planned SEPIC so as to any scale back the filter size, and gain higher potency. Within the interleaved configuration, we tend to parallel n SEPIC cells, and unnaturally shift the part of the gate signals by 2π/n, some ripple may be entirely off because of the phase shift and the RMS current of output capacitor is reduced. Therefore, the size of output capacitor and EMI filter can be greatly reduced.
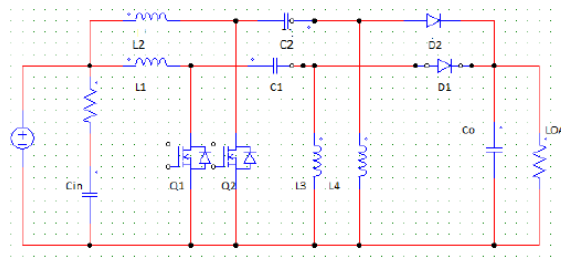
Fig.2. Interleaved SEPIC

The circuit components of converter cell 1 include L1, S1, C1, L2 and D1, and the circuit components of converter cell 2 consist of L3, S2, C2, L4 and D2. S1 and S2 are driven in the interleaved fashion (with 180 degree phase shift), and the inductor currents, IL1, IL2, IL3 and IL4, have to operate under Continuous Conduction Mode (CCM). When the converter works in boost type (duty ratio is greater than 0.5), and in DCM mode when duty ratio is less than 0.5.

A. Modes of Operation

The operation of interleaved sepic is similar to the conventional sepic. In boost mode of operation since duty ratio is greater than 0.5, firing pulses of both converter will overlap each other. So at-least one switch will be on for entire operating cycle. But in buck mode, there will be no overlapping between the firing pulses. So one switch will remain off during some time of the operating cycle. For the converter, the values of all capacitors are taken to be sufficiently large so that they will block the direct current. Hence the average value of current flowing through them is zero. The inductors L3 and L4 are only source of load current. So average current through these inductors will be same as load current.

A SEPIC is claimed to be in continuous-conduction mode if this through the inductance L1 and L2 ne'er go right down to zero. Throughout a SEPIC's steady-state operation, the typical voltage across capacitance C1 and C2 is adequate to the input voltage (V_{in}). As a result of capacitors C1, C2 blocks electrical energy, the typical current across its zero, creating inductance L1 and L2 the sole supply of load current. Thus the typical current through inductance L2 is that the same because the average load current and thus freelance of the input voltage. The operation of boost converter in boost mode is explained below.
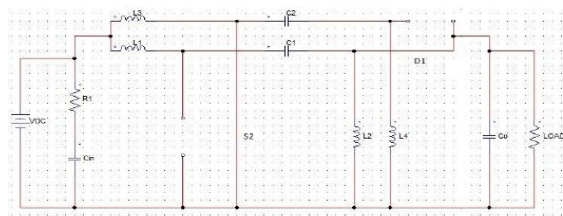
Mode 1

Fig. 3 Mode 1 operation

In mode 1, switch S1 is on and S2 is off. Capacitors C1 and C2 are charged to input voltage with left plate positive. Inductor L3 will be charging and capacitor C2 will be discharging through S2 and L4. This makes the diode D2 to be reverse biased. Since S1 is off, D1 will be forward biased and inductor L1 and L2 will be discharging through the load.
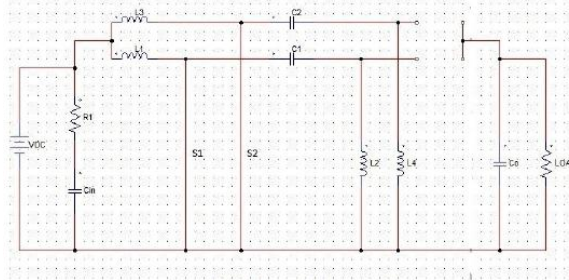
Mode 2

Fig. 4 Mode 2 operation

In this mode, both switches are turned on, hence all inductors will be charging.

Mode 3
S1 is turned on and S2 is turned off. So current in L1 and L2 will be increasing and that of L3 and L4 will be decreasing.
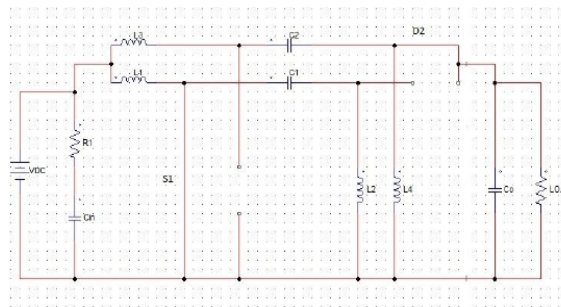

Fig. 5 Mode 3 operation

Mode 4
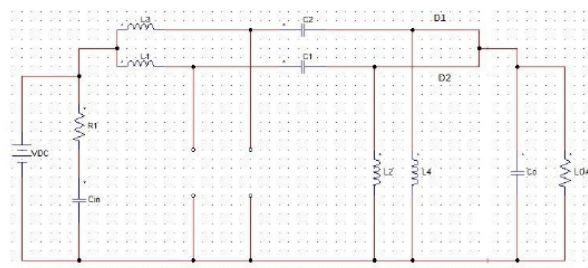Here both switches are turned off. Hence all inductors will be discharging.
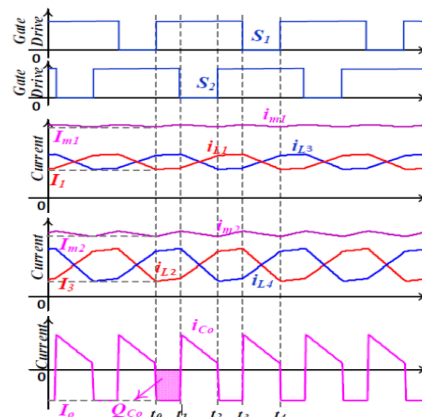

Fig. 6 Mode 4 operation

Fig. 7 Boost operation
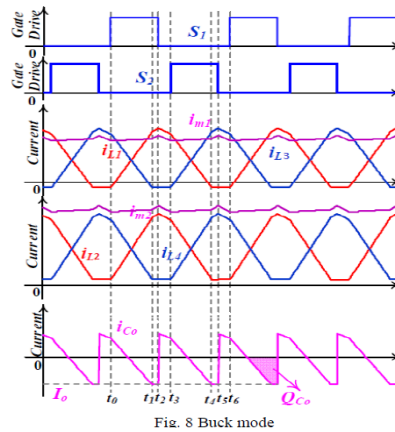
DOI 10.17148/IJARCCE.2018.7433

Fig. 8 Buck mode

Circuit wave form for boost operation is shown in figure. 7. For boost operation, inductor charging time will be greater than discharging time. Similarly, the wave form for buck operation is given in figure 8. For buck mode, inductor charging time will be less than discharging time.

Design Equation of PFC SEPIC Converter

The operation of the SEPIC depends upon the constant current in the intermediate ripple-filter inductor (L3 and L4).The selection of Boost inductor (L1 and L2) and capacitors C1, C2 and Co is based on allowable ripple current and voltage and is given by following equations.

Output voltage $VO = D\, Vin/(1-D)$
Boost inductor $L1, L2 = D\, Vin/[fs\, (\Delta ILi)]$
Intermediate capacitor $C1, C2 = DVdc/\, [(Rfs)\, (\Delta VCi)]$
Output filter inductor $L3, L4 = (1-D)Vdc/[fs(\Delta ILo)]$
Output filter capacitor $Co= Iav\, /(2\omega\Delta Vdc)$

The symbols used are fs for switching frequency; Vin for average input voltage of SEPIC converter; D for Duty cycle; ΔILi for Peak to peak ripple current ILi ; ΔILo for Peak to peak ripple current ILo; Lo and Li for filter inductor and Boost inductor respectively; Co and Ci for filter capacitor and Boost capacitor respectively; Iav for average DC output current.

Bacterial Colony Optimization Principle:

Lifecycle Model

The behavior of artificial bacterium during this paper includes 5 elements; however those behaviors area unit continuous, mingle, and amalgamate. Chemo taxis behavior is usually in the midst of communication on the entire lifecycle. Therefore, chemo taxis and communication area unit treated mutually model in microorganism COLONY Optimization (BCO). Bacterium have 2 chooses once long times of chemo taxis and communication. They may die for the lack of food, or they may reproduce if they are capable of searching for food. Within the complicated environment, some individuals may run into dangerous place (go out of boundary). Specific situations like this also worth special treatment in Lifecycle Model (LCM). Migration conducts as associate degree freelance model that involves energy depletion, cluster diversity, and chemo taxis potency.
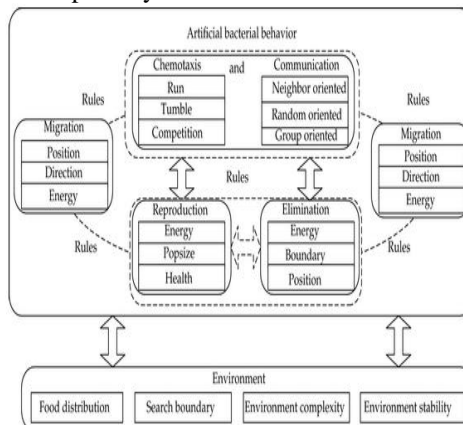

Figure 9: Lifecycle model.

The framework of this model relies on Associate in nursing Agent-Environment-Rule (AER) schema; that's, there are a unit 3 basic elements: agent, setting, and rule. The elaborate description is listed below: (i)A: artificial microorganism,(ii)E: artificial setting,(iii)R: the environment/organism interaction mechanisms. Lowest common multiple model is completely different from the first population-based model during which all the people share identical state properties. Lowest common multiple may be a philosophy that embraces the individuality of the people in an exceedingly system with multiple people that have its own set of state variables and parameters. Wanting in state area, the population is cherish clouds of people with similar behaviors, and alternative clouds, amounting to separate people. Basically, this permits for people to exist and phylogeny to occur and permits extinction. In general, the lifecycle model of artificial microorganism in BCO will be divided into four sub models: chemo taxis and communication model, copy model, elimination model, and migration model.

Bacterial Colony Optimization
Implementation of Chemo taxis and Communication

As illustrated above, bacteria chemo taxis all life time can be divided into two models: tumbling and swimming. In the process of tumbling, a stochastic direction participates into actually swimming process. Therefore, turbulent director and optimal searching director altogether influence the search orientation in tumbling, update the positions of each bacterium as ,whereas no turbulent director acceding in swimming process to affect the bacteria swimming toward optimal as formulated,

$$\text{Poistion}_i(T) = \text{Poistion}_i(T-1) + C(i)$$
$$* \left[f_i * (G_{\text{best}} - \text{Position}_i(T-1)) + (1-f_i) \right.$$
$$\left. *(P_{\text{best}_i} - \text{Position}_i(T-1)) + \text{turbulent}_i \right],$$

$$\text{Poistion}_i(T) = \text{Poistion}_i(T-1) + C(i)$$
$$* \left[f_i * (G_{\text{best}} - \text{Position}_i(T-1)) + (1-f_i) \right.$$
$$\left. *(P_{\text{best}_i} - \text{Position}_i(T-1)) \right],$$

Where $f_i \in \{0,1\}$ is the turbulent direction variance of the Th bacterium. And are the globe best or personal best position of the th bacterium. Is the chemotaxis step size. The BCO uses the adaptive chemotaxis step referred to Niu et al,

$$C(i) = C_{\text{min}} + \left(\frac{\text{iter}_{\text{max}} - \text{iter}_j}{\text{iter}_{\text{max}}} \right)^n (C_{\text{max}} - C_{\text{min}}),$$

Where iter_{max} the maximal number of iterations is, is the current number of iterations, and is the chemotaxis step of the th bacterium. With $C_{\text{max}} = C_{\text{min}}$, the system becomes a special case of fixed chemo taxis step length, as the original proposed BFO algorithm. If, it is the linearly decreasing strategy of chemo taxis step. And otherwise, chemo taxis size is changing with a nonlinear decreasing strategy. As it is proved by Niu et al. in their chemo taxis step mentioned papers, easy low-dimension issues favor to linear decreasing strategy of chemo taxis step, but, in high dimension multimodal complicated issues, nonlinear decreasing ways of chemo taxis step square measure additional common.

Implementation of Interactive Exchange

Interactive exchange in BCO may be divided into individual exchange and cluster exchange as represented on top of. Individual exchange can also specify dynamic neighbor familiarised and random familiarised cluster exchange suggests that cluster familiarised .But in every generation, each microorganism has only 1 kind of the exchange model to settle on. As interactive exchange might have an effect on the variety of microorganism cluster, every microorganism has only 1 probability to exchange in every generation. Pseudo code shows the method of interactive exchange.

Bacterial Behavior in Bacterial Colony Optimization

According to the comparative experiments, the proposed BCO algorithm shows the superior searching abilities in most cases. In this section, simulation studies will conduct in a vary environment with nutrient-noxious distribution. The nutrient distribution of environment at t =0 is set by the function, we are able to conclude that the new proposed optimization algorithm can find optimum at a high speed. When a relative optimum was found, the strategy was changed so that more time would be spent on local searching. After a long time of chemo taxis and communication, reproduction, and elimination process, the final fitness value of each bacteria has been showed in Figure 10. From Figure 10, we know that all of the bacteria have found the optimum at the end of 2000 runs.
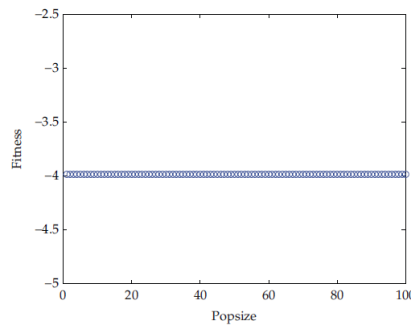
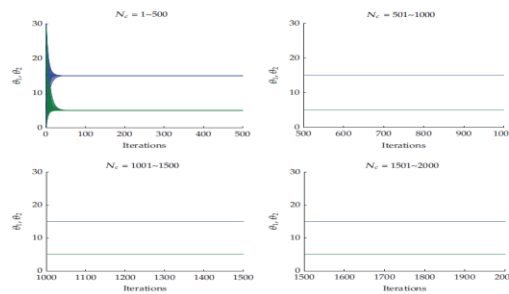Figure 10: The final optimal function values of each individual

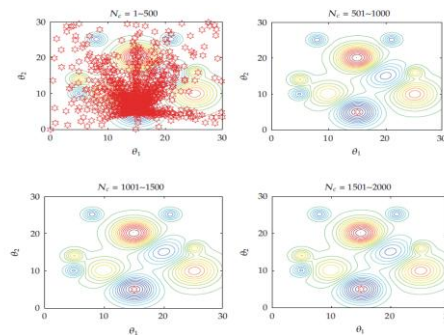Figure 11: 2-D Position with the iteration process

Figure 12: The process of finding the optimum

Figures 11 and 12 suggest that the position of the bacterial group changes with the chemotaxis process from two dimensions. In BCO, bacterial chemotaxis time equals to Running frequency. Chemotaxis goes along with entire optimization process. For example, if bacterial chemo taxis Nc _ 2000, then the whole run frequency Runs _ 2000. What the figures inform us is that bacteria can search for optimum quickly with the help of communication. Most individuals can even find the optimum in the first 500 runs. The above figures only point out the group search ability without answering how Micro communities can adapt their behavior to nutrients. The four bacteria optimization process. Those four bacteria are initialized from different positions, but after 100 runs, all of the four have found their optimum. The single bacterium chemotaxis process when chemotaxis ranges between 1 and 100. Optimum can be quickly achieved with our proposed method. In the first 25 steps, the bacterium had already entered into optimum region. Thereafter, it changes the strategy to local search, the whole optimum procedure, which reveals the fact that the bacterium has found the optimum after 100 runs.

BCO-optimized PI control design
In this part, bacterial foraging optimization technique is applied on the system in order to optimize the PI controller gains employed in a previous research study by maintaining the system in the upright position and to counteract the disturbances occurring in different motion scenarios.

Optimization algorithm objective functions and constraints
The most critical step in applying optimization techniques is to choose the objective functions that are used to evaluate fitness function. The objective functions can be created using performance indices functions to evaluate the errors of the controlled loops. These performance indices used to optimize the errors of the system are: mean of the squared error (MSE), Integral of Time multiplied by Absolute Error (ITAE), Integral of Absolute magnitude of the Error (IAE), Integral of the Squared Error (ISE), and time multiplied by the Squared Error (ITSE) to minimize the error signals and

compare them to find the most suitable one. The TWRM's bacterial foraging-optimized PI control scheme schematic description is demonstrated. The optimized PI controller is used to minimize the error signals by minimizing the value of the objective functions of performance indices defined as follows:

$$\mathbf{MSE} = \frac{1}{t} \int_0^{\tau} (e(t))^2 dt,$$

$$\mathbf{ITAE} = \int_0^{\tau} t\,|e(t)|\,dt,$$

$$\mathbf{IAE} = \int_0^{\tau} |e(t)|\,dt,$$
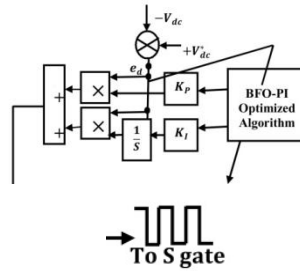
$$\mathbf{ISE} = \int_0^{\tau} e(t)^2 dt,$$

$$\mathbf{ITSE} = \int_0^{\tau} te(t)^2 dt,$$

Where $e(t)$ is the error signal in time domain.

Implementation of BCO-PI algorithm:
The behavior of the robotic machine was observed for the tilt angle of the entire vehicle, angular displacements of the two wheels, and linear displacements of the linear actuators using different motion scenarios.

Payload free motion ($h_1 = h_2 = 0$)
The system is considered to start initially at $\theta = -5°$ and neglecting the effect of both linear actuators, h_1 and h_2, by setting them to zero during the system stabilization. PI controller optimized by MSE gives a value of 46.6% of overshoot which is the biggest value for the overshoot, followed by 34.8% overshoot value for ITSE. The controller optimized by IAE gives the best value with minimum overshoot, 27.9%, where ISE and ITAE give good overshoot percentages for 33.8 and 29.3%, respectively. In summary, it is clear that BCO reduces the percent overshoot, especially if optimized by IAE criterion. As for settling time, it can be seen that the settling time values of BCO vary in the range of 0.78 s for IAE to 1.87 s for BCO optimized by MSE. The best method to optimize the settling time is by using the IAE, the best rise time is given by MSE (0.19 s) and the worst one is ITAE (0.248 s). All other BCO methods produce almost the same value. But because BCO results are not so different, it cannot be concluded that BCO can optimize the rise time. As in rise time values, the peak time values show almost the same values for all methods with small variation between them. All other BCO error methods produce peak time between 0.35 and 0.46 s. The best values are given by BCO optimized by MSE and ISE, 0.35 s. In short, the best optimized PI controller employed is the one optimized by IAE for the low percent overshoot and minimum settling time.

Payload vertical movement only
In addition, the system stability was examined for each BCO optimization criterion against the vertical linear motion of its center of mass. Considering the following initial conditions: $\theta = -5°$, $h_1 = 0.28$ m and neglecting the effect of the horizontal linear actuators h_2, Outputs and inputs simulation of the system in the case where the payload is kept fixed for a period of 12 s from the start of the simulation and then activated to move in a vertical direction along the IB for a distance of 10 cm before settling again at a height of around 38 cm from the chassis of the vehicle. It is clear, since no disturbance occurred in the stabilization condition of the IB,that the control scheme was robust and maintained the system's stability against the motion of h_1. Out of the five methods, the BCO optimized by IAE performed better than the other methods.

Payload horizontal movement only
For completing the picking/placing handling task, the TWRM is allowed to transfer the picked payload in a horizontal direction parallel to the chassis' axis, the output response of the system with moving the horizontal linear actuator only and its effects on the performance of the system stability. The carried load is kept stationary at a height of 28 cm. As for the horizontal actuator, it is permitted to orient horizontally for a distance of 7 cm before settling again at a fixed position. The model's initial conditions are set as follows: $\theta = 5°$, $h_1 = 0.28$ m, and $h_2 = 0$ m. As can be seen from this

scenario's simulation results, for the MSE and ITAE criterion, the system stability was affected by the activation of the horizontal actuator and the TWRM keeps moving instead of maintaining its position. On the other hand, the remaining methods produce better performance and good robust against the movement of the horizontal actuator.

Simultaneous vertical and horizontal motion (h_1 and $h_2 \neq 0$)
The system's output response with moving the two linear actuators simultaneously and their effects on the system's stability performance. The initial conditions are set to $\theta = -5°$, $h_1 = 0.28$ m, and $h_2 = 0$ m. The system, without any interruptions, remains stable during the operation of initiating the vertical linear actuator. However, once the horizontal actuator starts to extend its rod, for both MSE and ITAE criterions, the system stability was affected and the TWRM wheels keep maneuvering instead of preserving its position. This issue did not appear in the remaining methods' simulation results and produced good robust and better performance. Another phenomenon has been noticed, while the horizontal actuator activates. The IB tilts to the opposite direction of the horizontal actuator's extension with a steady inclination angle of around 7° for withstanding the change in the COM's position.

Trajectory of a 1-m straight-line motion
The system stability was examined during moving the TWRM in a straight line for 1 m after balancing the robot in the upside position, the control scheme, including the five tested criterions, was capable to counter the occurred disturbances caused by the wheels' motors' activation at the beginning (8 s) and the end (18 s) of the straight-line motion, the maximum control effort spent for maneuvering the system in a 1-m straight-line trajectory, compared to the other criterions, was noted for the ITSE method, around 1.8 N.

Control system robustness
Moreover, the system stability was examined against the effect of disturbance forces. As it is shown that disturbance force affects the system, but the controller reacts against this force to stabilize the system. However, the controller resulted from MSE shows that the displacement of the system is effected with slight change, while the other optimized controllers show better performance.

Space Vector Modulation:
The desired three phase voltages at the output of the inverter could be represented by an equivalent vector V rotating in the counter clock wise direction. The magnitude of this vector is said to the magnitude of the output voltage and also the time this vector takes to finish one revolution is that the same because the elementary fundamental quantity of the output voltage.
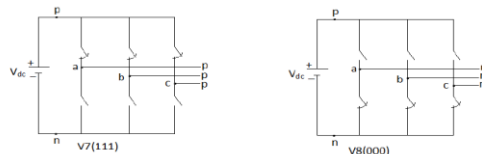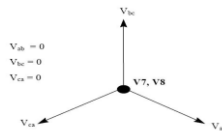
Figure13. Zero Output Voltage Topologies

Figure14. Representation of the zero voltage vectors in the α, β plane

When the desired line-to-line output voltage vector V is in sector 1 ,vector V could be synthesized by the pulse-width modulation (PWM) of the two adjacent switching state vectors V1 (pnn) and V2 (ppn), the duty cycle of each being d1 and d2, respectively, and the zero vector (V7 (nnn) / V8 (ppp)) of duty cycle d0:
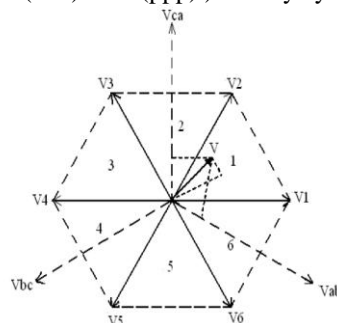
Figure 15 Output voltage vector in the α, β, plane

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$$d_1 \vec{V}_1 + d_2 \vec{V}_2 = \vec{V} = mV_g e^{j e}$$

$$d_1 + d_2 + d_0 = 1$$

Where, $0 \leq m \leq 0.850$ is the modulation index. This would correspond to a maximum line-to-line voltage of 1.0Vg, which is 15% more than conventional sinusoidal PWM is presented.

All SVPWM schemes and most of the other PWM algorithms, use the Equations 4.3 and 4.4 for the output voltage synthesis. The modulation algorithms that use non-adjacent switch state vectors are shown to supply higher doctorate and/or switch losses. however a number of them, for e.g. physical phenomenon modulation, will be terribly easy to implement and may offer quicker transient response The duty cycles 1 2 d d, and d0 , are uniquely determined from Figure 4.7, and the equations of 4.3 and 4.4, the only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle.
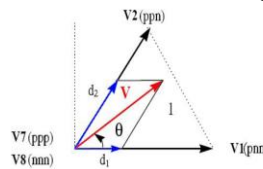

Figure16. Synthesis of the Required Output Voltage Vector in Sector 1

Space vector modulation algorithms:
Two-Dimensional Space Vector:

For any balanced three-phase variable $V_a + V_b + V_c$, where $\vec{V}$ be the voltage vector, there is a relationship.

$$V_a + V_b + V_c = 0$$

The above equation suggests that the three variables could be mapped into a vector V on the orthogonal plane, where $\alpha - \beta$

$$\vec{V} = \vec{V}_\alpha + j\vec{V}_\beta$$

The transformation for this orthogonal co-ordinate mapping, someday referred to as 3/2 transformation, is expressed as

$$\left[V_\alpha, V_\beta \right]^T = T_2 \left[V_a \quad V_b \quad V_c \right]^T$$

Where T is the transformation matrix and is expressed as

$$T = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}$$

Three-Dimensional Space Vector

For any balanced three-phase inverter, an assumption is always made that $V_a + V_b + V_c = 0$,

Where $\vec{V}$ be the voltage vector. The three variables in *a-b-c* coordinate *Vabc* can be mapped into a vector V on the orthogonal $\alpha - \beta$ plane. Since every variable maintains the equal section distinction for every section, zero–sequence current is mechanically invalid because the reference vectors are on a plane. once the system becomes unbalanced, there's no zero–sequence part or triple harmonics as a result of the reference vectors square measure on a plane So the three-dimensional space vector representation and mapping will be similar to that of 2-D one.

Two-Dimensional SVPWM for Calculating Switching Angles

A two-dimensional scheme for an *n*-level $n \geq 3$ cascaded multilevel inverter is proposed. In the proposed method, a simple algorithm of forming switching sequence is applied that leads to minimum change in voltage. An efficient hybrid construction electrical converter should make sure that the overall Harmonic Distortion (THD) within the voltage output wave shape is little enough. Associate in nursing formula is projected for the cascaded construction electrical converter with equal voltage steps below the area vector modulation. The formula leads to the tokenism ThD

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of output voltage of the cascaded construction electrical converter with equal voltage steps. A new expression of ThD is given to change the derivation. The output voltage of the hybrid construction electrical converter is 2S one with the SVPWM modulation $E_{p1}, E_{P2}, E_{p3}...E_{pn}$ indicates the voltage steps in positive side and $E_{n1}, E_{n2}, E_{n3}...E_{nm}$ indicates the voltage steps in negative steps. $\theta_1, \theta_2, \theta_3..\theta_n$ are the switch angles that indicates the on and off instance of switches within the electrical converter ar bestowed in Liang and Nwankpa (1999), Sirisukprasert et al (2002) and dynasty and Wang (2002).

Mathematical formulation

The formula are often expressed from the premise wave form by applying Fourier series analysis, the amplitude of any

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{n} \left[E_k \cos\left(n\theta_k\right) \right]$$

odd ordinal harmonic are often expressed as,

Where n is an odd harmonic and θ_k is the *kth* switching angle. The amplitude of all even harmonics is zero. The modulation index m is defined as,

$$m = \frac{\pi}{4} \frac{V_1}{\sum_{i=1}^{n} E_i}$$

Vn is the total harmonic component and *V1* is the fundamental harmonic component. The voltage THD is defined as

$$THD = \sum_{n=3,5,7,...}^{\infty} \sqrt{\frac{V_n^2}{V_1^2}}$$

Now, to search out the matter associate degreed to implement a rule for the subsequent variable inputs of the electrical converter $V_1, V_2, V_3...V_n$ Modulation index term m. Output of the algorithm $\theta_1, \theta_2, \theta_3...\theta_n$ such that THD is minimum. The input voltages $V_1, V_2, V_3...V_n$ are from dc sources. The input m is determined by a controller in multilevel inverter. The pulse angles $\theta_1, \theta_2, \theta_3...\theta_n$ are employed by the electrical converter to regulate the switches. It's vital to notice that minimizing voltage doctor's degree is fascinating in some applications. In some high power applications one needs to limit every order harmonic to sure most allowed values. For the 3 part system, the triple order harmonic may be off while not facilitate of modulation techniques, nevertheless it's desired to attenuate doctor's degree for sure applications is given in Beig et al (2004), Naik and Udaya (2005) and Khajehoddin et al (2007). From modulation index m, verify the worth of by evaluating

$$m = \sum_{k=1}^{n} e_k \sqrt{1-(\mu_k \rho)^2}$$

where,

$$e_k = \frac{E_k}{\sum_{i=1}^{n} E_i}$$

$$\mu_k = \frac{\sum_{i=1}^{nk} E_i - E_k/2}{\sum_{i=1}^{n} E_i - E_n/2}$$

The switching angles are determined by,

$$\theta_k = \sin\left(\mu_k \rho\right)$$

The output voltages of the inverter is,

$$V = \sum_{k=1}^{\infty} E_k \left(V_{\theta k} - V_{\pi-\theta k} + V_{\pi+\theta k} + V_{2\pi+\theta k}\right)$$

where V is unit function. By Fourier series expansion,

$$V = \sum_{n=1,3,5,...} V_n \sin\left(n\theta\right)$$

$$V_n = \frac{4}{n\pi} \sum_{n=1,3,5...}^{\infty} E_1 \cos\left(n\theta_1\right)$$

Modulation index m for the basic output voltage

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$$m = \frac{\pi}{4}V_1 = \frac{\pi}{4}\sum_{n=1}^{\infty} E_1 \cos\left(n\theta_1\right)$$

The THD is expressed as

$$\text{THD} = \sum_{n=3,5,7,\dots}^{\infty} \sqrt{\frac{V_n^2}{V_1^2}}$$

General structure of the algorithm

The control processing unit calculates the basic parameters to apply a switching state. The input data to the control processing unit is the reference space vector. During various iterations, the unit determines the sector number, triangle number of the subhexagon. The sector number and triangle number identify the correct switching sequence. The flowchart is given for an n-level inverter and can be used for any n-levels without change. The input supply is the amplitude of the voltage steps and modulation index m, the initial value of o . The flow diagram of the proposed algorithm to find minimum THD is shown. The modulation index mc is calculated for various iterations. The difference between two modulation index terms is calculated.
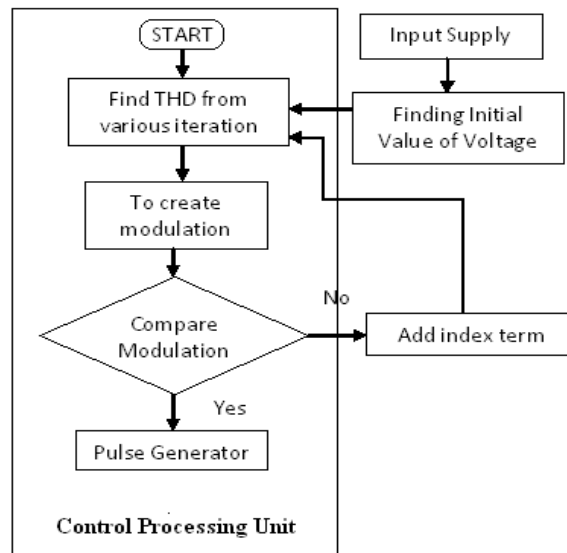

Figure17. Flowchart of the Algorithm

Where,

$$|m - m_c| < \delta$$

δ – Reference value increases (or) decreases the pulse generation in the pulse generator.

If the distinction between the 2 modulation index terms is a smaller amount than reference price, the planned formula outputs the best change angles. The iteration technique is employed to resolve and realize minimization of the voltage THD
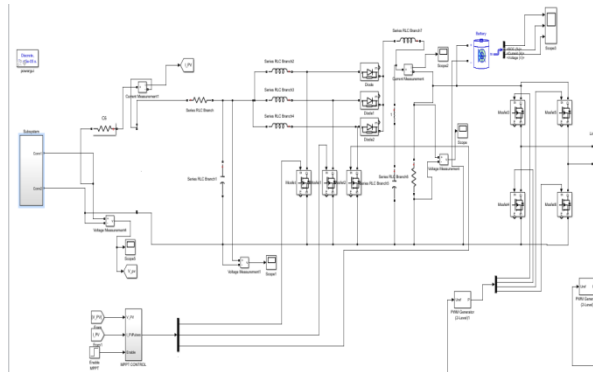
MATLAB Simulink
Introduction to MATLAB
MATLAB could be a software package for computation in engineering, science, and applied math.
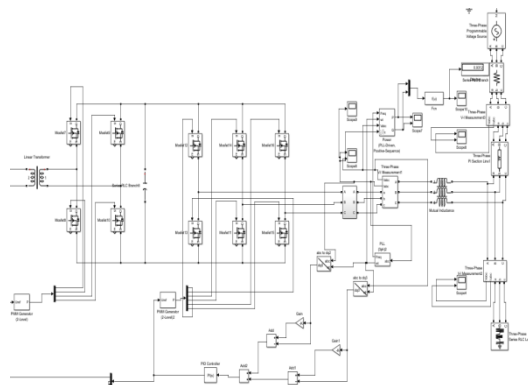

It offers a strong artificial language, glorious graphics, and a large vary of knowledgeable information. MATLAB is revealed by and a trademark of The Math Works, Inc. The focus in MATLAB is on computation, not mathematics: Symbolic expressions and manipulations aren't doable (except through the nonobligatory Symbolic tool cabinet, an imaginative interface to maple). All results aren't solely numerical however inexact, because of the misestimating errors inherent in pc arithmetic. The limitation to numerical computation will be seen as a disadvantage, however it's a supply of strength too: MATLAB is far most well-liked to Maple, Mathematical, and also the like once it involves numeric.
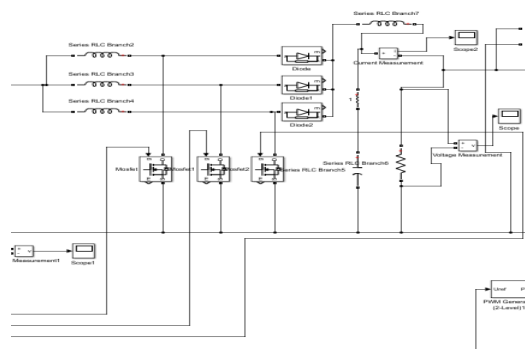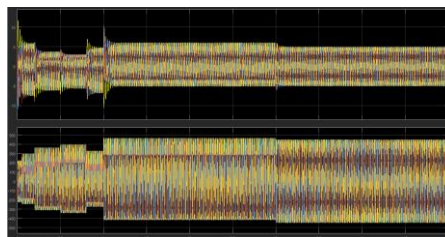
Simulation results:

The above figure shows the Simulink model (front end) of the Existing system.

The above figure shows the Simulink model (back end) of the Existing system.
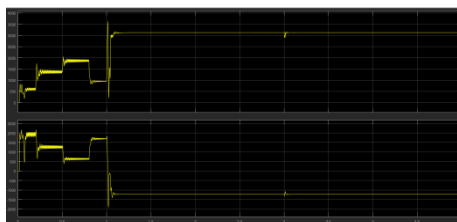

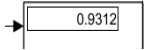The above figure shows the Simulink model of the interleaved converter in the Existing system.

The above figure shows the Simulation result of Three phase voltage (Vabc) & current(Iabc) in the Existing system.
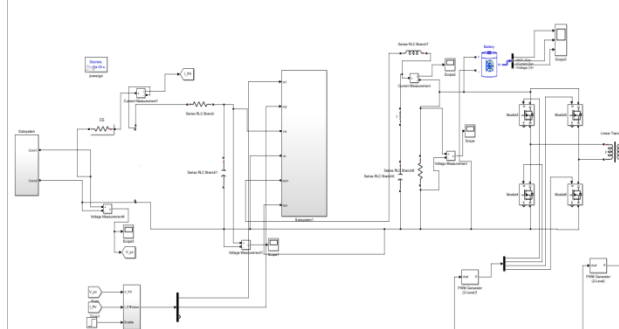
Their time response is T ≥1sec.

The above figure shows the Simulation result of Real power (W) and Reactive power (var) in the Existing system.

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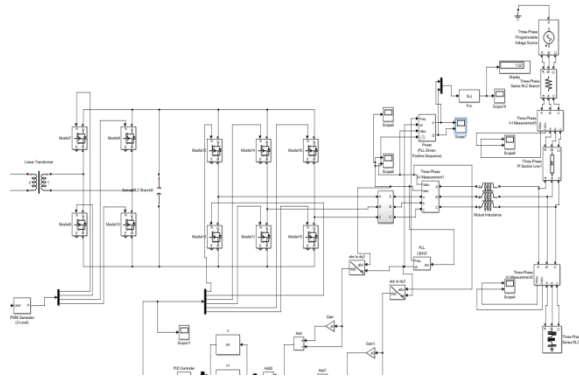ISO 3297:2007 Certified
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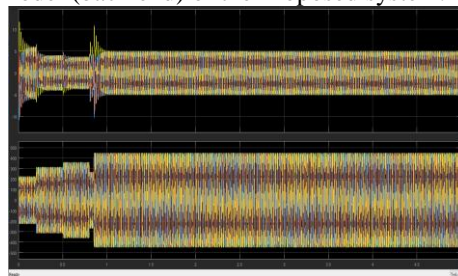
Their time response is T ≥1sec.

The above figure shows the numerical value of power factor in the existing system.
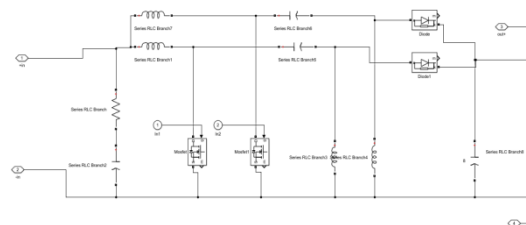

The above figure shows the Simulink model (Front end) of the Proposed system.
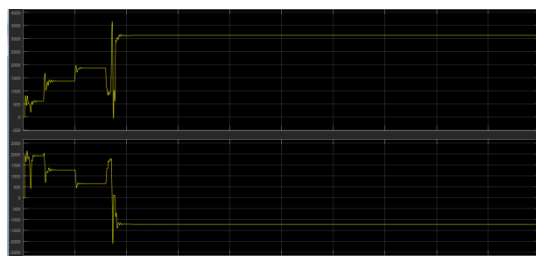

The above figure shows the Simulink model (back end) of the Proposed system.

The above figure shows the Simulation result of Three phase voltage (Vabc) & current (Iabc) in the Proposed **system.**

The above figure shows the Simulink model of the SEPIC converter in the proposed system.

Their time response is T< 1secThe above figure shows the Simulation result of Real Power (W) and Reactive power (var) in the Proposed system.
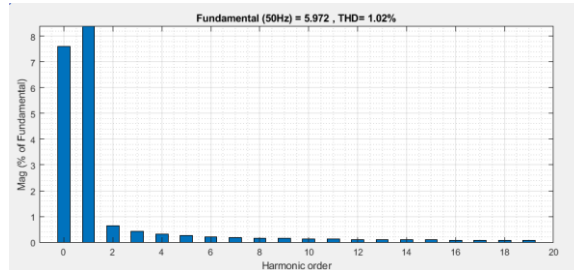
Their time response is T < 1sec.

Display

The above figure shows the numerical value of power factor in the proposed system.
Note: Thus, this proposed simulation result shows the quick time response when compared to the Existing system, and the power factor of the proposed system also attains Unity

The Result

Comparision Table

SNo.	Parameters	Proposed
1.	PCC Voltage	430 V
2.	Active power	180.53KW
3.	Reactive power	23.98KVAR
4.	Switching frequency	20Khz
5.	Output Voltage	430 V
6.	Voltage Ripple	0.1V
7.	Current Ripple	0.5A
8.	Efficiency	91%
9.	Power Factor	1
10.	Total Harmonics Distortion (THD)	1.021

CONCLUSION

In this paper, an interleaved and coupled SEPIC converter with 5kw SST is proposed for front end power factor correction. To evaluate some of the benefits of interleaving a 120W two phase interleaved SEPIC was simulated in MATLAB. This style might simply be upgraded to higher power by the right choice of power parts. Also, since the choice of output voltage and input voltage square measure at the designer's discretion, the fundamental style may well be tailored to several powered applications. Interleaving per fluorocarbon pre-regulators has several advantages. It will cut back EMI and boost inductance magnetic volume. The number of reduction varies and depends on the look necessities and style tradeoffs. The designer could prefer to cut back either the boost inductance magnetic volume or decrease the shift frequency to scale back the dimensions of the EMI filter. In some cases simply adding an extra part can cut back the dimensions of the EMI filter. Interleaving conjointly reduces the RMS current within the boost electrical condenser greatly reducing electrical over stress on the electrical condenser. However, the quality and value of the look can increase with every extra part.

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