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Designing and Optimizations Of Low Power Multiplexer Using CMOS Device Modeling

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Abstract: In today's world power consumption is become major power concern in VLSI designing. Portable devices like laptops, cell phones, and computers require a circuitry that consumes less power. Also large power dissipation is directly associated with cost and complexity of the devices. High speed multiplier plays a dominant role in designing of digital circuits. The low power CMOS devices can be used in real time image, speech processing and 3D computers graphics application, mainly the fields where high speed is required.

Keywords: MUX, MTCMOS, CMOS, Low Power VLSI, Leakage current.

I INTRODUCTION

With rapid development of portable digital applications, the demand for increasing speed, compact implementation and low power dissipation triggers numerous research efforts. The idea to enhance the performance of logic circuits results in the development of many logic design techniques during the last two decades. Multiplexer abbreviated as MUX can be analogue circuits using MOSFETs and transistors or they can be of digital type circuits made from logic gates.

II MULTIPLEXER

A Multiplexer can be analogue or digital in nature by either using transistors or logic gates. Multiplexer (MUX) is fundamentally used as a switch in arithmetic circuits. ALU is the dominant hardware element widely from handhelds to big computing devices. A digital equipment as a big unit has its market which depends on power back-up. When the size influences, it causes the power to proportionally vary.

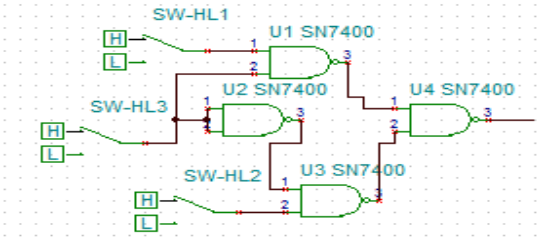

Fig 1 Multiplexer

III Static dissipation

Leakage power, also called static power dissipation, leakage power is actually consumed when the device is in its inactive state as all the power consumed in this state is considered "wasted" power. Different causes for the leakage power are CMOS leakage currents.

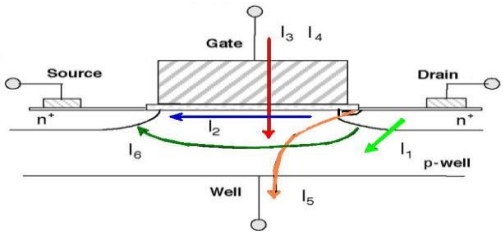

Fig 2 Leakage current mechanism in CMOS

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In current CMOS technologies, the sub threshold leakage current, I_{SUB}, is much larger than the other leakage current components. This is mainly because of the relatively low V_T in modern CMOS devices. I_{SUB} is calculated by using the following formula:

$$I_{SUB} = \frac{W}{L}\mu V_{th}^2 C_{sth}\, e^{\frac{Vgs - Vt + \eta Vds}{n\, Vth}} (1 - e^{\frac{-Vds}{Vth}})$$

where *W* and *L* denote the transistor width and length, μ denotes the carrier mobility, $V_{th} = \frac{kt}{q}$ is the thermal voltage at temperature T, $C_{Sth} = C_{dep} +$ Citdenotes the summation of the depletion region capacitance and the interface trap capacitance both per unit area of the MOS gate

In FN tunneling, electrons tunnel into the conduction band of the oxide layerequation show the FN tunneling of electrons from the inverted surface to the gate. Ignoring the effect of finite temperature and image-force-induced barrier lowering, the current density in the FN tunneling is given by.

$$J_{FN} = \frac{q^3 E_{OX}^2}{16\pi^2 h \emptyset_{OX}} \exp(-\frac{4\sqrt{2M * \emptyset^{3/2}}}{3hQE_{OX}})$$

Where E_{ox} is the field across the oxide; $Ø_{ox}$ is the barrier height for electrons in the conduction band; and m^* is the effective mass of an electron in the conduction band of silicon.

IV DYNAMIC DISSIPATION

In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance (CL) to ground during discharge. Therefore, in one complete charge/discharge cycle, a total of Q=CLVDD is thus transferred from V_{DD} to ground. For a small instant of time both PMOS and NMOS will be "on" simultaneously. The duration depends on the input and output transition (rise and fall times). So a direct path exists between VDD and GND (short circuit). The dynamic power consumption is given by

$$P_{DYN} = \frac{1}{2} C_L V_{DD^2} f_c$$

Since most gates do not operate/switch at every clock cycle, they are often accompanied by a factor'α', called the activity factor.

V MTCMOS TECHNOLOGY

The Multi-Threshold CMOS (MTCMOS) technology provides a solution to the high performance and low power design requirements of modern designs. While the low Vth transistors are used to implement the desired function, the high Vth transistors are used to cut off the leakage current. Multi-Threshold CMOS (MTCMOS) is an important enabling technology that provides high performance and low power operations by utilizing both high and low threshold voltage (Vth) transistors. By using low Vth transistors in the signal path, the supply voltage (VDD) can be lowered to reduce switching power dissipation while still maintaining the performance. Although the switching power can be reduced quadratic according to the VDD reduction, the Vth that has been decreased for the performance compensation incurs an exponential increase in the sub-threshold leakage current.

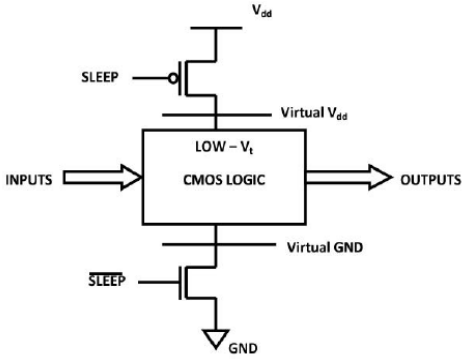

Fig3 MTCMOS General Structure

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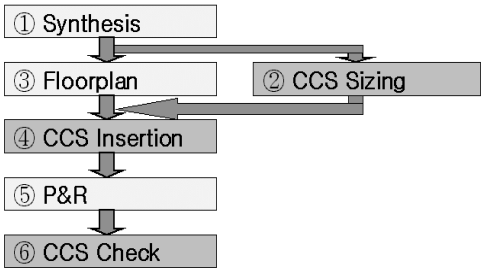

Fig 4 MTCMOS design flow

VI SIMULATION AND RESULT

For analysis purpose 2*1 multiplexer using CMOS and other model of 2*1 mux, simulate on cadence software and plot various graphs or power and currents comparator were also implemented using GDI and CMOS design techniques.

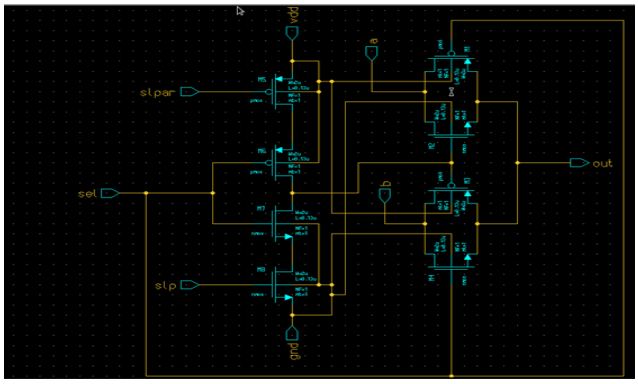

Fig 5 Schematic of MTCMOS 2:1 MUX Cell

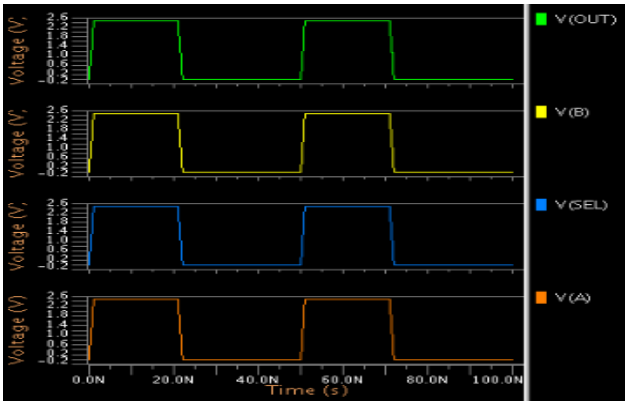

Fig 6 Out Wave form of voltage 2*1 Mux

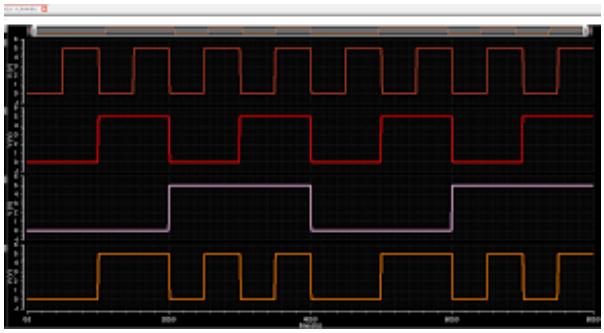

Fig 7 Output of MUX variable input

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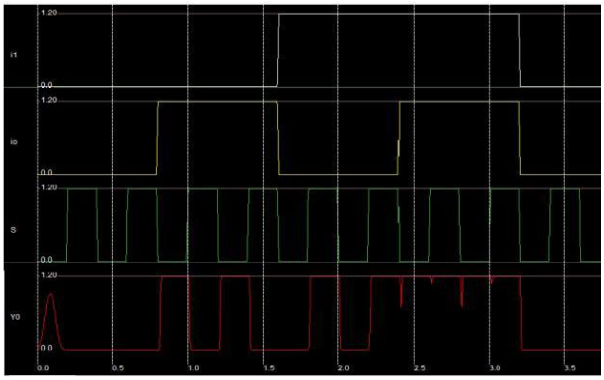

Fig 8 Output graph for leakage power

VII CONCLUSION

In the MTCMOS technique it consumes least amount of power as compare to the other techniques. The power consumption is decreases then the power dissipation will also decreases. The CMOS technique has high delay as compare to the other techniques. But the transmission gate technique has low delay and in MTCMOS technique it has delay but it is least as compare to the CMOS techniques.

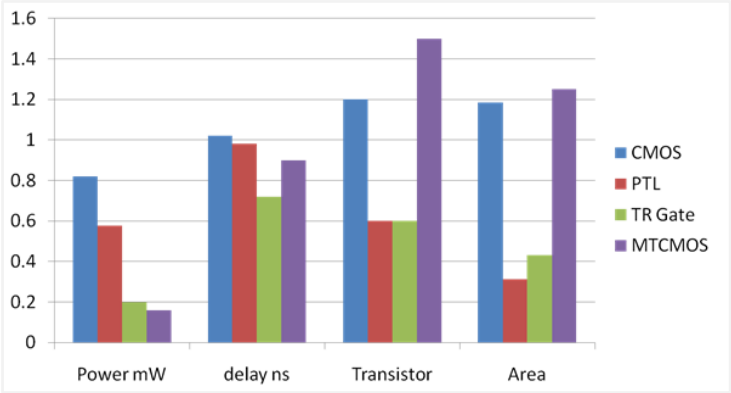

Fig 9 Comparisons of CMOS with other technique

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