ZIGZAG KEEPER: A NEW APPROACH FOR LOW POWER CMOS CIRCUIT

Kaushal Kumar Nigam[1], Ashok Tiwari[2]

Department of Electronics Sciences, University of Delhi, New Delhi – 110005, India[1]

Department of Electronic & Communication, MANIT, Bhopal – 462051, India[2]

ABSTRACT: In CMOS circuits, the reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence, static power dissipation. For the most recent CMOS feature sizes (e.g., 45nm and 65nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. ITRS reports that leakage power dissipation may come to dominate total power consumption [1]. In the nanometer technology regime, power dissipation and process parameter variations have emerged as major design considerations. These problems continue to grow with leakage power becoming a dominant form of power consumption. Leakage power dissipation is projected to grow exponentially in the next decade according to the International Technology Roadmap for Semiconductors (ITRS).This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques at circuit level and process level are used to efficiently minimize leakage current which lead to minimize the power loss and prolong the battery life in idle mode. A novel approach, named "Zigzag keeper," was proposed at circuit level for the reduction of power dissipation. Zigzag keeper incorporate the traditional zigzag approach with keeper which use the sleep transistor plus two additional transistors driven by already calculated output which retain the state of the circuit during the sleep mode while maintaining the state or state retention.

Keywords: Low Power, Sub-threshold Leakage, Gate oxide Tunneling.

I. INTRODUCTION

Power consumption is one of the top issues of VLSIcircuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobileera, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay and area and thus, designersare required to choose appropriate techniques that satisfyapplication and product needs. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage havebeen scaling down for decades. Because of this

technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-thresholdleakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduceleakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques

are summarized and compared with our new approach presented in this paper.

This paper is organized as follows: Section I gives the introduction of different approaches to minimize the power loss.Section II explains the proposed new approach.in section III Simulation and experimental result. We conclude in section IV followed by references.

II. PREVIOUS WORK

This Section reviews the previously proposed approach. In order to compare with the zigzag with keeper approach, this section explains several previous leakage reduction approaches: sleep, stack, zigzag and sleep keeper.

A.Base Approach

It is a traditional approach.Base approach is generally indicates conventional CMOS transistor. In the base approach pull-up network and pull-down network are used using few transistors. The pull-up network is called a P-MOS transistor and pull-down network is called as N-MOS transistor.
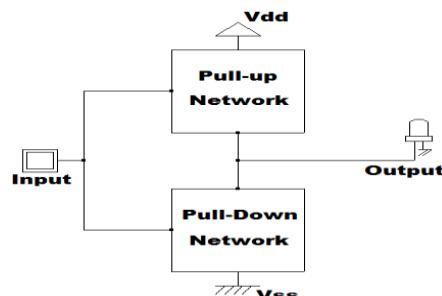

Fig.1: Base Approach

B.Sleep Approach

The most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between Vdd and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and Gnd.
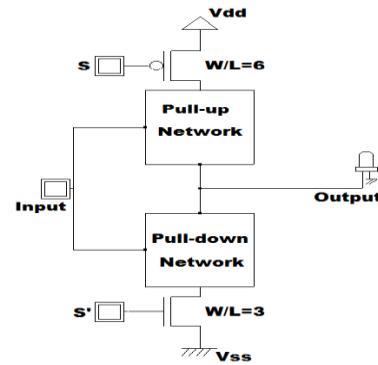

Fig.2: Sleep Approach

C. Zigzag Approach

The zigzag technique in Figure 3 uses one sleep transistor in each logic stage either in the pull-up or pull-down network according a particular input pattern [4]. Input vector that can achieve the lowest possible leakage power consumption. Then, we either assign a sleep transistor to the pull-down network if the output is '1' or else assign a sleep transistor to the pull-up network if the output is '0.' For Figure 3, we assume that the output of the first stage is '1' and the output of the second stage is '0' when minimum leakage inputs are asserted. Therefore, we apply a pull-down sleep transistor for the first stage and a pull-up sleep transistor for the second stage. To reduce the wake-up cost of the sleep transistor technique, the zigzag technique is introduced.
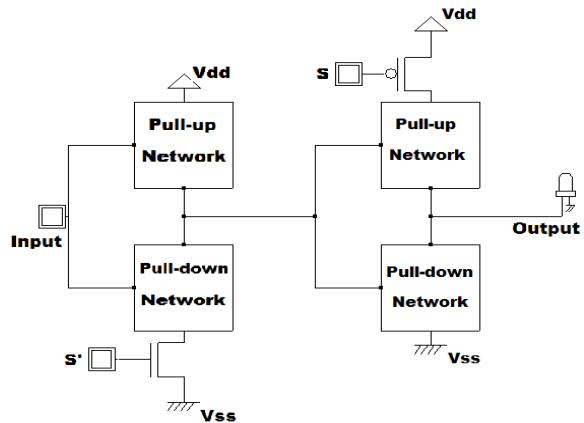

Fig.3: Zigzag Approach

The zigzag technique reduces the wake-up overhead by choosing a particular circuit state (e.g., corresponding to a "reset") and then, for the exact circuit state chosen, turning off the pull-down

network for each gate whose output is high while conversely turning off the pull-up network for each gate whose output is low. By applying, prior to going to sleep, the particular input pattern chosen prior to chip fabrication, the zigzag technique can prevent floating.

D. Stack Approach

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Fig 4 shows its structure. When the two transistors are turned off together, induced reverse bias between the twotransistors results in sub threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches.
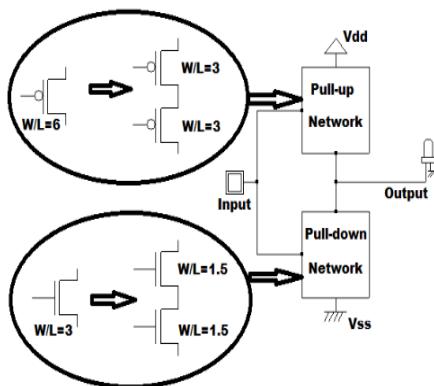

Fig.4: Stack Approach

E. Sleepy Keeper Approach

The basic problem with traditional CMOS is that the transistors are used only in their most efficient, and naturally inverting, way: namely, PMOS transistors connect to V_{dd} and NMOS transistors connect to G_{nd}. It is well known that PMOS transistors are not efficient at passing G_{nd}; similarly, it is well known that NMOS transistors are not efficient at passing V_{dd}. However, to maintain a value of '1' in sleep mode, given that the '1' value has already been calculated, the sleepy keeper
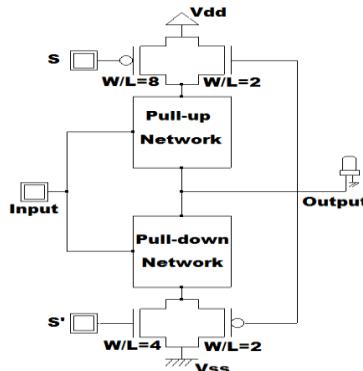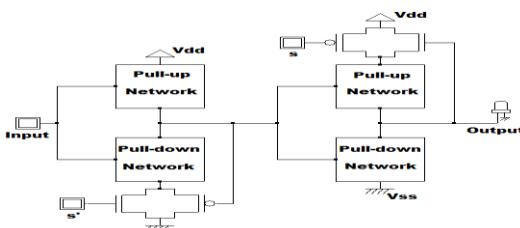

Fig.5: Sleepy Keeper Approach

approach uses this output value of '1' and an NMOS transistor connected to V_{dd} to maintain output value equal to '1' when in sleep mode. As shown in Figure 5.

An additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects V_{dd} to the pull-up network. When in sleep mode, this NMOS transistor is the only source of V_{dd} to the pull-up network since the sleep transistor is off. Similarly, to maintain a value of '0' in sleep mode, given that the '0' value has already been calculated, the sleepy keeper approach uses this output value of '0' and a PMOS transistor connected to G_{nd} to maintain output value equal to '0' when in sleep mode.

III. PROPOSED APPROACH

A. Zigzag Keeper Structure

In this chapter, introducing new leakage power reduction technique named as "zigzag with keeper". Zigzag keeper incorporates the traditional zigzag approach and sleep keeper approach which use the sleep transistor plus two additional transistors

driven by already calculated output –which retain the state of the circuit during the sleep mode while maintaining the state or state retention. Therefore, far better than any prior approach known; the zigzag with keeper technique can achieve ultra-low leakage power consumption while saving state.

Fig.6: Zigzag Keeper Approach

B. Zigzag Keeper Operation

In case of base approach no direct path occur from power rail to ground because it is a inversely behave such as V_{dd} is connected to PMOS transistor and NMOS transistor is connected to ground and if the input = '0' then output ='1' means PMOS transistor is turned on and NMOS transistor is turned off similarly if the input ='1' then output = '0' means PMOS transistor is turned off and NMOS transistor is turned on. However, it has to maintain a value '1' in sleep mode. A variation of the sleep approach, the zigzag approach reduces wake up caused by sleep transistor. Sleep transistor is added in base approach according to given logic value. It may be logic '0' or '1' value at the input of base approach. If the input ='0' then output ='1'. In this case PMOS transistor (pull-up) is turned on and NMOS transistor (pull down) is turned off, so the sleep(S') NMOS transistor always add in turnoff side means connect between pull-down network and ground of the first chain inverter but maintaining a value '1' in sleep mode, additional PMOS transistor is added to parallel with sleep (S') NMOS transistor. For the second chain inverter if the input = '1' then output = '0'. In this case PMOS transistor (pull-up) is turned off and NMOS transistor (pull down) is turned on so the sleep(S) PMOS transistor always added in turn off side means connect between power rail and pull-up network but maintaining a value '0' in sleep mode, additional NMOS transistor is added to parallel with sleep(S)PMOS transistor. During the active mode (s=0 and s'=1), the sleep transistors are turned on so it is reducing delay and during the sleep mode (s=1 and s'=0), the sleep transistor are turned off so it is saved state. MICROWIND software is used for this approach to analysis of power dissipation at different technologies such as 45nm, 65nm, 90nm, and 120nm at a given power supply according to technologies.
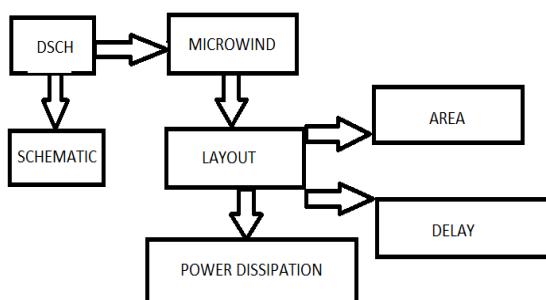

Fig.7: Experimental Methodology

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SCHEMATIC, LAYOUT USING A MICROWIND TOOL

We used MICROWIND software tool to estimate the power dissipation, propagation delay and Area. The supply voltages used by the technologies are tabulated in table:

Table1:The supply voltages used at different technologies

Technology	45nm	65nm	90nm	120nm
V_{dd}	0 .40v	0.70v	1.20v	1.20v

B. SIMULATION RESULTS

We haveestimated only the powerdissipation for eight design approaches i.e. the base case, sleep, zigzag, stack, and sleepy keeper approaches with newly proposed approaches named "Zigzag keeper". The simulations table for Power Dissipation is shown below

Table 2: Propagation Delay, Power consumption, Area

Techniques	Propagation Delay(ps)	Power Dissipation (µw)	Area (µm2)
Base	1.56	0.086	76.46
Sleep	2.42	0.040	107.12
Zigzag	1.35	0.038	99.32
Stack	0.39	0.098	106.01
Sleepy keeper	1.98	0.085	149.59
Zigzag keeper	1.22	0.011	172.62

The simulation result shows zigzag keeper approach is having the least power dissipation as compared to all the discussed approach. The power Dissipation is decreasing as the process technology scaled down. The result can be better explained in the form of graphs given below.
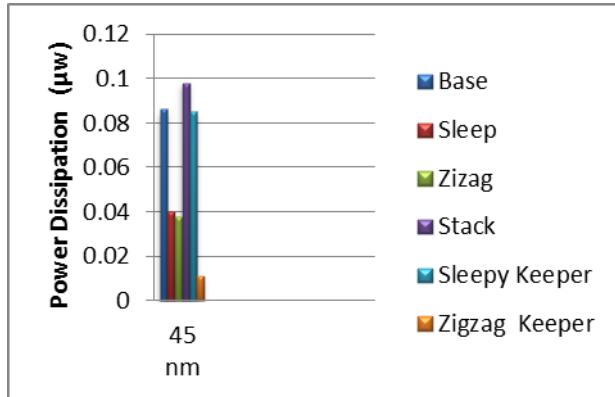
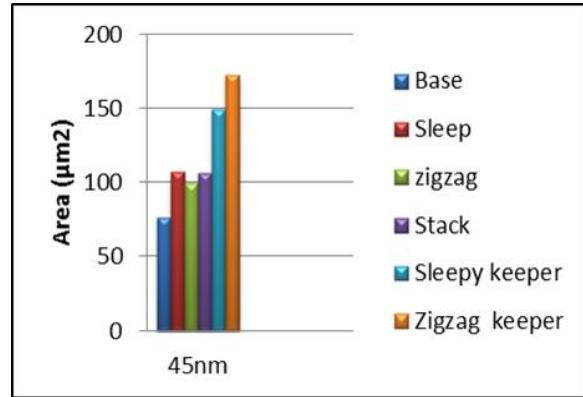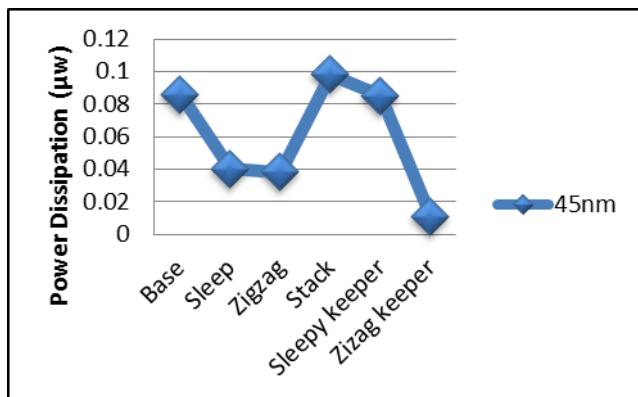Fig.8: Power Dissipation Chart for different
approach with 45nm

Fig.9: Power Dissipation Chart for different
technology with 45nm

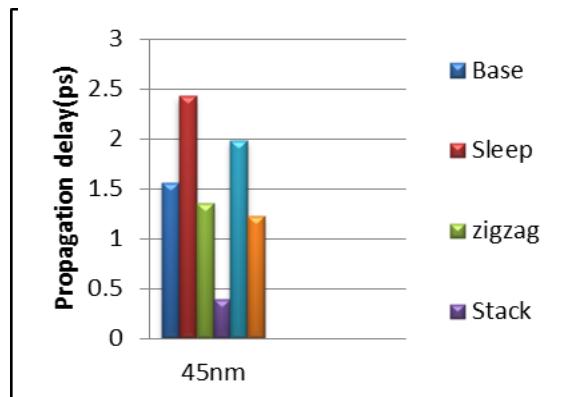Fig.10: Propagation delay Chart for different
approach with 45nm

Fig.11: Area chart for different approach with
45nm

V. CONCLUSION

In nanometre scale CMOS technology, sub-threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing power consumption is yet known. Therefore, designers choose techniques base upon technology and design criteria. Scaling down of device dimensions, supply voltage and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. We have presented an efficient design methodology for reducing the power dissipation in VLSI design.

The proposed technique in the thesis is "ZIGZAG KEEPER "and comparing the power consumption with other existing techniques. The proposed technique is more effective in reducing power consumption. The result is simulated with MICROWIND software.

VI. FUTURE PROSPECT

The advent of a mobile computing era has become a major motivation for low power design because the operation time of a mobile device is heavily restricted by its battery life. The growing complexity of mobile devices, such as a cell phone with a digital camera or a personal digital assistant (PDA) with global positioning system (GPS), makes the power problem more challenging.

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 1, Issue 9, November 2012

The proposed technique can be implemented in low power VLSI circuit and save the power consumption of the chip which leads to increase battery life.

REFERENCES

[1]International Technology Roadmap for Semiconductors, SemiconductorIndustryAssociation, 2002.

[2] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal ofSolis-State Circuits, Vol. 30, No. 8, pp. 847-854, 1995.

[3]M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijay Kumar, "Gated-   Vdd: A Circuit Technique to Reduce Leakage in Deep submicron Cache   Memories," International Symposium on LowPower Electronics and Design, pp. 90-95, 2000.

[4] K.-S. Min, H. Kawaguchi and T. Sakurai, "Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-gating Scheme in Leakage Dominant Era," IEEE International Solid-State Circuits Conference, pp. 400-401, 2003.

[5]Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, 1998.

[6]J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization andSimulation, pp. 148-158, 2004.

[7] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D. Dissertation, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2005.

[8]Kahng, S. Muddu, P. Sharma, "Defocus-aware leakage estimationand control**,"** International Symposium on Low Power Electronicsand Design, pp. 263-268, 2005.

[9] Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur,C.Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-kdielectrics reliability issues**,"** IEEE Transactions on Device and materials Reliability, Vol. 5, Issue 1, pp. 5-19, 2005.

[10]S. Kim and V. Mooney, "The Sleepy Keeper Approach: Methodolgy,

Layout and Power Results for a 4bit Adder," Technical Report GITCERCS- 06-03, Georgia Institute of Technology, 2006

[11] K. Flautner, N. S. Kim, S. Martin, D. Blaauw, and T. Mudge, "Drowsy Caches: Simple Techniques for Reducing Leakage Power," Proceedings of the International Symposium on ComputerArchitecture, pp. 148-157, 2002.

[12] H. Hanson, et al. Static energy reduction techniques for microprocessor caches. Proc.Of the Int. Conf. Computer Design, 2001.

[13] J. Kao and A. Chandrakasan, "MTCMOS sequential circuits,"Proceedings of European Solid-State Circuits Conference,pp 332- 335, 2001.

[14] Se Hum Kim and Vincent J. Mooney III, "sleepy Keeper: a New approach to low leakage power VLSI Design" very large integration,2006 IFIP International conference.