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# Analytical Study of Capacitance Extraction of MOSFET

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**Abstract**: Gate capacitance in PMOS is a key parameter for process development, material selection, and device modelling. This paper proposes and develops a extraction technique to overcome these shortcomings. Ids–Vgs and Ccx–Vgs are simultaneously measured so that the effect of $V_d$ on mobility is inherently taken into account, and the measured mobility becomes Vds independent. This allows the measurement time reducing to the order of microseconds and, in turn, minimizing the effect of charge trapping. Unlike the standard high-frequency $C_{ox}$–$V_{gs}$, Cox is independent of gate leakage. This advantages, together with its easy implementation, should make this technique a simple tools for process development, material selection, and device modelling in future generations of CMOS technology.

**Keywords**: Mobility, MOSFET, split C–V technique

## I. INTRODUCTION

The gate capacitance and channel mobility (µ ) is an important parameter for complementary metal oxide semiconductor (CMOS) technologies. Although saturation velocity is used for short-channel devices under high drain bias [1], effective mobility is widely used for benchmarking different devices in technology development and material selection [2], [3]. In addition, capacitances and mobility is a key parameters for device modelling [4]. The reduction in operation bias and doping can also lead to lower field for future CMOS technologies. As a result, accurate extraction of capacitance and mobility is essential. Conventionally, effective mobility is extracted by measuring the inversion charge per unit area [5]–[7]. The drain side from the Ids–$V_{gs}$ measurement [8], [9], and a nonzero bias must be applied to the drain, typically in the range of 25–100 mV [7]–[13]. This $V_{ds}$ reduces the voltage difference between the gate and the channel when moving toward the drain, leading to a non uniform charge distribution. When $Q_i$ is determined from the split C–V technique, however, both the source and the drain are grounded, and the channel is uniform. As a result, the Qi measured by the conventional C–V is higher than the inversion charges for Ich, leading to an underestimation of mobility [14]–[18]. Since capacitance mobility is an important parameter for technology development and circuit simulation, impact from $V_{ds}$ must be corrected. Efforts have been made to take into account $V_{ds}$ impact on mobility evaluation [14]–[19]. Huang et al. [14] measured the gate-to-source capacitance values separate biasing the source and the substrate to achieve the same conditions as those for measuring Ich. [15] averaged two Cox measured with and without substrate bias. Liu et al. [19] suggested to correct mobility either by mathematical extrapolation based on a nonzero drain bias condition or by averaging Ich measured under two $V_{ds}$ with opposite polarities. Thomas et al. [16] performed a linear regression to obtain the limiting value of $dI_d/dV_g$ at $V_d$ =0 V. Corrections have been also made through analysis and modelling [17], [18].

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## II. STRUCTURE

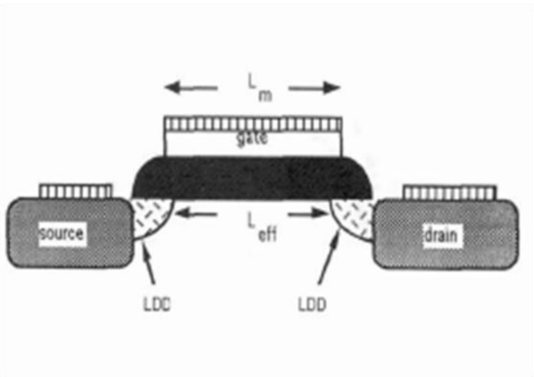

FIGURE-1: STUCTURE OF MOSFET

Figure-1 is the structure of the P-type MOSFET transistor which has oxide thickness ($t_{ox}$) 30nm, intrinsic concentration (Ni)$1.4*10^{10}cm^{-3}$, Impurity atoms (Na)$2*10^{15}$,width of the channel (W) 3µm, channel length(L)1µm,and the threshold voltage ($V_t$) is the 0.75v.

### III. ANALYTICAL ANALYSIS

The analysis of P-type MOSFET in different ways have done and many articles published such as [17], [19]. The extraction technique of capacitance method is slightly more complicated than the conventional approach, it gives very accurate $Q_i$ at different $V_{DS}$, which cannot be easily achieved using the conventional approach. Based on this technique, the capacitance Cox is obtained by directly adding source-to-gate ($C_{sg}$) and drain-to-gate ($C_{dg}$) capacitances using the following expression:

$$C_{ox} = \frac{\partial Q_i}{\partial V_{gs}} \qquad 1$$

$$C_{ox} = \frac{\partial Q_i}{\partial V_{gs}} + \frac{\partial Q_v}{\partial V_{gs}} \qquad 2$$

$$C_{ox} = C_{sg} + C_{ds}$$

The advantage of this method is that both capacitances can be measured independently with appropriate drain bias applied. Since the MOS transistors are symmetric, the source and drain terminals and interchangeable. Charge model [21] one can estimate the voltage

$$Q_i = C_{OX}\left(V_{GS} - V_{FB} - \psi_S - \gamma\sqrt{\psi_S}\right) \qquad 3$$

Where

$$\psi_S = 2\psi_F + \Phi(y) \qquad 4$$

$$\psi_F = \frac{kT}{q}\log\left(\frac{N_A}{N_i}\right) \qquad 5$$

$$\gamma = \frac{\sqrt{2\varepsilon_S q N_A}}{C_{OX}} \qquad 6$$

In (4)-(6) $\psi_S$, is the surface potential, $\psi_F$ is the Fermi potential, and $\boldsymbol{\Phi}$(y) is the potential along the inversion channel region. The average voltage shift be estimated using the following expression by assuming that $\boldsymbol{\psi}_S$ varies linearly in the channel region from $2\boldsymbol{\psi}_F$ to

$2\boldsymbol{\psi}_F + V_{DS}$

$$\Delta V = \frac{V_{DS} + \gamma\sqrt{\psi_S + V_{DS}} - \sqrt{2\psi_F}}{2} \qquad 7$$

Assuming N, = 1.45 x 1010 c m -3 NA, = 3 X $10^{16}$ $cm^{-3}$, and to, = 30 nm, one obtains ΔV = 74 mV which is consistent with the value obtained from conventional and. In accordance with the data presented above, we conclude that the inversion charge is indeed a strong function of the gate and drain biases, and any slight variation of $V_{DS}$ can significantly reduce the inversion charge which due to measurement.

### III RESULT AND DISCUSSION

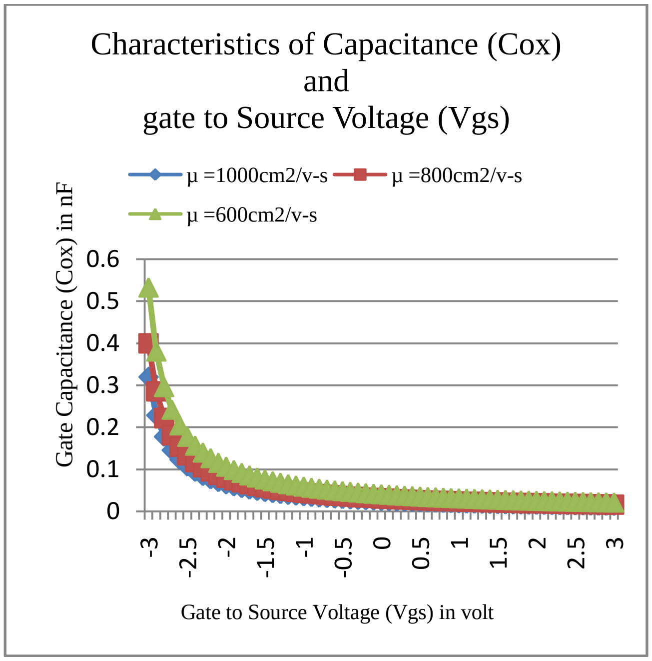

Figure2: Cox-Vgs relationship for different mobilty

Figure2 is the variation between gate capacitance and applied gate to source voltage of the p-type MOSFET here it is clear that when gate to source voltage is negative, its capacitance is big and it is reduced when positive voltages increases.

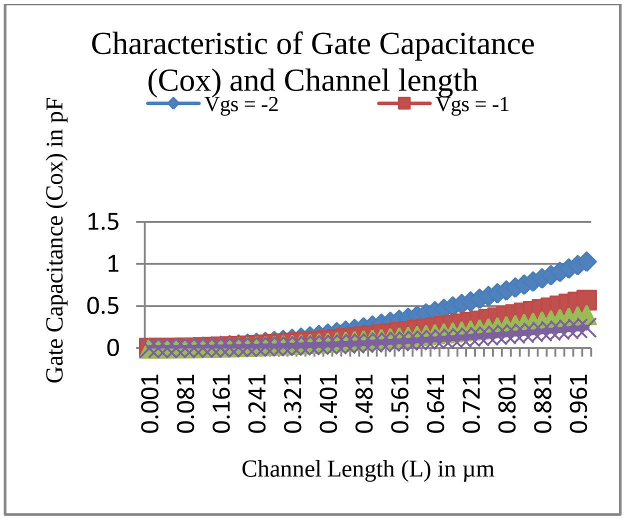

Figure3: Relationship between the gate capacitance

Figure3 shown here that the variation of gate capacitance with channel length of the purposed device. When channel length is small the capacitance is also small because the length of the channel is directly proportional to the capacitance of the device, And increasing the length of the channel the capacitance increases with non linearly.

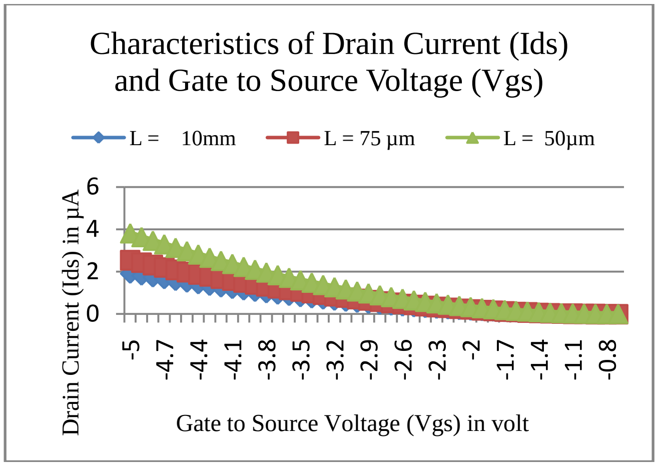

Figure4:Relation between drain current ($I_{ds}$) and gate to source voltage ($V_{gs}$)

Figure4 here shown that Ids- $V_{ds}$ relationship. For P-type MOSFET current is large only when the negative voltage at the gate to source would be large i.e. Drain current would be decreased non linearly when negativity be decreased.

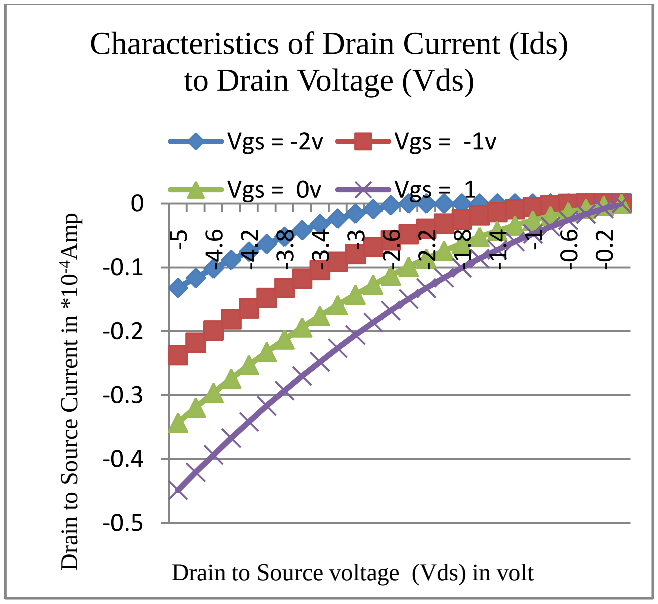

Figure5: Ids-Vds characteristics of P-type MOSFET

Figure5 shown here the current voltage characteristics of the purposed device for the different gate to sources voltages. The drain current increases non linearly with drain to source voltage.

## IV. CONCLUSION

The extraction techniques for evaluating gate capacitance of the device to fast switching. In this paper, technique has been proposed and analyzed the structure for the objectives and developed to obtain speed of device and the simultaneous measurement of $I_{ds}$–$V_{gs}$ and $C_{ox}$–$V_{gs}$.

## REFERENCES

[1] P. D. Chow and K. L. Wang, “A new AC technique for accurate determination of channel charge and mobility in very thin gate MOSFETs,” IEEE Trans. Electron Devices, vol. ED-33, no. 9, pp. 1299–1304, Sep. 1986

[2] J. Koomen, “Investigation of the MOST channel conductance in weak inversion,” Solid State Electron., vol. 16, no. 7, pp. 801–810, 1973.

[3] Z. Ji, J. F. Zhang, W. Zhang, G. Groeseneken, L. Pantisano, S. De Gendt, and M. M. Heyns, “An assessment of the mobility degradation induced by remote charge scattering,” Appl. Phys. Lett., vol. 95, no. 26, pp. 263 502– 263 503, 2009.

[4] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, “High-kappa/metal-gate stack and its MOSFET characteristics,” IEEE Electron Device Lett., vol. 25, no. 6, pp. 408–410, Jun. 2004.

[5] K. Chain, J. Huang, J. Duster, K. K. Ping, and C. Hu, “A MOSFET electron mobility model of wide temperature range (77–400 K) for IC simulation,” Semiconductor Science and Technology, vol. 12, no. 4, p. 355, 1997.

[6] K. Tatsumura, M. Goto, S. Kawanaka, and A. Kinoshita, “Correlation between low-field mobility and high-field carrier velocity in quasi-ballistictransport MISFETS scaled down to Lg = 30 nm,” in IEDM Tech. Dig., 2009, pp. 1–4.

[7] C. G. Sodini, T. W. Ekstedt, and J. L. Moll, “Charge accumulation and mobility in thin dielectric MOS transistors,” Solid State Electron., vol. 25, no. 9, pp. 833–841, 1982.

[8] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R.Wise, “Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing,” IEEE Trans. Electron Devices, vol. 53, no. 5, pp. 944–964, May 2006.

[9] J. F. Zhang, H. K. Sii, G. Groeseneken, and R. Degraeve, “Hole trapping and trap generation in the gate silicon dioxide,” IEEE Trans. Electron Devices, vol. 48, no. 6, pp. 1127–1135, 2001.

[10] J. F. Zhang, H. K. Sii, G. Groesendeken, and R. Degraeve, “Degradation of oxides and oxynitrides under hot hole stress,” IEEE Trans. Electron Devices, vol. 47, no. 2, pp. 378–386, 2000.

[11] J. Wang, N. Kistler, J. Woo, and C. R. Viswanathan, “Mobility-field behavior of fully depleted SOI MOSFETs,” IEEE Electron Device Lett., vol. 15, no. 4, pp. 117–119, Apr. 1994.

[12] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, “On the universality of inversion layer mobility in Si MOSFETs: Part I—Effects of substrate impurity concentration,” IEEE Trans. Electron Devices, vol. 41, no. 12, pp. 2357–2362, Dec. 1994.

[13] V. Kilchytska, D. Lederer, N. Collaert, J. P. Raskin, and D. Flandre, “Accurate effective mobility extraction by split C–V technique in SOI MOSFETs: Suppression of the influence of floating-body effects,” IEEE Electron Device Lett., vol. 26, no. 10, pp. 749–751, Oct. 2005.

[14] J. Ramos, E. Augendre, A. Kottantharayil, A. Mercha, E. Simoen, M. Rosmeulen, S. Severi, C. Kerner, T. Chiarella, A. Nackaerts, I. Ferain, T. Hoffmann, M. Jurczak, and S. Biesemans, “Experimental evidence of short-channel electron mobility degradation caused by interface charges located at the gate-edge of triple-gate FinFETs,” in Proc. ICSICT, 2006, pp. 72–74.

[15] C. L. Huang, J. V. Faricelli, and N. D. Arora, “A new technique for measuring MOSFET inversion layer mobility,” IEEE Trans. Electron Devices, vol. 40, no. 6, pp. 1134–1139, Jun. 1993.

[16] J. Koga, S. Takagi, and A. Toriumi, “Different contribution of interface states and substrate impurities to Coulomb scattering in Si MOS inversion layer,” in Proc. Int. Conf. Solid State Devices Mater., 1994, pp. 895–897.

[17] S. M. Thomas, T. E.Whall, E. H. C. Parker, D. R. Leadley, R. J. P. Lander, G. Vellianitis, and J. R.Watling, “Accurate effective mobility extraction in SOI MOS transistors,” in Proc. Ultimate Integr. Silicon, 2009, pp. 31–34.

[18] M. P. Morgensen and L. M. Lunardi, “Analytical correction for effective mobility measurements in MOSFETs,” IEEE Trans. Electron Devices, vol. 58, no. 9, pp. 2871–2873, Sep. 2011.

[19] H. Ishiuchi. Y. Matsumoto, $. Sawada, and 0. Ozawa, “Measurement of intrinsic capacitance of lightly doped drain (LDD) MOSFET’s,” IEEE Trans. Electron Devices, vol. ED-32, pp. 2238-2242, 1985.

[20] Y:T. Yeow, “Measurement and numerical modeling of short-channe1 MOSFET gate capacitance,” IEEE Trans. Electron Devices, vol.

[21] S. Selberherr, A. Schutz, and H. Potzl, “MINIMOS-A two-dimensional MOS transistor analyzer, ” IEEE Trans. Electron Devices, vol. 1131 Y. P. Tsividis, Operatiop and Modeling of the MOS Transistors.
New York: Mcgraw-Hill, 1987, ch. 2.

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