ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 2, Issue 6, June 2013

An HVD Based Error Detection and Correction Code in HDLC Protocol Used for Communication

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Abstract: With the increase of data transmission and hence sources of noise and interference, engineers have been struggling with the demand for more efficient and reliable techniques for detecting and correcting errors in received data. Although several techniques and approaches have been proposed and applied in the last decade, data reliability in transmission is still a problem. In this report propose a high efficient combined error detection and correction technique based on the horizontal-vertical diagonal (HVD) parity check in HDLC. This method has been experimentally implemented and simulated using Field Programmable Gate Array .Simulation results show that the proposed technique detects 99.99% of the errors and corrects as predicted up to three bits of errors in the received impaired n-bit code. An independent design platform is utilized for the simulation by Xilinx 8.1 using ModelSim SE-EE 5.4a coded in VHDL which shows a significant reduction in uncorrected errors during data transmission. The efficient performance of HVD makes it a more applicable coding technique for communication, data transmission, different protocols and other application.

Keywords: EDAC (Error Detection and Correction), FPGA (Field Programmable Gate Array), HDLC (High Data Control Protocol), HVD (Horizontal Vertical Diagonal), ModelSim, VHDL (VHSIC Hardware Descriptive Language), Xilinx.

I. INTRODUCTION

Error detection and correction (EDAC) techniques are used to ensure that data is correct and has not been corrupted, either by hardware failures or by noise occurring during transmission or a data read operation from Memory. There are many different error correction codes in existence. The reason for the different codes being used in different applications has to do with the historical development of the data storage, the types of data errors occurring, and the overhead associated with each of the error detection techniques. The basic concept of error detection and correction method is as follow 1.Networks must be able to transfer data from one system to another without data can be corrupted during transmission. 2. For reliable communication, errors must be detected and corrected. 3. Error detection and correction are implemented either at the data link layer or the transport layer of the OSI model.

In this paper implement an error correction and detection techniques in high-level data link control (HDLC) using VHSIC Hardware Descriptive Language. Layer two of the OSI model is the data link layer, and the most commonly used protocol is the HDLC protocol.

A bit orientated protocol sends information as a sequence of bits. An example of a bit orientated protocol is HDLC. Frames are used as a transport mechanism to transport data from one point to another. A frame contains error checking information which allows data to be sent reliably from a sender to a receiver. HDLC is one of the most enduring and fundamental standards in Communications. HDLC is in itself a group of several protocols or rules for transmitting data between network points. The HDLC protocol also manages the flow or pace at which the data is sent. The data is organized into a unit called a frame. Some of the key operations of the HDLC protocol implemented are handling bit oriented protocol structure and formatting data as per the packet switching protocol, it includes Transmitting and receiving the packet data serially [1].

The HDLC (High-level Data Link Control), developed by the ISO, is bit-oriented protocol of link layer. It shows many characteristics, such as powerful error detection, high efficiency and synchronous transmission, etc. And it is one of the most popular protocols in the field of communication. It is a transmission protocol used at the data link layer (layer 2) of the OSI seven layer model for data

ISSN (Print) : 2319-5940
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communications. The HDLC protocol embeds information in a data frame that allows devices to control data flow and correct errors.

The HDLC frame is synchronous and therefore relies on the physical layer to provide method of clocking and synchronizing the transmission and reception of frames. The frames are separated by HDLC flag sequences that are transmitted between each frame and whenever there is no data to be transmitted. The header of the packet contains an HDLC address and an HDLC control field.

The trailer is found at the end of the frame, and contains a Cyclic Redundancy Check (CRC), which detects any errors that may occur during transmission. A CRC value is generated by a calculation that is performed at the source device. The destination device compares this value to its own calculation to determine whether errors occurred during transmission.

In normal HDLC protocol made, all received frames are presented to the host on the output register. A status register is provided which can be used to monitor the status of the receiver channel, and indicates if the packet currently being received includes any errors. HDLC has three operational modes. These modes are Normal Response Mode (NRM), Asynchronous Response Mode (ARM) and Asynchronous Balanced Mode (ABM).Normal Response Mode refers to the standard primary-secondary relationship. In this mode, a secondary device must have permission from the primary device before transmitting. Once permission from the secondary has been granted, the secondary may initiate a response transmission of one or more frames containing data [2].

The paper is organized as, the related work that has been done previously is given in section 2, the proposed method of error detection and correction is described in the section 3, results are given in section 4 and in the end of the paper, paper is concluded in the section 5.

II. PREVIOUS WORKS

In order to maintain good level of reliability, it is necessary to protect memory cells using protection codes, for this purpose, various error detection and correction methods are being used. The method used in [3], is based on the hardware and time redundancy, although this technique reduces the number of input and output pins of the combinational logic; it requires additional encoding/decoding circuitry. The reliability issue can be solved, but the hardware redundancy schemes like duplication or triple modular redundancies are expensive. In [4], the encoder and the decoder can use any error detection and correction code. But the data is only coded in write operations, and decoded in read operations. So, the accumulation of upsets is likely to occur and it depends on the reading and writing application request frequency. In order to avoid this accumulation of upsets, it is necessary to use an extra logic which is able to constantly detect and correct upsets in all coded data. The EDAC method given in [5] is again based on TMR, so increases the density as it is a hardware redundancy method. The method given in [6] reduces power consumption in single-error correcting, double error-detecting checker circuits that perform memory error correction code. This method can be employed to solve the non linear power optimization problem but it involves tedious computation of H- matrix.

The method in [6], which is named HVD, provides very high detection coverage rate that can correct up to three upsets in a data array. It uses parity codes in four directions in a data part to assure the reliability of memories and it can detect and correct the errors in real data bits. If the parity bit is itself erroneous, then that error is detected by generating the parity bits for parities that is syndrome bits, but this is a complicated process. An easy way to find the errors in parity bits is presented in this paper. For this, we can take data bits and parity bits as a whole word. These words can be viewed as an m x n array. The hamming code will be used for the error detection and correction for this whole word containing both the data bits and the parity bits across the length of array. After finding the error, it can be detected whether it is a data bit or a parity bit.

III. PROPOSED METHOD

The proposed detection and correction method is called HVD code (which is used in the place of CRC in a HDLC protocol) since the parity bits are applied on the row, column and two diagonals on a data part. In addition to horizontal (H) and vertical (V) parity bits, we use diagonal (D) parity bits in two directions as shown in figure 1.In order to increase the detection ability, an additional parity bit is computed based on calculated parity bits of each dimension. In our HVD code implementation, h, v, d and d represent the number of errors in the horizontal, vertical and slash and backslash lines respectively. A. Error Detection Method.

EDAC method is used in HDLC protocol. For these purpose here we are using HDLC frame, the term frame to indicate the independent entity of data transmitted across the link from one station to another. Figure 2 shows the frame format. The frame consists of four or five fields.

ISSN (Print) : 2319-5940
ISSN (Online) : 2278-1021

International Journal of Advanced Research in Computer and Communication Engineering
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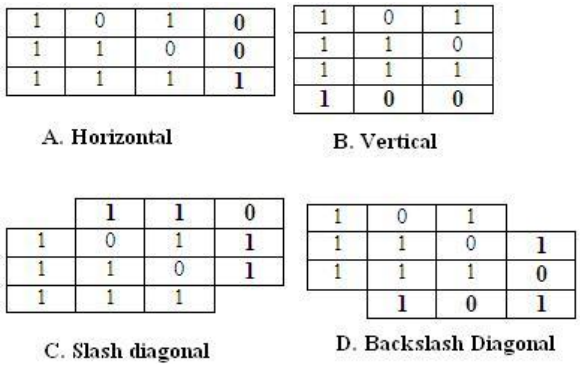

Figure 1:
The horizontal, vertical, slash and backslash diagonal dimension parity scheme in HVD

Flag	Address	Control	Information	FCS	Flag
1Byte	1 or 2Byte	1Byte		2 or 4Byte	1Byte

Figure 2: HDLC frame field and their size

A. Detection Method

For the HDLC frame, parities are calculated in all the directions at the receiver end (for example, from $v_{1 \text{ to }} v_{8 \text{ in}}$ vertical direction). These calculated parities are compared against the actual received parities. If the result of comparison does not show any difference, it means the received data at the receiver is correct so no correction is required; but if there is a difference between the received and calculated parities, the erroneous parity lines are identified and then the correction process starts.

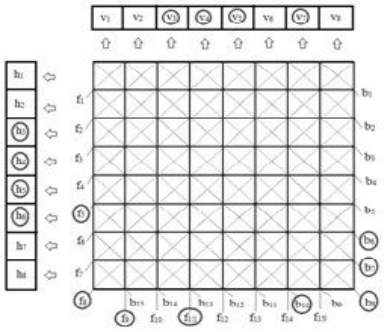

Figure 3: Coded array with erroneous parities

B. Correction Method

At the end of the detection process, the erroneous parity lines are marked with a circle as shown in above figure 3. For correction, first the candidate bits are marked. Wherever atleast two of the four erroneous parity lines intersect, that bit in array is marked as candidate bit. Candidate bits for the erroneous parity lines are shown with black squares in figure 4.

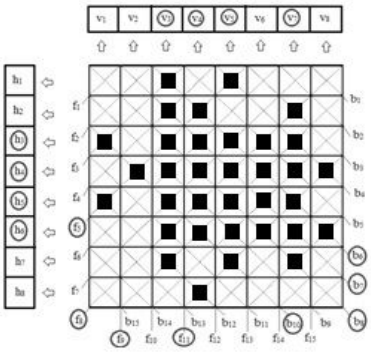

Figure 4: Coded array with data bits

To find the erroneous bits among the candidate bits, all the candidate bits are checked. The candidate bit for which all the four lines intersect, is an erroneous bit; if not then the bit is correct. This particular candidate bit can be removed. The error bits for the set of candidate bits in figure 4 are shown with dark circles in figure 5.These erroneous bits are flipped to correct.

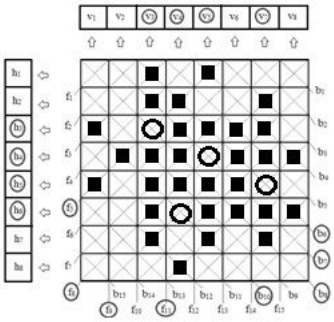

Figure 5: Coded array with error bits

To find whether the erroneous bits are data bits or parity bits, the error bits can be checked as, if the position of the erroneous bit is 2^k (for k = 0, 1, 2, 3….), then it is an erroneous parity bit otherwise it is a data bit that is erroneous.

IV. RESULT

This method is simulating in Xilinx 8.1 using ModelSim SE-EE 5.4a platform and the robustness of the technique

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is evaluated by random error incorporation. The results show that, a large combination of multiple errors can be corrected. The number of errors that can be corrected depends upon the length of the array of coded word. It increases with the length of the array.

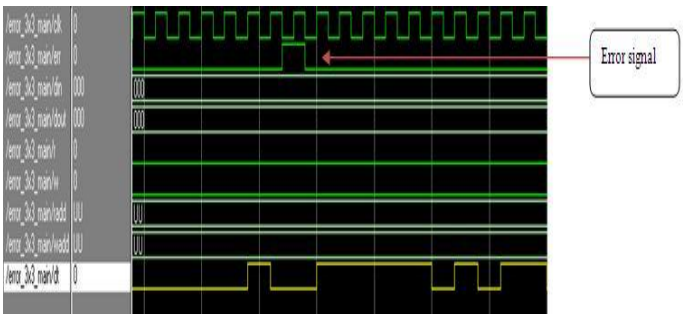

Figure 6: Simulation result when error signal is high

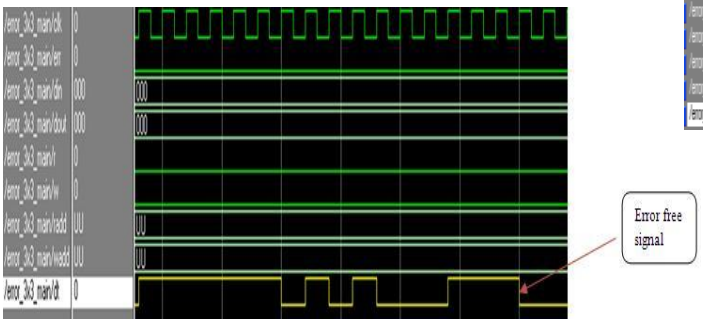

Figure 7: Simulation result for correction function

The VHDL codes for correction function are simulated for various lengths of code such as 4, 9, 16, 32 and 64 bit code. Simulation result, error is high (at the receiver end) is given in above Figure 6. The simulation results after error detection and correction in a 3x3 data array is given in the figure 7.There is no need of extra calculations of syndrome bits for parity bits as needed in [7].

A. Hardware Analysis

This method requires only 2 adders, 1 multiplexer and 3 XOR gates for different length of code. It does not require any other extra hardware as needed in [3] and [4], as it is not a hardware redundant method. As shown in figure 8

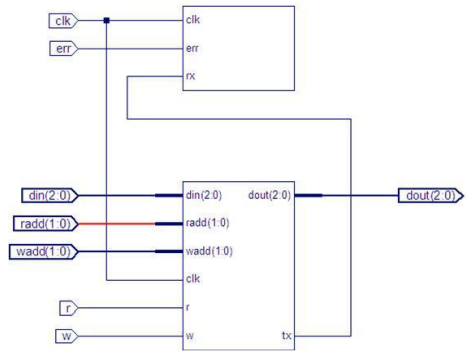

Figure 8: RTL view of HVD

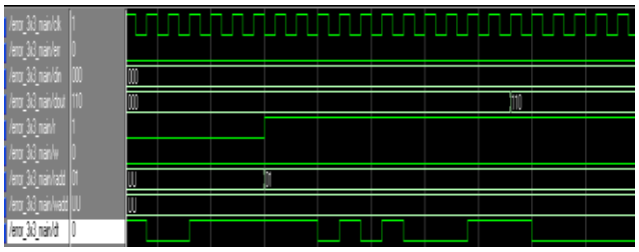

Figure 9: Simulation result for Read operation

B. Code Rate

The code rate can be defined as; "the measure of relative amount of information which is transmitted in each codeword" .It is an important metric to evaluate the performance of any error detecting & correcting code. For a good error detection and correction method should have more code rate. In The variation in code rate for different bits is shown with blue line in figure 10 [1].

Code Rate = (R) =Data Bits (k)/ Total number of bits (n)

Where k is data bits and n is total number of bits in the codeword.

C. Bit overhead

Another important measure to compare the two codes is the bit overhead. The bit overhead (BO) can be defined as, "the ratio of parity bits to data bits". Bit overhead determines the percentage of redundancy in the codeword. A good error correction and detection method should have lesser bit overhead. With the proposed method, we can get the reduced bit overhead as shown with red line in the figure 10 [1].

Bit Overhead = BO = Parity bits (c) / Data bits (k)

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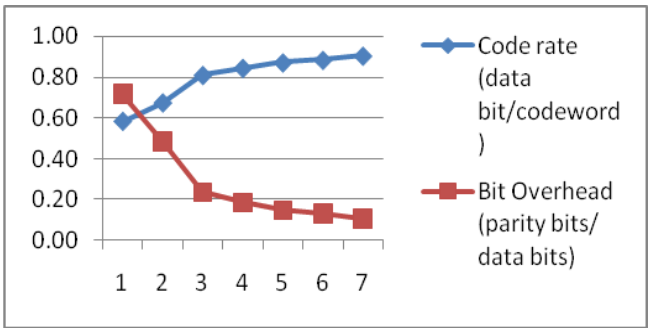

Figure 10: Code rate and Bit overhead for various bits

V. CONCLUSIONS

In this paper an easy method with lesser computations is presented. It is a simpler method of finding the errors by removal of error bits, so reduces the complexity. This method can detect and correct the errors in data bits as well as in the parity bits without any extra calculations. This paper presents a high-level error detection and correction method which is called HVD code. This type of detection and correction code uses the parity code in four directions in a data array. All of multiple error bit flips can be detected and 3-bit errors can be corrected, based on the experimental results. With the help of this HDLC Controller perform read and write operation from the particular memory location, as showing in above figure 9. Also design error detection and correction code for parity bit.

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BIOGRAPHY

Shubham Fadnavis was born in India. In 1983, she got her Bachelor's Degree in Electronics & Communication Engineering from SDITS, Khandwa (M.P) in 2008.Currently she is pursuing her Master's Degree in Digital Communication from AITR, Indore (M.P)