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An Enhanced (15,5) BCH Decoder Using Verilog HDL

M. Prashanthi[1], P. Samundiswary[2]

M. Tech, Department of Electronics Engineering, Pondicherry University, Pondicherry, India[1]

Assistant Professor, Department of Electronics Engineering, Pondicherry University, Pondicherry, India [2]

Abstract:Error-correction codes are the codes used to correct the errors occurred during the transmission of the data in the unreliable communication mediums. The idea behind these codes is to add redundancy bits to the data being transmitted so that even if some errors occur due to noise in the channel, the data can be correctly received at the destination end. Bose, Ray- Chaudhuri, Hocquenghem (BCH)codes are one of the error-correcting codes. The BCH decoder consists of four blocks namely syndrome block, IBM block, chien search block and error correction block. This paper describes a new method for error detection in syndrome and chien search block of BCH decoder. The proposed syndrome block is used to reduce the number of computation by calculating the even number syndromes from the corresponding odd number syndromes. The new factorization method used to implement the algorithm of chien search block of enhanced BCH decoder reduces the number of components required. Thus, a new model of BCH decoder is proposed to reduce the area and simplify the computational scheduling of both syndrome and chien search blocks without parallelism leading to high throughput. The enhanced chase BCH decoder is designed using hardware description language called Verilog and synthesized in Xilinx ISE 13.2.

Keywords: BCH Codes, Syndrome Block, Chien search Block, Error detection

I. INTRODUCTION

The information theory and coding theory are used in computer communication and telecommunication applications. Error correction and detection are the techniques used in the above mentioned applications that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subjected to channel noise which introduces the errors during transmission of messages from the source to receiver [1][6].
The channel coding theory states that the reliable transmission is achievable by performing proper coding. “Channel Coding” is the technique, which is used to sustain the originality of the information bits, to avoid the re-transmission of information bits as well as to detect and correct any error which has been occurred during transmission.
Error detection is the detection of errors caused by noise or other impairments during transmission from the transmitter to the receiver.It uses the concept of redundancy[8], which means adding of extra bits for detectingerrors at the destination. In error correction the receiver can use any of the error-correcting code, which can automatically corrects certain errors and enables reconstruction of the original data.

A. Detection Methods

1) *Repetition codes:*

A repetition code is coding scheme that repeats the bit across a channel to achieve error-free communication. Repetition codes are very inefficient and can be susceptible to problems if the error occurs in exactly the same place for each group.

2) *Cyclic Redundancy Checks (CRC):*

A CRC is a single-burst error –detecting cyclic code designed to detect accidental changes to design to detect accidental changes to digital data in computer networks. It is not preferable for detecting maliciously introduced errors.

3) *Parity Bit:*

These are the simplest form of error-detecting code. They can detect single or any other odd number of errors in the output. Even parity is a special case of a cyclic redundancy check (CRC), where the 1-bit CRC is generated by the polynomial $x+1$.

B Correction Methods

1) *Automatic Repeat Request (ARQ):*

Automatic Repeat request (ARQ) is an error control method for data transmission that makes use of error-detection codes, acknowledgment and negative acknowledgment messages and timeouts to achieve reliable data transmission. ARQ is appropriate if the communication channel has varying or unknown capacity. It requires the availability of a

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channel, results in possibly increased latency due to retransmissions and requires the maintenance of buffers and timers for retransmissions.

2) Forward Error Correction (FEC):

An error-correcting code (ECC) or forward error correction (FEC) code is a system of adding redundant data or parity data, to a message, so that the message can be recovered by a receiver even when a number of errors are introduced, during the process of transmission.Aback-channel is not required in forward error correction since the receiver does not have to ask the sender for retransmission of the data [9] [10].
Error-Correcting codes are futureclassified into two major class of codes such as convolutional codes and block codes:

Convolutional codes:
They are processed on a bit-by-bit basis. They are suitable for implementation in hardware and many algorithms exist for decoding these codes. The Viterbi algorithm provides high performance.Thus the Viterbi decoder is commonly used which allows optimal decoding.

Block Codes:
The block codes are implemented as (n, k) codes where n indicates the codeword and the k defines the original information bits. Therefore, the numbers of redundant bits need to be added in to the original message bits are given as (n-k) the block codes are fixed channel codes.BCH codes are subset of the Block codes.

The objective of this work is to reduce the number of components used in both in syndrome and chien search blocks[5] [3].The new factorization method which allowed to conceive another chien search block with reduced number of logic gates.

This paper is organized as follows; Section II explains the existing BCH decoder and section III explains the modified BCH decoder and detailed structure of syndrome and Chien search respectively. Section IV shows the simulation results of the enhanced BCH decoder. Results are analysed in the section V. Section VI is drawn with the conclusion.

II. EXISTING BCH DECODER

A. BCH Codes

BCH codes is an abbreviation for Bose, Ray- Chaudhuri, Hocquenghem, invented in 1960s and today they are used as a baseline for many recent Error Correcting codes. They are the powerful class of multiple error correction codes with well-defined mathematical properties. BCH code can correct multiple random error patterns. Galois Field or Finite Field Theory is the mathematical properties within which BCH codes are defined.
The finite field has the property that any arithmetic operations on field elements always have results in the field only. To provide an excellent error correcting capability, the generator polynomial of the BCH codes has carefully specified roots. With a generator polynomial of g(x), t- errors correcting cyclic codes are the binary BCH codes; with a condition that g(x) must be the least degree polynomial over Galosis Field GF (2). The block length of the BCH code, constructed over GF (2^m) is given by n= 2^m – 1.

The BCH decodershown in figure1 has four modules [1] namely: syndrome calculator, Inversionless Berlekamp Algorithm, Chien search and error correction.

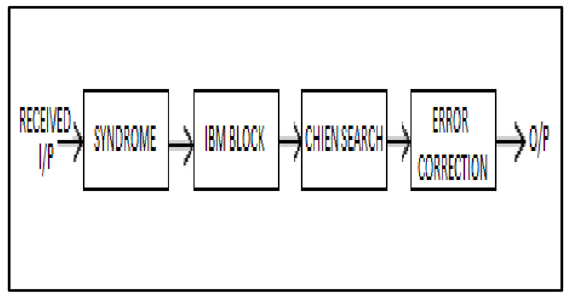

Figure 1: Block Diagram of BCH Decoder

B. Syndrome Calculator

The syndrome calculator is the first module at the decoder, the design of this module is almost same for all the BCH decoder architectures. The input to the module is corrupted codeword[2]. The equation for the code word, received both and the error bits are given as below:

Codeword equation

$$c(x) = c_0 + c_1 x + c_2 x^2 + \cdots + c_{n-1} x^{n-1} \quad \dots (1)$$

Received bits equation

$$r(x) = r_0 + r_1 x + r_2 x^2 + \cdots + r_{n-1} x^{n-1} \quad \dots (2)$$

Error bits equation

$$e(x) = e_0 + e_1 x + e_2 x^2 + \cdots + e_{n-1} x^{n-1} \quad \dots (3)$$

Thus, the final transmitted data polynomial equation is given as below:

$$r(x) = c(x) + e(x) \quad \dots (4)$$

The 1st step at the decoding process is to store the transmitted data polynomial in the buffer register and then to calculate the syndrome S_j. The important characteristics of the syndrome are that theydepends on only error location [8]] not on transmitted information. The equations of the syndromes is given below

S_j indicates the syndrome is denoted as

$$S_j = \sum_{i=0}^{n-1} r_i \alpha^{i.j} \qquad for\ (1 \le j \le 2t) \quad \dots (5)$$

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From the equation it is observed that the syndromes are depends on only error polynomial e(x), so if there is no errors occurs during the transmission then all the generated syndromes will be zero.
The architecture of the syndrome calculator is shown in Figure 2.

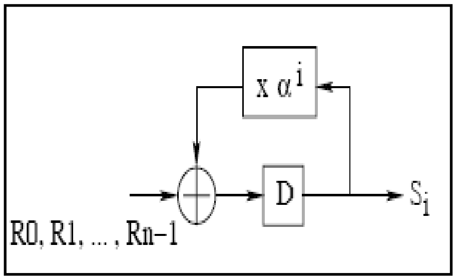

Figure 2: Syndrome Calculator

C. *Inversion less Berlemkamps Algorithm:*

The second stage in the decoding process is to find the co-efficient of the error location polynomial using the generated syndromes in the previous stage. The error location polynomial is given as

$$\sigma(x) = \sigma_0 + \sigma_1 x + \cdots \sigma_t x^t \qquad ...(6)$$

The relation between syndromes and the error location polynomial is given as below

$$\sum_{j=0}^{t} s_{t+i-j}\sigma_j = 0 \quad for\ (i = 1,2 \ldots\ldots t) \qquad ...(7)$$

There are various algorithms used to solve the key equation solver[1]. Here the inversion less Berlekamp Massey algorithm is used to solve the key equation.

The decoder of this paper is based on the Inversion-less Berlekamp algorithm (IBM) for key equation calculation[7].

D. *Chien Search*

The error location is the next step of decoding process, which can be done by using chien search block.

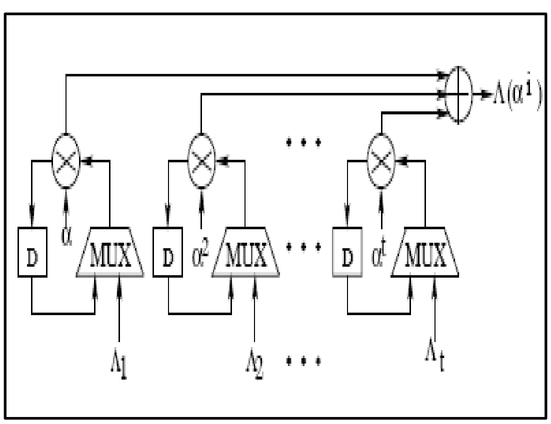

Figure 3:*ChienSearch Architecture-Error Location*

To locate the roots of the polynomial, chien search block is implemented in hardware for the BCH decoder [3]. The chien search block has a property that the roots are going to be a power of α reducing the evolution of the polynomial for every root[9]. So, the use of the chien search block provide the computational benefits of the step,

$$\Lambda_i^j = \Lambda_i^{(j-1)}\alpha^i \qquad ...(8)$$

This property makes the chien search method more superior than the other methods.

E. *Error Correction*

The output of the chien search block is called roots of equation. The reciprocal of the roots of equations are added with the corresponding location of the corrupted codeword received by decoder[4]. The result of this addition is the original codeword that was encoded by the encoder before transmission.

III. ENHANCED BCH DECODER

A. *Syndrome Calculator:*

The newly developed syndrome is easy to compute and provide a simple and scalable approach. There will be 2t syndromes which can be corrected by the decoder. It's quite exhaustive to find 2t syndromes, but from the equation

$$s_{2t} = (s_t)^2 \qquad ...(9)$$

The even numbered syndrome can be computed from the corresponding odd numbered syndromes.Hence, it only needs to compute t syndromes instead of 2t syndromes.As the number of calculated syndromes reduces, the area needed for BCH decoder is also decreased.

B. *Chien Search:*

This algorithm can detect the error position by calculating

$$\Lambda(\alpha^i)\ \ for(0 \le i \le n-1) \qquad ...(10)$$

Where, $\Lambda(x)$is the error locator polynomial.

For the case of(n,k) it is necessary to calculate:

$$\Lambda(\alpha^{(n-1)}, \Lambda(\alpha^{(n-2)}, \ldots\ldots\ldots\ldots \Lambda(\alpha^{(0)} \qquad ...(11)$$

If the expression reduces to $\pi(\alpha^i) = 0$, the that value of x is a root and identifies the error position else the position does not contain any error.

1) *Factorization Method:*

In this method,(Λ) the error locator polynomial is factorized such that it is not depicted in itsexpression, which allows to conceive another form of the circuit of the Chien search that minimize a large number of the used logic gates in the circuit .

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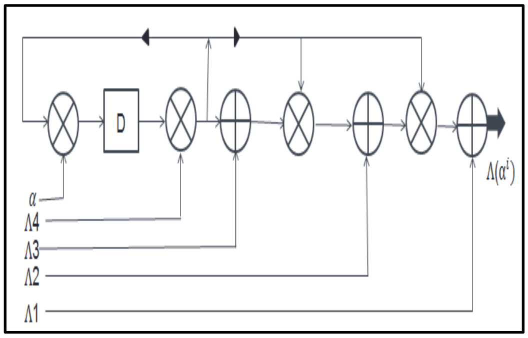

Figure 4:Chien Search Architecture-Error Location

IV. SIMULATION RESULTS

Simulation is carried out using Xilinx ISE 13.2 design suit tool with Spartan 3E as the target device. Simulation results of (15,5) BCH decoder are discussed below.

A. Syndrome:

The syndrome block is the first block of the BCH decoder. It depends on the error location than the transmitted information[2].The number of calculated syndromes according to the algorithm will be six from s1 to s6 as shown in the below figure 5.

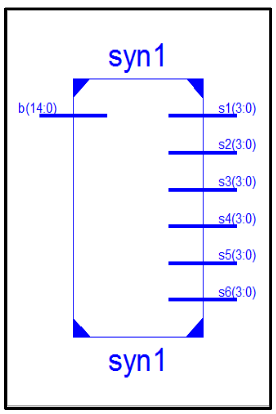

Figure 5: RTL Top View ofSyndrome

In the above figure 5, b[14:0] is the 15 bit received corrupted input ands1[3:0] to s6[3:0] is the six 4bit syndrome block output.

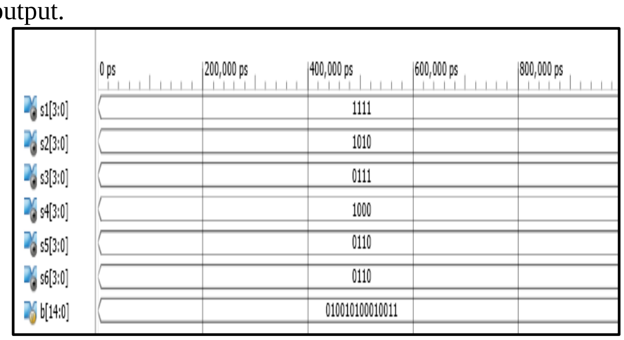

Figure 6: TimingWaveform of Syndrome

B. Inversion less Berlemkamps Algorithm(IBM):

The syndrome outputs will be the input to the IBM block which generates four co-efficient of the error location polynomial having length of four bits i.e. from lambda0 to lambda3 as shown in figure 7.

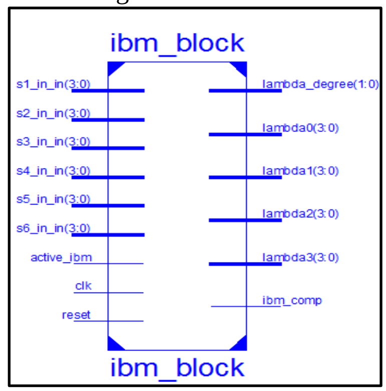

Figure7: RTL Top View ofIBM

It is observed through the RTL Top view of IBM block that s1_in_in to s6_in_in,clk,reset are the IBM outputs and lambda0 to lambda3 having length of 4bits are outputs along with the lambda degree which indicates the polynomial degree.

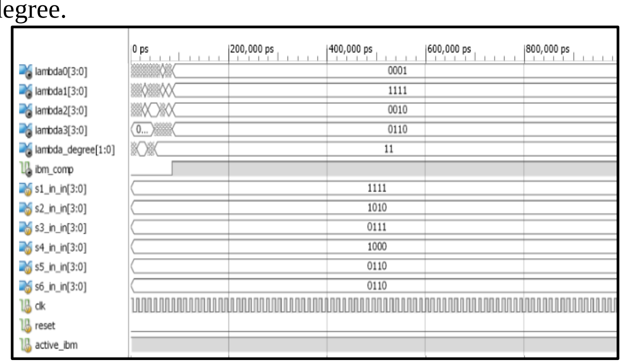

Figure 8:TimingWaveform of IBM

C. Chien Search:

The IBM block outputs are the inputs to the chien search block which generates 15 bit results that shows the exact position where the errors are present.

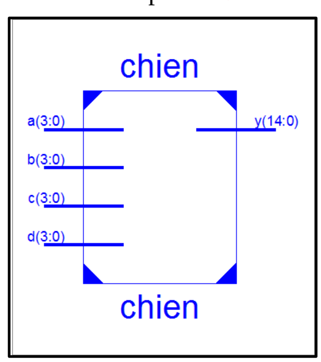

Figure8: RTL Top View ofChien Search

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a,b,c,d in the above figure 8 are the chien search block inputs each of 4 bits and y[14:0] is the 15 bit output which shows the exact error location.

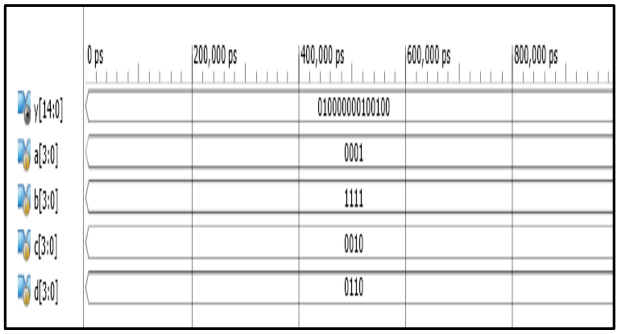

Figure 9: Timing Waveform ofChien Search

D. Error Correction:

Here the chien search output is EX-ORed with the received data that gives the output which is the uncorrupted data.

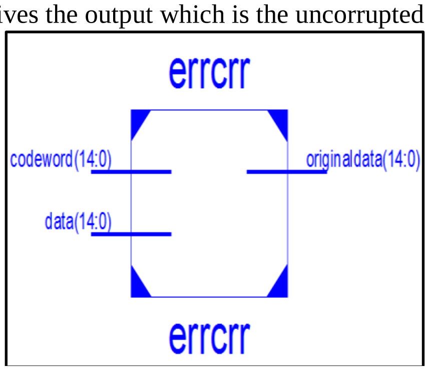

Figure 10: RTL Top View ofError Correction

The variable data in figure 10 is the received corrupted input at the decoder and codeword which is the output of the chien search are the inputs to the error-correction block which gives uncorrupted original data as the output.

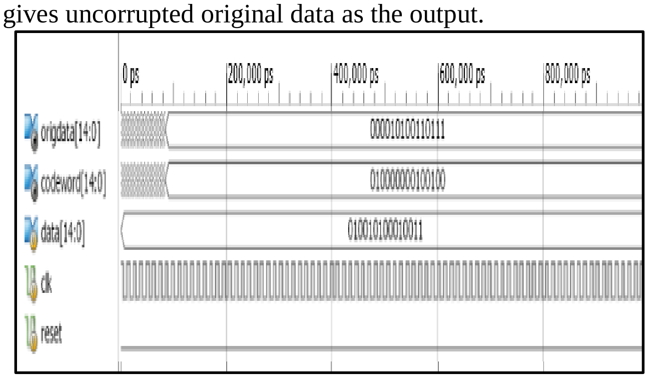

Figure 11: Timing Waveform ofError Correction

E. BCH decoder:

Figure 11 shows the complete BCH decoder block with integration of all the internal blocks with input as the 15 bits received as corrupted data and output as the uncorrupted original data.

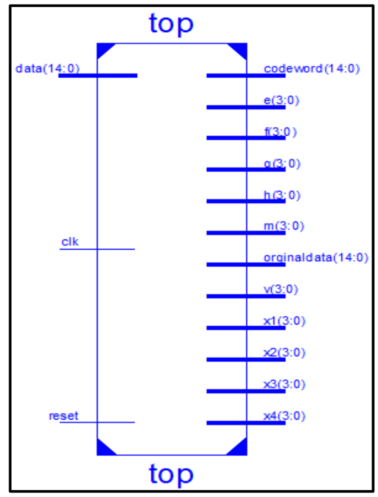

Figure 11: RTL Top View of BCH Decoder

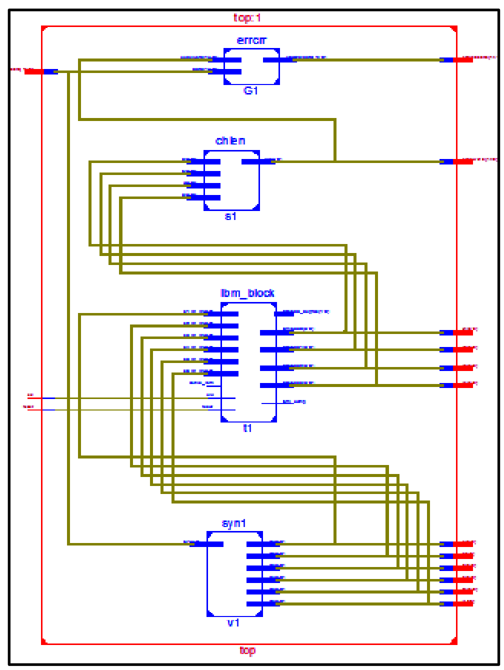

Figure 12: RTL Internal View ofBCH Decoder

Figure 12 shows the internal block diagram of the complete BCH decoder consists of syndrome block, IBM block, chien block and the error correction block which are interconnected with each other.

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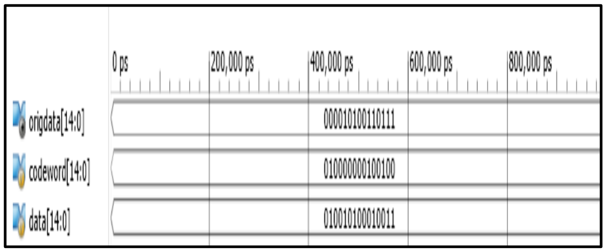

Figure 13: Timing Waveform of BCH Decoder

V. PERFORMANCE ANALYSIS

Table 1: Comparison of the Existing and Proposed Model

Block	No Of Slices		4 Input LUT		Delay(ns)	
	Existing	Proposed	Existing	Proposed	Existing	Proposed
BCH DECODER	334	303	604	562	8.32	8.72
SYNDROME	25	19	43	33	8.06	8.27
CHIEN SEARCH	98	81	31	14	9.94	10.792

The above table 1 shows the major disadvantage of existing model which occupies more area than the proposed model.The proposed model has reduced no of slices and no of 4 input Look Up Tables (LUTs). Thus the enhanced BCH decoder has reduced area compared to that of existing model.

VI. CONCLUSION

In this paper, an enhanced BCH decoder is simulated in Xilinx ISE 13.2 by replacing the syndrome and Chien search block of the existing BCH decoder with the new syndrome and Chien search block. From the performance analysis done through the simulation, it is observed that the enhanced BCH decoder reduces the area in terms of slices and LUTs which in turn simplify the computational scheduling of the syndrome and chien search leading to high throughput.

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BIOGRAPHIES

M.Prashanthi obtained her B.Tech degree (2011) in Electronics and communication Engineering from Aurora's Technological and Research Institute, Parvatapur, uppal affiliated to Jawaharlal Nehru Technological University, Hyderabad. Currently, pursing M.Tech degree (2013) in the Dept. of Electronics Engineering, School of Engineering and Technology, Pondicherry University, Pondicherry, India.

P.Samundiswary received the B.Tech degree (1997), M.Tech degree (2003) and Ph.D. (2011) in the department of Electronics and Communication Engineering from Pondicherry Engineering College affiliated to Pondicherry University, India. She is having 15 years of teaching experience. She is currently working as Assistant Professor in the Dept. of Electronics Engineering, School of Engineering and Technology, Pondicherry University, Pondicherry, India. Her research interests include Wireless Communication and Wireless Networks.