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Method for a Fast-Lock Low-Jitter Delay-Locked Loop using a Dual Charge Pump and Lock Control Circuit

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Abstract: Author has described a method for a fast-lock low-jitter delay-locked loop using a dual charge pump and lock control circuit. Benefits include improved functionality, improved performance, and improved cost effectiveness.

Keywords: Charge pump, Loop filter, Phase frequency detector (PFD), VCDL

I. BACKGROUND

Conventionally, phase-locked loops (PLL) and delay-locked loops (DLL) are used for the clock synchronization. The locking time and the jitter performance are important characteristics. DLLs are preferred over PLLs in applications without clock multiplication due to the DLLs' stability and faster locking time. Because the noise in the voltage-controlled delay line (VCDL) does not accumulate over many clock cycles, DLLs offer better jitter performance than PLLs. The fast locking and low jitter enable a system to reduce the wait time required before it can operate.

A typical building block of a conventional DLL is comprised of the following:

- Phase frequency detector (PFD)
- Charge pump
- Loop filter
- VCDL
- Additional circuitry to overcome the problem of a limited locking range

II. GENERAL DESCRIPTION

The disclosed method is a fast-lock low-jitter delay-locked loop using a dual charge pump and lock control circuit. The method uses two types of loop tuning, the fine-tuning loop and a coarse tuning loop. The coarse-tuning loop is used to reduce the lock time, and the fine-tuning loop is used when the DLL is close to lock to reduce the output jitter.

The method provides a clock deskewing buffer in microprocessor or memory applications.
The key elements of the disclosed method include:

- Sequential PFDs
- Precharged PFDs
- Two charge pumps
- Adjustable pulse width circuit
- Lock control circuit

III. ADVANTAGES

The disclosed method provides advantages, including:

- Improved functionality due to providing a fast-lock low-jitter delay-locked loop using a dual charge pump and lock control circuit.
- Improved functionality due to providing an adjustable tuning point between coarse and fine tuning.
- Improved functionality due to reducing the silicon surface area required.
- Improved performance due to providing fast locking.
- Improved performance due to reducing jitter.
- Improved cost effectiveness due to using a small chip area, reducing the cost of fabrication.

IV. DETAILED DESCIPTION

The method is a fast-lock low-jitter delay-locked loop using a dual charge pump and lock control circuit. The method uses two PFDs and two charge pumps. One PFD is sequential and one is precharged. The system uses an adjustable pulse width circuit to turn off the coarse charge pump when the loop is close to lock.

Two charge-pump (fine and coarse) paths reduce the locking time. The VCDL delay is controlled by Vc, which is produced by the fine-tuning and the coarse-tuning loop. The

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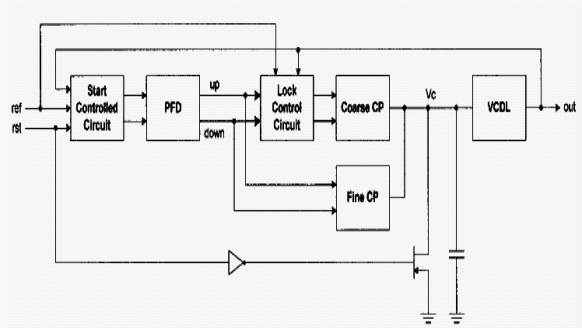


coarse tuning loop is comprised of the lock control circuit, the coarse charge pump, and the fine charge pump. The fine tuning loop is comprised of only the fine charge pump. The coarse charge pump outputs a larger amount of current to the loop filter as compared to the fine charge pump (Figure 1).

When the DLL is in the out-of-lock state, coarse tuning is activated to increase the amount of charge into the loop filter to reduce the lock time of the DLL. The coarse charge pump and the fine charge pump are used during coarse tuning. When the DLL is close to lock, fine-tuning is activated. Only the fine charge pump is used during fine tuning to obtain a low-jitter output signal. The lock control circuit will stop the coarse charge pump from operating during fine tuning. The range of phase error when the coarse charge pump is turned off can be controlled by adjusting the delay output from the lock control circuit.

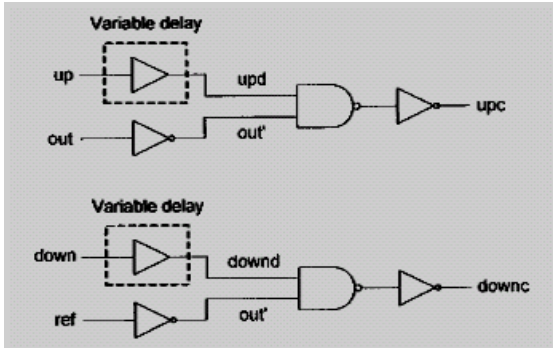
The disclosed method includes a lock control circuit to control the switching between coarse tuning and fine tuning. The circuit is connected to the coarse charge pump to control the output of the PFD to the charge pump and the current from the charge pump into the loop filter. The lock control circuit is comprised of a delay array connected to four inverters and two NAND gates (Figure 2).

Two lock control circuits are required for the coarse charge pump, one for the UP signal and the other for the DOWN signal. The delay array determines when the coarse charge pump deactivates for the DLL to perform fine locking. A fixed delay is illustrated for the sake of simplicity. When the switching point between the coarse tuning and fine tuning requires adjustment, a current-starved inverter can be used to obtain a variable delay.

The input to the lock control circuit is UP and OUT, producing the UPC signal. The input to the lock control circuit is DOWN and REF, producing the DOWNC signal. The buffer immediately after the UP and DOWN signal functions as a variable delay that is used to adjust the amount of pulse width that is sent to the coarse charge pump. The larger the delay on the UP or DOWN signal, the longer the pulse width of the UPC or DOWNC signals. The lock control circuit without any delay at the UP or DOWN input signals outputs zero pulse if the phase error from the PFD is less than *R*. The delay in the variable delay can range from 0 to π. The larger the delay, the faster the DLL is able to lock (Figure 3).

Following Output waveform of the lock control circuit when (a) the phase error is less than π (b) when the phase error is more than π. The delay of the variable delay in the loop control circuit is π. The arrows show the direction of the signal when it is delayed.

Fig.:2 Clock Control Circuit



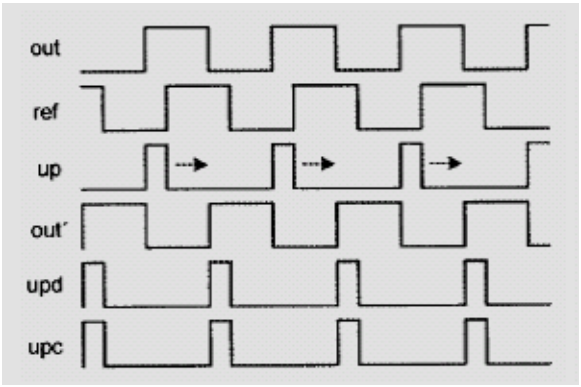


Fig.: 3(a). Waveform

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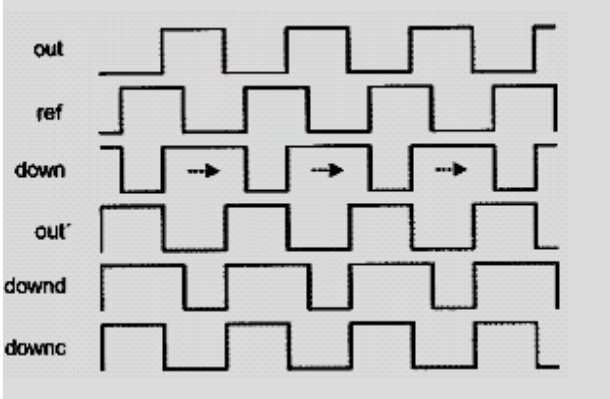

Fig.: 3(b). Waveform

However, the delays must be designed with a consideration for the amount of current output from the coarse charge pump. The control signal might overshoot if the system is designed with a large delay and high coarse charge pump output current (Figure 4).

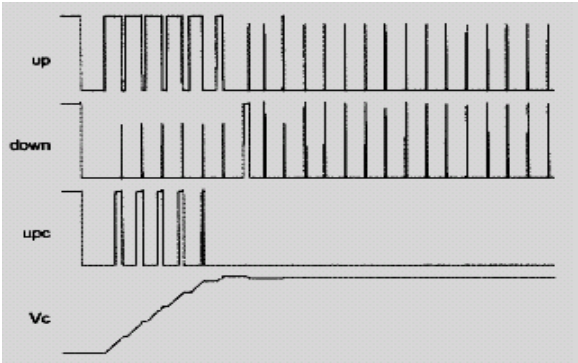

Fig.: 4 Charge Pump Output Current

The following logic can be used to ensure overshooting does not occur:

When $\theta_e = T_{shot}$ and Td = 0, $I_{fn,\ max}$
Then $T_{vcdl} \sim= T_{shot}$
When $\theta_e = T_{shot}$ and Td = n, $I_{fn,\ max} + I_{cp,\ max}$
Then $T_{vcdl} \sim= T_{shot}$

The value θ_e is the phase difference. T_d is the delay of the variable delay. $I_{cp,\ max}$ and $I_{fn,\ max}$ are the maximum output current of the coarse charge pump and fine charge pump. T_{shot} is the pulse width of the one-shot pulse. T_{vcdl} is the delay produced by the VCDL.

V. CONCLUSION

In the paper describe different types of method then made by the Dual Charge Pump and Lock Control Circuit then The Author will have made Fast-Lock Low-Jitter Delay-Locked Loop.

REFERENCES

[1]. B.W. Garlepp et al.; "A Portable Digital DLL for High- Speed CMOS Interface Circuits," JSSC, 34(5):632-644, May 1999.
[2]. T. Olsson et al.; "A Digitally Controlled Low-Power Clock Multiplier for Globally Asynchronous Locally Synchronous Designs," ISCAS, Geneva, May 2000.
[3]. I.C. Hwang et al.;"A digitally Controlled Phase-Locked Loop with a Digital Phase-Frequency Detector for Fast Acquisition," JSSC, 36(10):1574-1581, Oct. 2001.
[4]. T. Matano et al.; "A 1-Gb/s/pin 512-Mb DDRII SDRAM Using a Digital DLL and a Slew-Rate-Controlled Output Buffer," JSSC, 38(5):762-768, May 2003.
[5]. M. Combes et al.; "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells," JSSC 31(7): 958-965, July 1996.
[6]. Efendovich et al.; "Multi-frequency zero-jitter delay locked loop," JSSC 29(1):67-70, Jan 1994.
[7]. B.S. Kim et al.; "100MHz all-digital delay-locked loop for low power applications," Electronic letters 34(18):1739- 1740, 3 Sep. 1998.
[8]. J. Christiansen; "An Integrated CMOS 0.15nS Digital Timing Generator for TDC's and Clock Distribution Systems,." IEEE Trans. Nuclear Science, 42(4): 753–757, Aug. 1995.