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Low power wallace and dadda multiplier based on CLRCL full adder

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Abstract: Multiplication is one of the most critical arithmetic operation, which is extensively used in many VLSI systems such as application specific based digital signal processor architectures and microprocessor. Multipliers are the major source of power dissipation in the VLSI systems. By reducing the power consumption of the multipliers the power consumption of the VLSI system can be reduced. This paper presents the CLRCL full adder based 4*4 Wallace and Dadda multipliers. The CLRCL full adder has only ten transistors which is less in number when compared with conventional full adders which is used to design these multipliers. Designing Wallace and Dadda multiplier by using CLRCL full adder will reduce the transistor count and power consumption. The proposed design is simulated using 0.12µm.

Keywords: Full adder, multiplier, Power consumption, Wallace multiplier, Dadda multiplier

I. INTRODUCTION

The multipliers play a major role in digital signal processing applications and microprocessors. Currently the need for low power multiplier has been increased due to immense increase in portable devices. However, with the advance of VLSI technology, the computation speed can be improved at a constant pace. Instead, power consumption has been a more and more prominent design factor under the prevailing of battery operated mobile devices. Power consumption if a VLSI system increased when the chip density is increased [1].So the major consideration while designing multipliers is power consumption.

C.S.Wallace suggested a fast multiplier during 1964 with combination of half adders and full adders[2] Later the Wallace multiplier with full adder design showed rapid development in power consumption [3]. Luigi Dadda suggested a parallel multiplier during 1965 with half adder and full adder. Then Dadda multiplier with full adder showed rapid development in power consumption[4].For both the multipliers full adder is the basic unit .So the power consumption of the full adder will have an impact on these multipliers. Here Complementary and Level Restoring Carry Logic adder(CLRCL) full adder is used to design 4*4 Wallace and Dadda multiplier to its less transistor count and low power consumption [5].The simulation results shows rapid development in power consumption of 4*4 Wallace and Dadda multipliers when compared with conventional full adders like 28T,16T,14T based Wallace and Dadda multipliers.

II. EXISTING WORK

An Dadda and Wallace multiplier are efficient hardware implementation of digital circuit that multiplies two integers. Initially a 4*4 Wallace and Dadda multipliers were designed using conventional full adder .This full adder had 28 transistors [6]. The schematic diagram of 28T full adder is shown in Fig. 1.

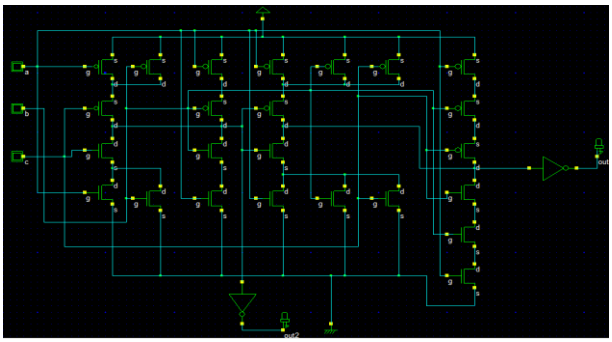

Fig. 1Schematic diagram of 28T Full Adder

Then 4*4 Wallace and Dadda multiplier are designed by using 28T full adder[7] as shown in Fig. 2and Fig. 3.The Wallace multiplier design has 280 transistors and the 4*4 Dadda multiplier has 336 transistors.

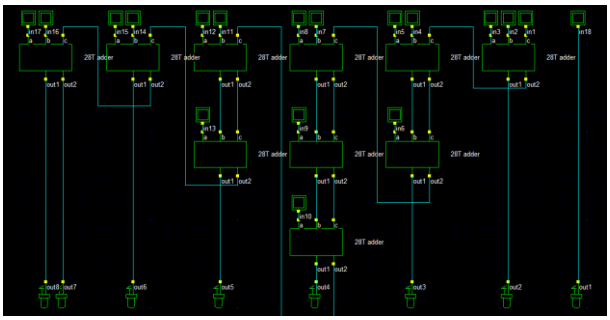

Fig. 2Schematic diagram 28T Full Adder based4*4Wallace Tree Multiplier

Later a 16T full adder is proposed. This full adder has 16 transistors [8] which is less in number when compared with 28T full adder as shown in Fig. 4.

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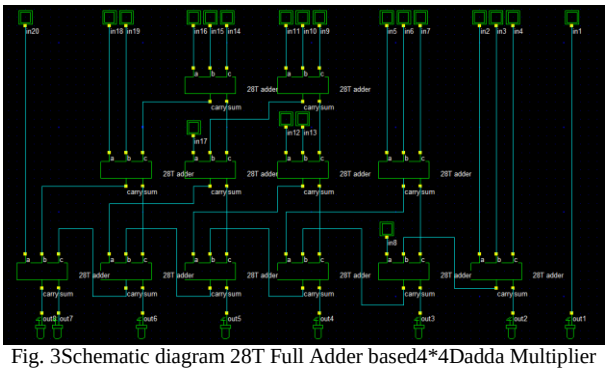

Fig. 3Schematic diagram 28T Full Adder based4*4Dadda Multiplier

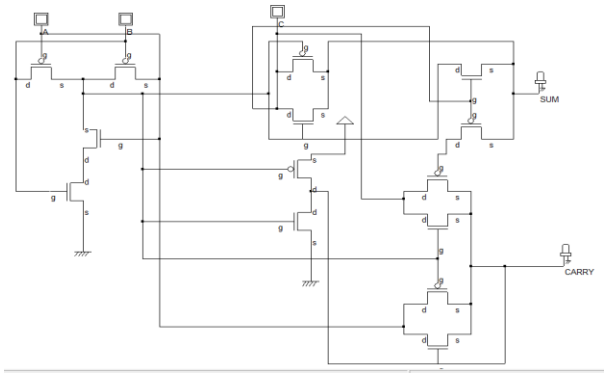

Fig. 4 Schematic diagram 16T Full Adder

Then 4*4 Wallace and Dadda multiplier were design using 16T full adder[7].From these design the transistor count of Wallace Tree multiplier is 160 and Dadda multiplier is 192 as shown in Fig.5 and Fig. 6.

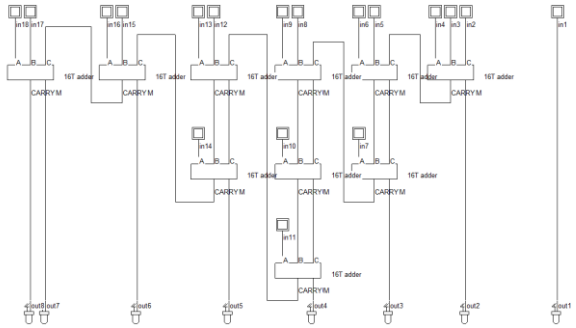

Fig. 5 Schematic diagram 16T Full Adder based 4*4 Wallace Tree Multiplier

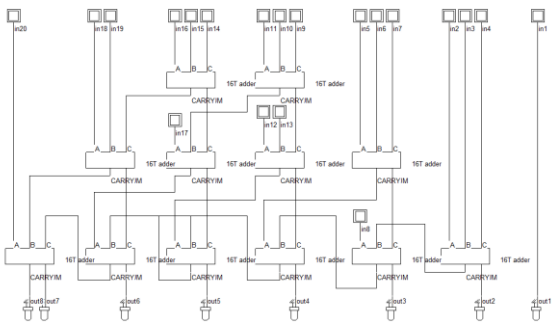

Fig. 6Schematic diagram 16T Full Adder based 4*4 Dadda Multiplier

Many researches had been done in terms of transistor count to reduce the power consumption of multipliers.Then a 14T full adder is proposed which has only 14 transistors [9] as shown in Fig. 7.

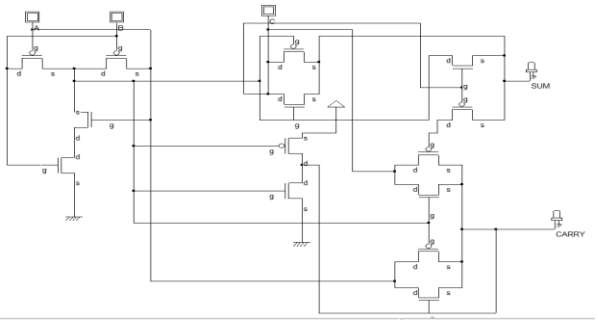

Fig. 7Schematic diagram 14T Full Adder

A 4*4 Wallace Tree multiplier and Dadda multiplier were designed using 14T full adder[7] as shown in Fig. 8 and Fig. 9

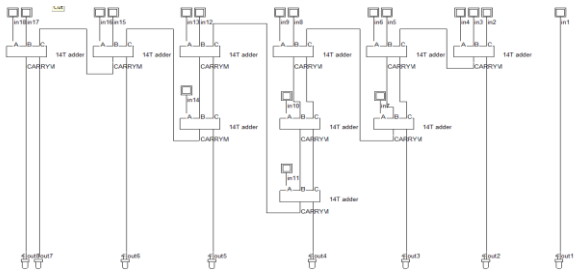

Fig. 8 Schematic diagram 14T Full Adder based 4*4 Wallace Tree Multiplier

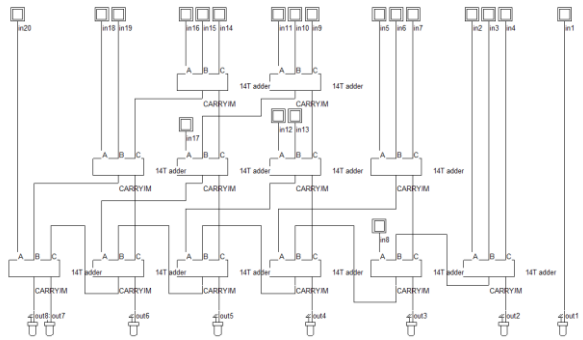

Fig. 9 Schematic diagram 14T Full Adder based 4*4 Dadda Multiplier

From the 14T full adder based Wallace and Dadda multipliers has 140 and 168 transistors respectively which is less in number when compared with 28T,16T full adder multipliers.

III.PROPOSED WORK

The proposed work presents the design of low power 4*4 Wallace and Dadda multipliers based on CLRCL full adder. Though different multipliers exists [10] here Wallace and Dadda multipliers is chosen due to its high performance and speed.CLRCL full adder has less number of transistors and power consumption when compared with existing adders [5] as shown in Fig.10.

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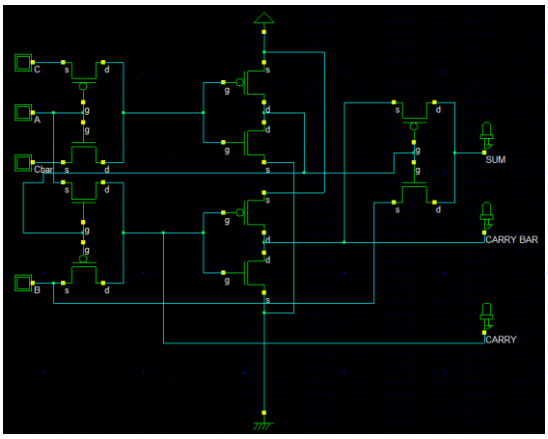

Fig. 10 Schematic diagram of CLRCL Full Adder

This full adderhas two major advantages when compared with existing adders.First one is it act as level restoring circuit to contest the output threshold voltage loss. Second one is the inverter in this design serves as a buffer along the carry chain to speed up the carry propagation. The ultimate intention of this full adder is that the carry signal must not suffer from distortion as it is propagated. Here a 4*4 Wallace multiplier is designed with the help of CLRCL full adder as shown in Fig. 11

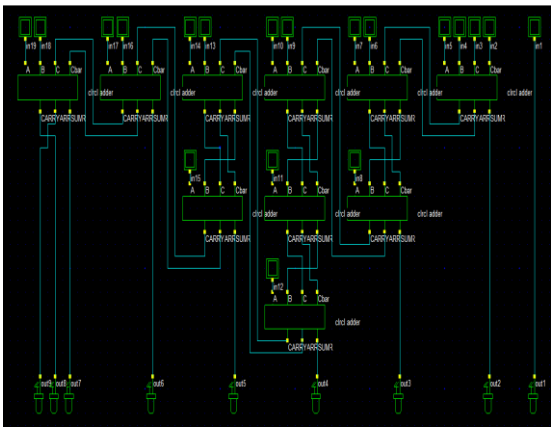

Fig. 11 Schematic diagram CLRCL Full Adder based 4*4 Wallace Multiplier.

The proposed design has 10 CLRCL blocks with 100 transistors and power consumption of 0.591µW.A 4*4 Dadda multipliers is designed using CLRCL full adder as shown in Fig.12.This design has 210 transistors and 0.437µW power consumption.

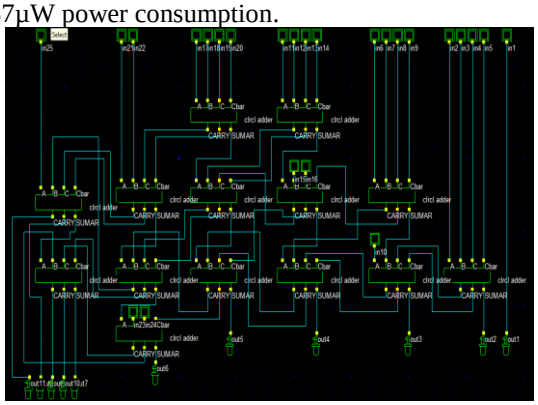

Fig. 12Schematic diagram CLRCL Full Adder based 4*4 Dadda Multiplier

IV. RESULTS AND COMPARISON

A. Results

The proposed 4*4 Wallace multiplier and Dadda multipliers are simulated using 0.12µm technology in microwind 2 tool. From the simulation results the Wallace and Dadda multiplier consumes less power when compared with conventional full adders based Wallace and Dadda multiplier. The simulated waveforms of these multipliers are shown in Fig. 13 and Fig. 14.Digital signal processing applications become more efficient by using these multipliers.

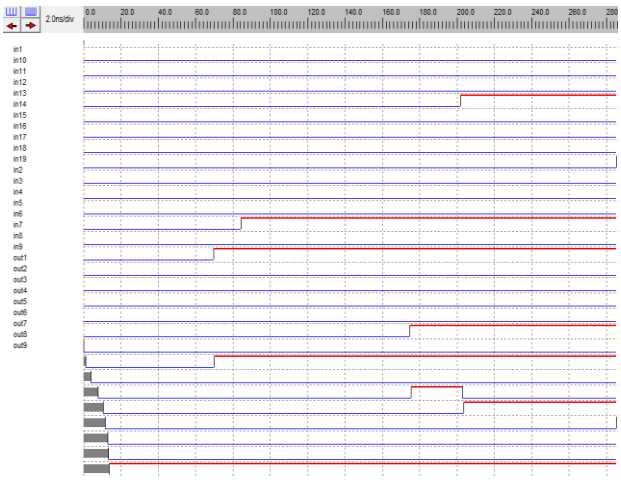

Fig. 13Waveform of CLRCL Full Adder based 4*4 Wallace multiplier.

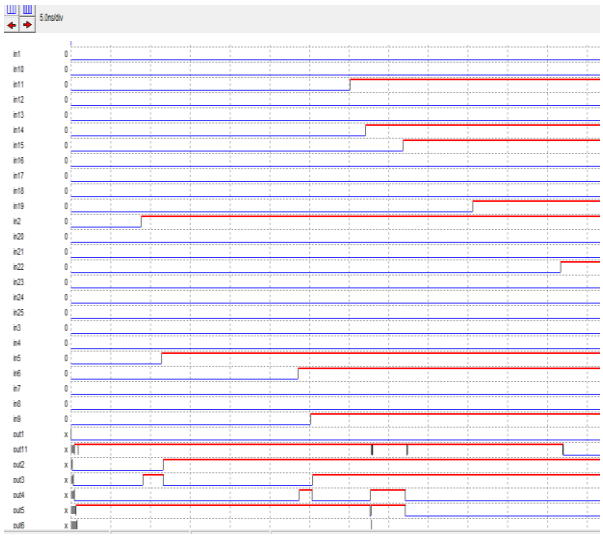

Fig. 14 Waveform of CLRCL Full Adder based 4*4 Dadda Multiplier.

B. Comparison

A comparative analysis is made between CLRCL based Wallace multiplier and conventional adder based Wallace tree multiplier is shown in Table 1.And Table 2 shows the comparative analysis between CLRCL based Dadda multiplier and Conventional adder based Multiplier.Table 1 and Table 2 shows that CLRCL based Wallace and Dadda multipliers were better in terms of transistorcount and power consumption when compared with 28T, 16T and 14T fulladder based multipliers.

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TABLE I
COMPARATIVE ANALYSIS OF WALLACE MULTIPLIER

Wallace multiplier	Transistor count	Power consumption
28T based	280	8.58w
14T based	140	8.60w
16T based	160	8.50w
CLRCL based	100	0.591µw

TABLE II
COMPARATIVE ANALYSIS OF DADDA MULTIPLIER

Dadda multiplier	Transistor count	Power consumption
28T based	336	1.378uW
14T based	168	1.091uW
16T based	192	0.891uW
CLRCL based	120	0.827uW

V. CONCLUSION

In this paper, the power consumption and transistor count of 4*4 Wallace tree multiplier and Dadda multiplier were realized using CLRCL full adder. For comparative analysis these multipliers were realized with 28T, 16T and14T full adders. In all the Wallace and Dadda multiplier configuration investigated, the CLRCL full adder based Wallace and Dadda multiplier exhibited better result interms of transistor count and power consumption. These multipliers based on CLRCL full adders are worth enough to make the performance of digital signal processor more efficient.

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