ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 2, February 2014

IWSN FOR PATHRECONFIGURATION BASED TRANSCEIVER USING RTOS & MULTIPROCESSOR

P.Rubini[1], C.Subashini[2], J.Sathyapriya[3], T.Bharathi[4]

PG Scholar, Embeded System Technologies, S.A. Engineering College, Chennai, India[1]

Ph.D Scholar, Dr.M.G.R Educational & Research Institute University Chennai, India[2]

PG Scholar, Embeded System Technologies, S.A. Engineering College, Chennai[3,4]

Abstract: An Industrial area wireless sensor network plays major role for communication between Reservoir plant and operator room. These communication should always reliable using wireless sensor network. The IWSN techniques offers safety & security, path reconfiguration, support shortest path communication and allows only reliable communication. This work demonstrates an RTOS based architecture by transmitting messages from reservoir plant to operator room using Round Robin Scheduling and serial communication techniques to concentrates over two paths. The support of multiprocessor such as application processor and RF processor having functions of Inputs, Outputs and Data transcribing using IPC for integration between two layers. Here UART command perform IPC functions and mainly concentrates over path reconfiguration techniques. Wi-Fi based zig bee board provides built in Rf modules has been supports capability of UART communication that makes system more simplest, efficient memory and consume less energy.

Index Terms: IWSN, UART, Round Robin Scheduling, RF& ARM COTEX M4 PROCESSOR.

I. INTRODUCTION

The wireless sensor network communication protocols have been increased and perform for advance work. This work provides various techniques such as wireless link reliability, real-time capabilities, or quality-of-service. These new works are considered and suitable for future applications in industries and related wireless sense and control applications, partially replacing or enhancing conventional wire-based networks by WSN techniques and medical, defense purpose .This is suitable for embedded real time system's . In wireless sensor networks contains several nodes which is in grouping of sensor nodes that is commonly collects data from a gate node

The WSN consists of infinity of nodes to built the network each and every nodes are integrated with number of sensors. These sensors are interlinked with Radio Frequency transmitting and receiving information. The radio transceiver consists of two antenna which is presented internally and externally. UART used to configure RF module which is more simple and memory efficient. CDMA provide high power design replaces TDMA also provide single frequency used for multiple call and also for inherent frequency diversity, and universal frequency reuse .In this case use CDMA for inherent frequency diversity, and universal frequency reuse comparing to TDMA.RTOS architecture consist of two processors are application and RF processors using IPC communicate with two processors, IPC is realized high speed UART interfaces which are available in both chip. The rapidly increasing complexity and other specific requirements of industrial have made it necessary to adopt RTOS in IWSN stacks. The objective of this work is concentrated for reliable communication between man to machine communication using UART and type of RTOS scheduling. The multiprocessors consists of two layers such as memory abstraction layer and hardware abstraction layer. The adoption of RTOS and support of multiprocessor deserved to challenging the guarantee for timing integrity. The low cost commercial chips combined with high performance industrial processor such as low-high combination.

The normalized inter layer interface(NILI) performs operations for stack construction and inter layer interaction. These interaction deals for classified message formats such as (a) The specification of messages are packet payload, packet type, priority, timeout, etc. used to send or receive a packet. (b) The protocol stack was constructed for setting timing integration between upper layer pointer and lower layer pointer in each layer of the processor. The RTOS caused some timing integration overhead to the inter layer interaction and inter layer processing. Then to overhead as minimized by RTOS, by this causes high quality optimization must for timing critical layers.

II. RELATED WORKS

The work for wireless sensor and actuator networks target about industrial automation has been proceeded typical process automation and WSN applied in automation industry .According to this work assured about safety, security and availability before industrial wireless sensor networks will be adopted for full scale in process automation (1). The work for Hardware challenges and their resolution in advancing Wireless HART has been

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 2, February 2014

proved requirements and solutions for industrial wireless mesh networks are more challenging and complicate than other mesh networks (2).

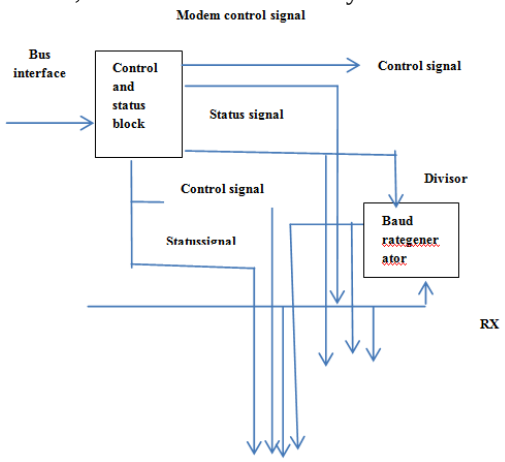
The low cost , low power and high performance micro control unit core used for wireless body sensor networks provide an asynchronous interface, error correction, avoid data loss , UART support for power management and multiple sensor support (3).

III. SYSTEM DESCRIPTION

The work is propose to provide security authorization, long distance communication, increase number of messages due to communication , interrupt handler, FIFO scheduling using RTOS type scheduling .The round-robin (RR) scheduling algorithm is designed especially for sharing time .The FCFS scheduling also do the same, but pre-emption is added to switch two processes .To implement RR scheduling, the ready queue as a FIFO queue of processes. The CPU scheduler picks the first process from the ready queue, sets a timer to interrupt after each time quantum, and results the process.

The serial communication protocol such as UART provides multiple communication commonly referred to as RS232 or RS485. This is to be configured for full duplex, half duplex, RX only, TX only. A Wireless HART as no configuration to support additional path with secured communication. So, by using UART to tackle problem in HART communications .Two paths as to be configured if path A failed using autonomous sensor to automatically pass data's to path B transmitted in to receiver of virtual terminal . RTOS architecture as two processors are application and RF processors using IPC communicate with two processors, IPC is realized high speed UART interfaces which are available in both chip. The rapidly increasing complexity and other specific requirements of industrial have made it necessary to adopt RTOS in IWSN stacks .

The choice of 1.8v, 2.5v,3.3v or 5v supply . The availability of single , dual, quad channel devices causes transmission and reception FIFO of either 16 bit or 64 byte depth. The features of UART stack are point of scale terminals, gaming terminals, cellular data , portable applications , Router control & factory automation.



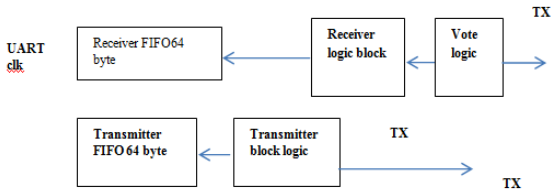


Fig 1.An UART stack used in WSN

The module shows how message signals passed from number of sensors to virtual terminal via a multiprocessor module . It consists of two processor Application processor that is ARM CORTEX M4 processor used for provides input output pins an Radio signal processor such as Embers 250 RF processor provides transmitter , receiver and ground pins these data's are in TTL logic which should be converted to CMOS logic by the device called silicon controlled rectifier. The power signal produces high affects module completely so to reduce power step down transformer was mounted on the module. The timer is useful for scheduling time management for each task. The serial communication protocol such as UART used to transmitting messages to Virtual terminal.

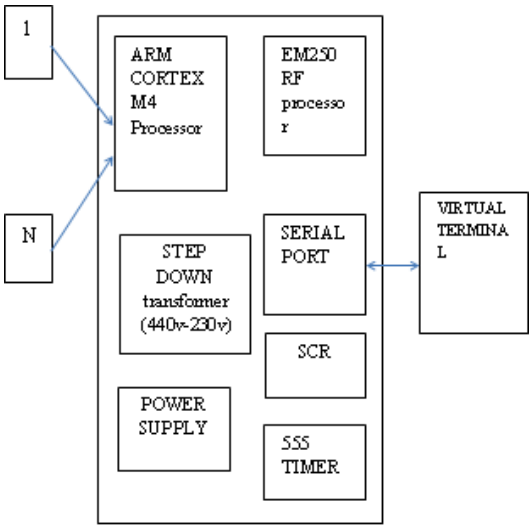


Fig 2.Block Diagram for system module

A. RTOS USES TO SCHEDULING MORE TASK:

The RTOS useful more scheduling more task using two process such Preemptive and non-premptive RTOS task shows in Fig.3 & 4.

This block shows multiple task as to run without preemption so continuously process the task with out any order so it exceeds deadline task not get completed originally . The RTOS scheduler used to produce ISR to setting this much of time to recover from the block . The recovered output is not much reliable and reconfiguration so to overhead that use preemptive RTOS scheduler.

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 2, February 2014

Table 1: Task scheduling

TIME	PROCESS CONTEXT	SAVED CONTEXT	TASK P1	TASK P2	TASK P3	TASK P4	TASK P5
0-4MS	P1		Running	Started	Started	Started	Started
4-8MS	P2		Finished	Running	Started	Started	Started
8-12MS	P3	P2	Running	Blocked after saved	Running	Started	Started
12-16MS	P4	P2,P3	Finished	Blocked after saved	Blocked after saved	Started	Started
16-20MS	P5	P2,P3,P4	Finished	Blocked after saved	Blocked after saved	Blocked after saved	Started

The task are scheduled with respect to time each in 4MS difference clearly shown in Table 1. The context shows progress of the task processed and after completion task as to be saved.

The Preemptive task scheduler such as RR scheduler use to overhead deadline missed condition to complete task with in deadline. RR scheduler performs number of task with time scheduling in ms.

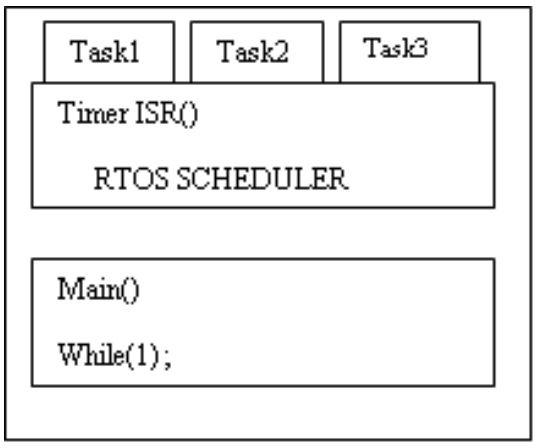


Fig 3.NON-PREMPTIVE RTOS

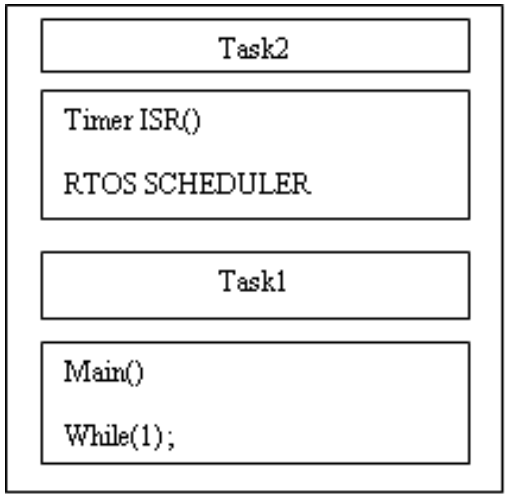


Fig 4.PREEMPTIVE RTOS

Round-robin (RR) is one of the algorithms employed by process and network schedulers in computing. As the term is generally used, time slices are assigned to each process in equal portions and in circular order, handling all processes without priority and also known as cyclic executive. In a centralized wireless packet radio network, where many stations share one frequency channel, a scheduling algorithm in a central base station may reserve time slots for the mobile stations in a round-robin fashion and provide fairness.

IV SIMULATION RESULT

The simulation results shows in Proteus software. By using ISIS work bench have all the devices such ground, microcontroller, microprocessor, CPU, virtual terminal, variable resistor etc these already there pick required devices

Proteus is software for microprocessor simulation, schematic capture, and printed circuit board (PCB) design. It is developed by Lab center Electronics

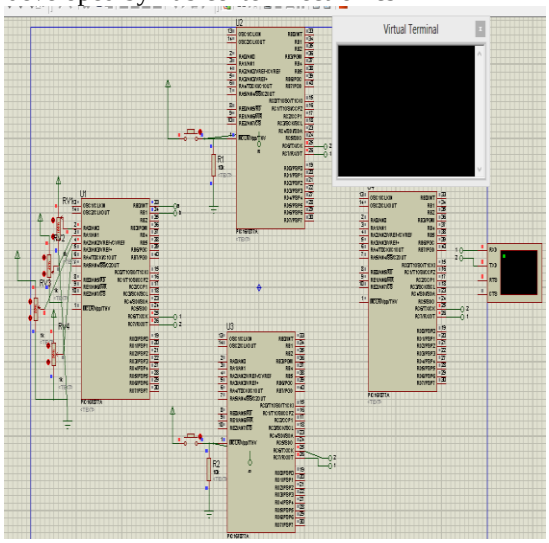


Fig 5. Snapshot for block message

The message is transmitted through number of sensor which is received by two paths for reliable reconfigurable process.

ISSN (Online) : 2278-1021
ISSN (Print) : 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 3, Issue 2, February 2014

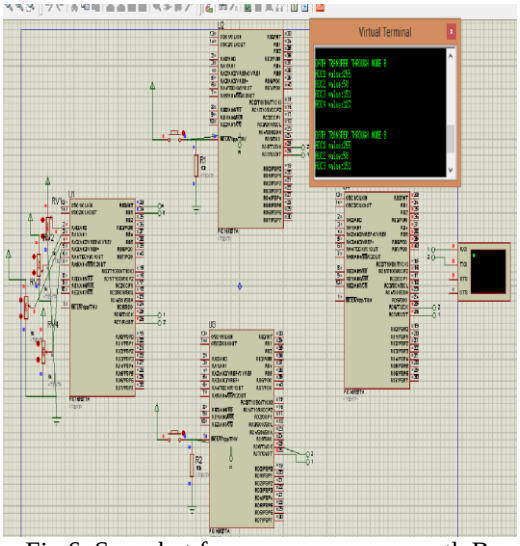


Fig 6. Snapshot for message pass on path B

The above figure shows messages passed via path B another path as to be terminated.

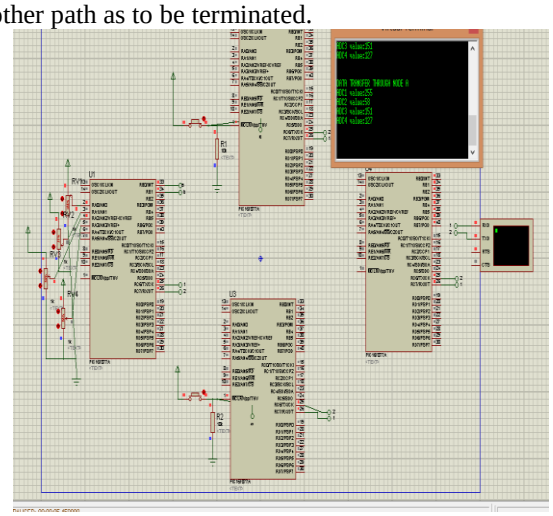


Fig 7.Snapshot for message pass on path A

This figure shows messages passed via path A another path as to be terminated or else in ON condition.

V. CONCLUSION

In this proposed system an RTOS-based architecture with multiprocessor support for IWSN protocol stacks. The advantages have been proven by a case study of UART stack that has been implemented on a low cost two processor platform. Reconfigure the problem such as timing integrity, the extra traffic caused by the inter layer interaction. A huge amount of messages are transmitted between layers in addition to the effective packets, to improve the standards to be more "RTOS and multi-processor friendly" is a feasible strategy. But the CDMA produces high power design that is sufficiently utilized by RTOS and multiprocessor support. The path required for communication will increase in future scope to protect the message maintain by any routing table. Number of nodes increased reconfiguration of blocked or else kept by unauthorized person due to messages and applicable for more application such as FPGA kit checker, home automation, medical communication. etc..

REFERENCES

[1] Akerberg, J.; Gidlund, M.; Bjorkman, M.Future research challenges in wireless sensor and actuator networks targeting industrial automation IEEE Int. Con. on Industrial Informatics (INDIN), 2011,410-415

[2] Xiuming Zhu; Song Han; Mok ,A.; Deji Chen; Nixon, M.. Hardwares Challenges and their resolution in advancing wireless HART . IEEE Int. Con. on Industrial Informatics (INDIN) ,2011,416-421

[3] Edmonds , N.; Stark,D.; Davis, J. "MASS: modular architecture for sensor systems". Int. Sym . Information processing in sensor Networks (IPSN), 2005.393-397

[4] Chiung – An Chen 1, Shih-Lun Chen 2,Hong –Yi Huang 3 and Ching-Hsing Luo An Efficient Micro Control Unit with a Reconfigurable filter Design for Wireless Body Sensor Networks (WBSNs) 22 November 2012

[5] I Turbe, X. ; Benkrid, K. ; Chuan Hong ; Ebrahim, A. , A Novel Reliable Reconfigurable Real-Time Operating System for Highly Adaptive, Efficient, and Dependable Computing on FPGAs , 2013

[6] Utz Roedig, Sarah Rutlidge, James Brown, Andrew Scott, "Towards Multiprocessor sensor nodes"ACM workshop on Topics in Embedded Network sensors2010

[7] ISA100 standard, International Society of Automation. www.isa.org/isa100

[8] Wireless HART standard, HART Communication Foundation. www.hartcomm.org

[9] WIA-PA standard, Chinese Industrial Wireless Alliance.www.industrialwireless.cn/en