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Implementation of On-Chip Network Protocol AMBA AHB

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Abstract: In this paper, the efficient bus architecture AMBA AHB is defined to support most advanced bus functionalities was designed and the hardware modelling for that architecture was done using VERILOG (IEEE STD 2001) and simulated in Modelsim. The scheme involves read and write transactions, lock transactions, pipelined transactions of the standard. AMBA (Advanced Microcontroller Bus Architecture) was introduced by ARM in 1996 as registered trademark and is an open-standard communication protocol, as more IP cores are integrated into an SOC design, the communication flow between IP cores has increased drastically and the efficiency of the on-chip bus has become a dominant factor for the performance of a system. The AHB design implementation is done with one master and four slaves, according to decoding scheme master can access the bus slaves based on generated address range. One entity acts as the master of the AHB instance, and the other IP's acts as the slaves of AHB instance and only the master can present commands and is the controlling entity. The slave responds to commands presented to it, either by accepting data from the master, or by presenting data to the master. Upgradeability and Customization benefits of programmable logic can be obtained by FPGA implementation.

Keywords: AMBA-AHB, Master and Slave protocols, System-on-chip (soc), FPGA, Intellectual property.

I. INTRODUCTION

The ARM Advanced Microcontroller Bus Architecture (AMBA) is an on-chip inter connects open-standard specification for the management and connection of functional blocks in system-on-a-chip (SoC) designs. The AMBA AHB specification [4] also defines an on-chip communications standard for designing the high-performance embedded microcontrollers. It is supported by ARM Limited [1] [5] with wide cross-industry participation. It is designed to be used with a central multiplexor or interconnection scheme. It also facilitates development of multi-processor designs with large number of peripherals and controllers.

Using this scheme bus master drive out the address and control signals indicating the transfer they wish to perform .A central decoder is also required to control the read data and response signal multiplexor, which selects the appropriate signals from the slave that is involved in the transfer.

Figure 1 shows the designed structure required to implement an AMBA AHB [2] design with one master and four slaves.

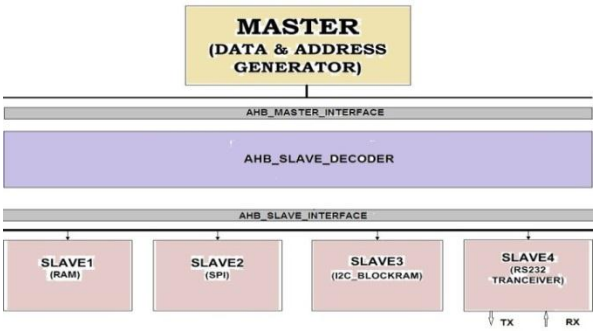

Fig 1: Block diagram of Implemented Design

A. *Basic Transfer*

- The address phase, this lasts only for a single cycle.
- The data phase, is the one which may require several cycles. This is achieved using the HREADY signal.

In a simple data transfer with no wait states:

- The master drives the address and the control signals onto the bus after the rising edge of HCLK.
- The slave then samples the address and control information on the next rising edge of the clock HCLK.
- After the slave has sampled the address and control it can start to drive the appropriate response. The address phase of any transfer occurs during the data phase of the previous transfer. This overlapping of address and data is fundamental to the pipelined nature of the bus and allows for high performance operation, while still providing adequate time for a slave to provide the response to a transfer.

B. *Address Decoding*

HSELx for each slave on the bus is provided by the central address decoding scheme. The select signal is a combinatorial decode of the high-order address signals.Simple address decoding schemes are encouraged in protocol to avoid complex decode logic and to ensure high speed operation. A slave must only sample the address and control signals and HSELx when HREADY is HIGH, indicating that the current transfer is going to complete. Under certain circumstances it is possible that HSELx will be asserted when HREADY is LOW, the selected slave hasto change by the time the current transfer completes. If a NONSEQUENTIAL or SEQUENTIAL transfer is attempted to a nonexistent address location then the default slave should provide an ERROR response.

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IDLE or BUSY transfers to nonexistent locations should result in a zero wait state OKAY response. Typically the default slave functionality will be implemented as part of the central address decoder.

II. AMBA AHB MASTER

An Bus master initiates read and write operations by providing address and control information. Only one bus master is allowed to use the bus actively at any given time. Hence, before initiating any transfer, it sends a request to the arbiter for accessing the bus. Once the master is granted the access (to the bus), the master initiates read/write operation. Master 0 is the default master and is selected whenever there are no requests for the bus.

Here, we have designed a data and address generator which eventually produces data and address based up on system clock

In this section the simulation results for AHB Master Interface [3] are presented, we first introduce the signals, then the Specification and finally the simulation results.

A. AHB Master Signals

The signals for AHB Master Interface [4] is

1. HWRITE – This is the signal from the bus master indicates the nature of transfer. When HWRITE is low, it indicates read transfer. If high, it **indicates** write transfer.

2. HADDR[31:0] -- These signals from the master provide information about address location where write or read transfer shall take place.

3. HWDATA[31:0] - These signals from the master provides information about data to be written in case of write transaction.

4. HRDATA[31:0] - These signals from the bus slave to the bus master provide information about data read in case of read transaction.

5. HSIZE[2:0] - This is the signal from the bus master to the bus slave provides information about the bus width. It can be a definite value that corresponds to one of byte (8-bit), half word (16-bit) and word (32-bit) up to 1024 bits. In this work, data bus width is fixed to 32-bit.

6. HRESP [1:0] - This signal from the bus slave to the bus master provides transfer response.

These are some of the auxiliary signals for AHB Master They are as follows:

REQ_VLD - This signal is input to the bus master. It is used by the bus master for deciding HBUSREQ. HBUSREQ signal is asserted whenever REQ_VLD is asserted.

WR - This signal is input to the bus master. It indicates that write transaction shall take place. HWRITE shall be set HIGH if WR is high.

RD - This signal is input to the bus master. If high, it indicates that read transaction shall take place and hence HWRITE shall be set LOW.

IN_ADDR [31:0] - These signals are input to the master providing information about address. These signals are used to decide HADDR.

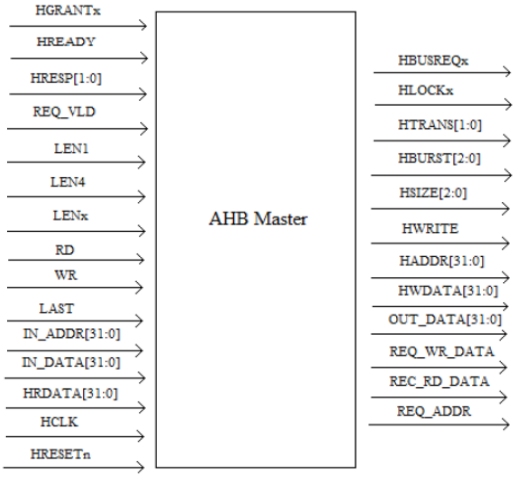

Fig 2: Signals of AHB Master Interface

B. Specifications

In the specification of AMBA AHB Master, we have some assumptions and guarantees. The guarantees and assumptions are as follows.

Note: All the assumptions and guarantees are again directly obtained from the AMBA AHB standard.

Guarantees

The guarantees are as follows.

- Data bus is 32-bit wide. That is HSIZE shall be fixed to WORD throughout.

- Bus master requests only for locked transfer.

- If the ongoing transfer is last transfer of an AHB sequence, then HLOCK shall be lowered.

- First transfer of an AHB sequence is always NONSEQ in nature. All following transfers in sequence shall be SEQ in nature.

- Nature of transfer shall be set according to WR and RD signals.

-If HREADY is low, then all control signals shall hold their values.

-When HREADY and HGRANT are simultaneously high, REQ_ADDR signal shall be high. It ensures that in next cycle, master can put address on address bus.

- When both REQ_ADDR and WR signals are high, REQ_WR_DATA signal shall also be high. It ensures that data shall be put on data bus one cycle after address is put on address bus.

-When a read transfer is taking place and HREADY is high, REC_RD_DATA signal shall also be high.

-When REQ_ADDR is high, the input signals IN_ADDR will be copied to address bus in the next cycle.

-When REQ_WR_DATA is high, the input signals IN_DATA will be copied to data bus in the next cycle.

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-When transaction read is in progress and HREADY is high, OUT_DATA will copy the value of HR_DATA in the next cycle.

2.2.2 Assumptions.
The assumptions are as follows:
- Length of transfer will be specified with REQ_VLD signal i.e., whenever REQ_VLD is high, one of LEN1, LEN4 and LENX signal shall be high.
- Nature of transfer will be specified with REQ_VLD signal i.e., whenever REQ VLD signal is high, at least one of RD or WR signal shall be high.
- If REQ_VLD signal is low, then RD, WR shall hold their values.
- There cannot be conflict between signals indicating nature of transfer, thus RD and WR signal cannot be high simultaneously.
- Input HRESP signal shall be OKAY throughout.

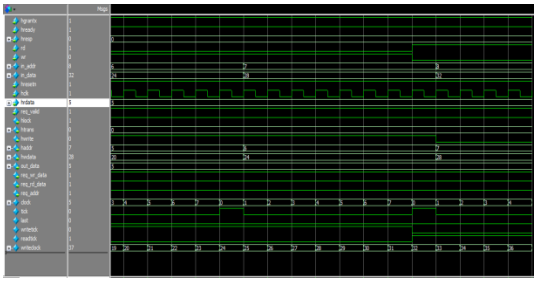

Fig 3: signals and simulation results for the AHB Master interface with address and data generator.

III. AMBA AHB SLAVE

A bus slave responds to transfers initiated by bus masters within the system. The slave uses a select signal HSELx from the decoder to determine when it should respond to a bus transfer. All other signals required for the transfer, such as the address and control information, are generated by the bus master. The bus slave signals back to the active master of the success, failure or waiting status of the data transfer.

Here we have considered ON Chip Ram, Rs232 Transceiver, I2C Block ram Slave controller, SPI controller as bus slaves.

NOTE: As the slaves considered in design are slower devices compared to interface, Clock Synchronization is the method used to synchronize clock frequency for efficient communication between interface and slaves.

In this section we present the synthesis results for AHB Slave. Let us see the AHB slave signal and auxiliary signals followed by the specifications.

An interface between a slave and a memory is introduced for implementing read and write transactions. We are considering memory with two status signals EMPTY and FULL. Two auxiliary signals have also been added named START and LAST. The START signal indicates start of an AHB transfer or sequence whereas LAST signal is used to indicate last transfer of an AHB sequence.

The signals used in this interface are shown in Figure 3. Figure 4 shows the timing diagram from AHB slave signals. The timing diagram shows the behaviour of auxiliary signals with respect to the input and the output signals. The signal used in interface between slave and memory is given below:

1. FULL - This signal is input to the bus slave indicating memory is full. When the memory is full, i.e.. FULL is high, no more data can be written into it without first being read.

2. EMPTY - This signal is input to the bus slave indicating memory is empty. When memory is empty, i.e., EMPTY is high, no more data can be read from it without rst being written.

3. ADDR[31:0] - These signals are output from the slave providing address information.

4. DI[31:0] - These signals are output from the slave and input to the memory providing information about data that should be written into memory.

5. DO[31:0] - These signals are output from the memory and input to the slave providing information about data that has been read from memory.

6. RD - This signal is input to the memory from the slave. It indicates that the read operation is being executed. 7. WR - This signal is input to the memory from the slave. It indicates that the write operation is being executed.

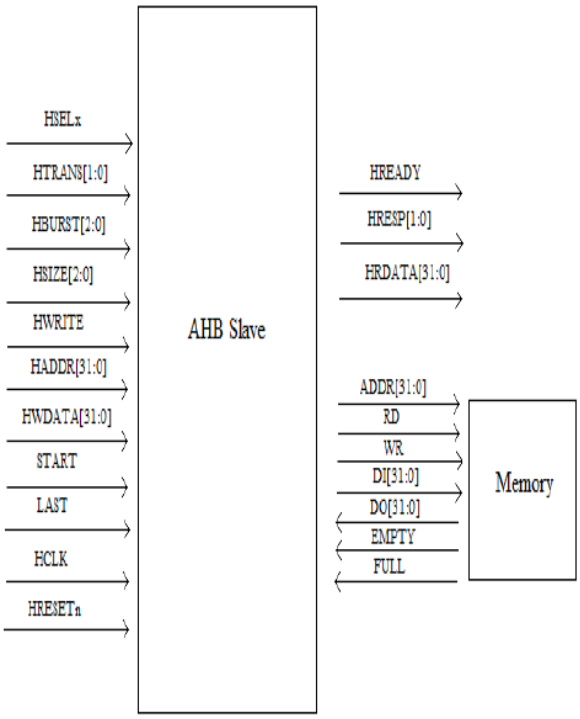

Fig 4: AHB slave Interface with ON CHIP as slave

A. specifications of AMBA AHB slave

In the specifications of AMBA AHB slave, we have the following guarantees and assumptions they are as follows

Guarantees.
NOTE :All the assumptions and guarantees are obtained directly from the AMBA AHB standard.

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The guarantees are as follows:

- When the slave is not selected by the decoder, HREADY signal shall be high.

-When the slave is not selected by the decoder, HRESP shall be OKAY.

-When no AHB transaction is taking place, HRESP shall be OKAY.

-RD and WR signal cannot be high simultaneously.

-If memory is full and write transfer is attempted, then the slave shall send an ERROR response. Similarly, if the memory is empty and a read transfer is attempted, then the slave shall send an ERROR response.

-When slave is involved in a transfer, HWRITE is used to decide values of WR and RD.

-When slave is involved in any transfer, signal HADDR is used to decide ADDR.

-When slave is involved in write transfer, signal HWDATA is used to decide DI.

-When slave is involved in read transfer, signal DO is used to decide HRDATA.

Assumptions.

The assumptions are as follows.

-When the slave is not selected by the decoder, all control signals shall be low.

-When HTRANS is IDLE, all control signals shall be low.

First transfer of any sequence is NONSEQ in nature.

-Non first transfer of an AHB sequence will always be SEQ in nature.

-If this is last transaction of a sequence and next cycle is not start of another sequence, HTRANS shall be IDLE in next cycle.

- If HREADY is low, then all control signals, address and data buses shall hold their values.

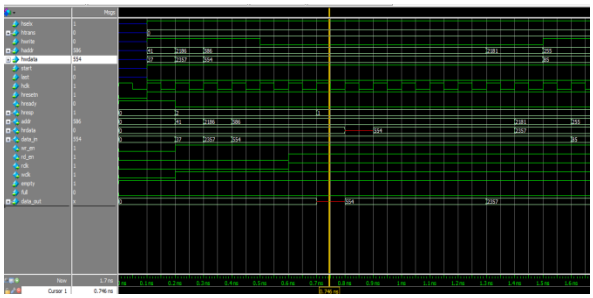

Fig 5: signals and simulation results for the AHB slave interface with On chip ram as slave.

In the same way interface between a slave and RS232 Transceiver, I2C Block Ram Slave Controller, SPI Controller are also introduced for implementing read and write transactions.

We are considering slaves with some status signals and auxiliary signals for prior communication.

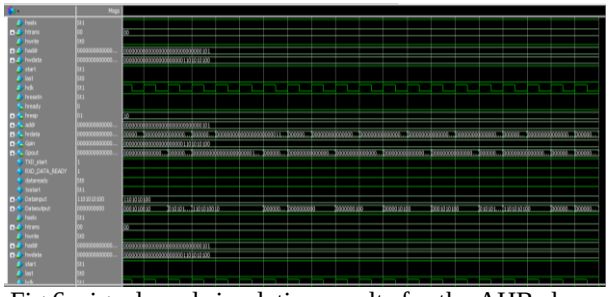

Fig 6: signals and simulation results for the AHB slave interface with RS 232 TXRX as slave.

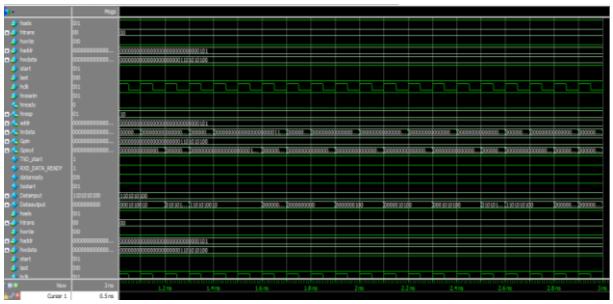

Fig 7: signals and simulation results for the AHB slave interface with SPI Controller as slave

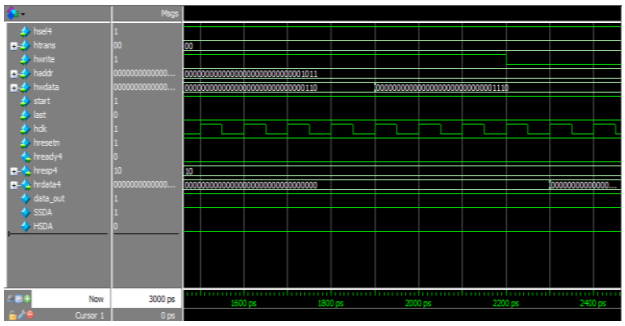

Fig 8: signals and simulation results for the AHB slave interface with I2C Block Ram Slave Controller as slave

IV. Implementation and Synthesis Results

The generated circuit is mapped using Quartus Tool in Altera Cyclone IV FPGA. It has 34 % of core coverage. Thus the synthesized circuit is very small. Thus we are not only able to synthesize the AHB Master from its formal specifications, but the synthesized circuit is also compact in term of resource utilization.

The Tool generated Synthesis results for designed AHB matrix is

Top-level Entity Name	AHB_MATRIX_TOP
Family	Cyclone IV E
Device	EP4CE40F23I7
Timing Models	Final
Total logic elements	13,615 / 39,600 (34 %)
Total combinational functions	13,449 / 39,600 (34 %)
Dedicated logic registers	534 / 39,600 (1 %)
Total registers	534
Total pins	33 / 329 (10 %)
Total virtual pins	0
Total memory bits	0 / 1,161,216 (0 %)
Embedded Multiplier 9-bit elements	0 / 232 (0 %)
Total PLLs	1 / 4 (25 %)

Fig 9: Synthesis results for implemented AHB matrix.

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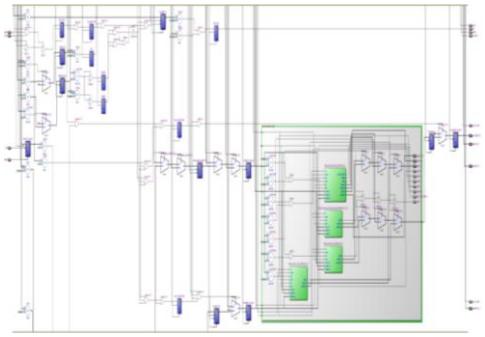

Fig 10 : RTL Schematic of Whole Matrix.

V. CONCLUSION

Using AHB protocol, the deadlocks can be avoided. Hence the loss of resources and data will be Minimized. To add flexibility and upgradability AHB protocol will be implemented by using FPGA as a target technology. In this project we observe that the data transfer operation fast as transfer is done as parallel communication in AMBA AHB. It also provides the opportunity to use master and slave up to 16 nos. and the data of every master is read and write simultaneously. The various scenarios for each component in the AMBA-AHB bus design are verified effectively during the simulation with respect to its behavior. We can use this protocol to interface between an ARM processor and any device provided both the IP cores should have AHB compliance. Data are successfully .

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BIOGRAPHIES

AV S R L BHARADWAJ received B. Tech Degree in Electronics and communication engineering from SS Institute of Technology in the year 2013. He is currently M. Tech student in VLSI SYSTEM DESIGN in VNR Vignana Jyothi Institute of Engineering & Technology, Bachupally, and Hyderabad, India. And his interested areas are in the field of low power and High speed VLSI Design.

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