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Design of SPI to I2C Bridge for High Speed Data Interfacing in Digital System

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Abstract: The purpose of this paper is to design and simulate the serial communication environment between SPI and I2C protocol with the help of the Bridge. By using the I2C as a slave side we can increase the number of I2C peripheral devices, it is not possible with SPI because it requires separate SS_n line for different slave devices which increase the board complexity. Most of the embedded systems having only SPI interface to connect with I2C peripherals. But it is not possible to directly connect SPI with I2C peripherals. The better option to deal with this problem is to build an SPI to I2C interface with the help of the Bridge. Bridge is commonly used for transforming or converting commands and data from one device to another to perform various applications. This effort mainly focuses on protocol conversion from SPI to I2C bridge, to interface with high speed digital system.

Keywords: SPI (Serial Peripheral Interface), I2C (Inter Integrated Circuit), Bridge, SCL (Serial Clock Line), SDA (Serial Data Line), Channel Selector.

I. INTRODUCTION

The Bridge helps SPI master to control a number of I2C slave devices for better transmission of information. This Bridge is developed using Open Source Tools because there are numerous commercial EDA tools are easily available but at a cost. They have many features and benefits, but have their own limitations. Cost saving is paramount important for a start-up or small size company. Commercial tools are closed nature i.e. file structures etc. and have limited customization features. Further to this open source developer and user community work in cohesion to achieve good software. So here ICARUS VERILOG or GTKWAVE are used.

II. SPI (SERIAL PERIPHERAL INTERFACE)

SPI is Serial communication protocol which is used in embedded system. It provides a simple connection with only four pins i.e. MISO (Master in Slave out), MOSI (Master out Slave in), SCLK (Serial Clock) and SSN (Slave Select).

Pin Description:
SCLK: Serial Clock line used to synchronize the data transfer. Master only can generate the Clock.

MISO: Master In Slave Out is a Serial Data Input (SDI) line used to send data to the master from a slave.

MOSI: Master out Slave in is a Serial Data out (SDO) line used to send the data from master to slave.

SSN: Slave Select signal which is active low line and for each device there is a different ssn. So to drive „n" no. of slaves on the bus master should have "n "SSN lines.

➢ **Data Transmission:**
To start a communication, the master device constructs the clock, by using a frequency which is supported by the slave device, normally up to a few MHz During each SPI clock cycle, a full duplex data transmission occurs, it means both transmission and reception occurs at separate line.

The master shows a bit on the MOSI line and the slave reads it, while the slave shows a bit on the MISO line and the master reads it. In this condition there is only one-directional data transfer is possible.

In any normal transmissions there are only two shift registers of some given word size, such as eight bits, one shift register in the master and one in the slave; they both are connected as shown in figure below.

Data is usually shifted out with the most-significant bit first to the slave register of slave device, while shifting a new least-significant bit into the same register. After that both the register has interchanged their register values.

If there are more data needs to be interchanged then the shift registers again loaded there values or repeats the process. Transmission may continue for any number of clock cycles.

When the transmission is completed, then the master stops switching the clock signal, and generally deselects the slave. The master must select only one slave at a time.

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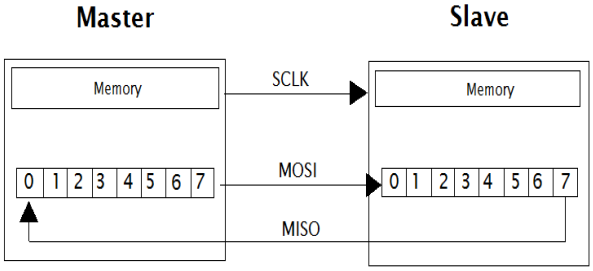

Figure 1 Data Transfer between SPI Master and Slave Device

II.I2C (Inter Integrated Circuit)

In I2C protocol communication become easy or without any data loss. I2C uses only two wires for communication i.e. SCL (Serial Clock Line) and SDA (Serial Data Line). It provides faster speed as compared to other protocols; also increases data transfer rate due to this it is light in weight, universal and efficient. I2C is used for accuracy and efficiency of data.

➢ **Data Transfer Rates** There is many cases in which large amount of data needs to be transferred. Many complex embedded systems contain a large number of different I2C devices, and in those cases it is very difficult to avoid collisions of the address, and also the 7 bits addresses allow only 127 different addresses where only 112 can actually be used. Due to this there are a few upgrades to the standard-mode I2C specifications:

- Fast Mode – data transfer rates up to 400 Kbit/s
- High-speed mode (Hs-mode) – data transfer rates up to 3.4 Mbit/s
- 10-bit addressing – supports up to 1024 I2C addresses

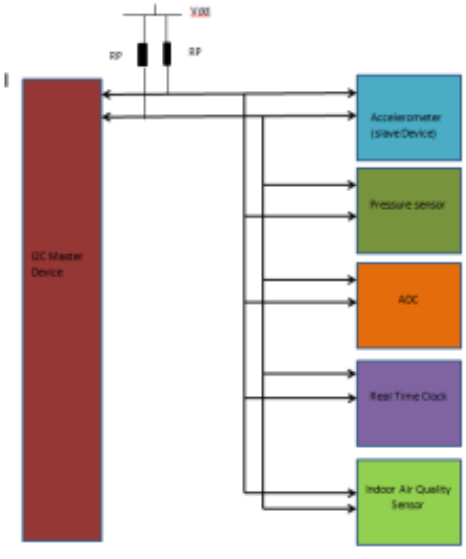

Figure 2 Block Diagram Of I2c

III. SPI TO I2C BRIDGE

A Bridge is a device used to convert normal or registered protocol e.g. SPI of one device to the protocol e.g. I2C which is suitable for the other device to attain the interoperability. Figure3 shows the block diagram of SPI to I2C Bridge .The working of the architecture is as follows:

➢ **WORKING OF THE BRIDGE**

A bridge consist of number of input and output pins and these pins are connected to many devices, first of all 32 bit inputs are given from the SS_n slave device, then the address of these 32 bit is calculated from the Address Encoder, which is 32 to 5 bit Encoder and also these 32 bit is NAND and give output high which is assume here as Enable pin, when this Enable pin is high then only the function of bridge starts. Enable pin passes to address Encoder, Address Frame Generator and Data Register. The output of the Encoder is of 5 bit and it goes to PISO (Parallel in Serial out) , it is having 8 bit shift register and its bit no. A1 to A5 generate address, A0 is used for R/W this R/W bit decides there is transmission or reception of the data occurs. If A0 bit is '0' then the data is transmitted from MOSI and if A0 bit is "1" then data is received from the MISO . Data from MOSI goes to input register SISO (Serial in Serial out) and if there's reception occurs then data passes to MISO pin from the output register SISO. The output of the PISO(Address Frame Generator) is "0X" where "0" indicates Address(A) and "X" indicates R/W bit and which goes to channel selector, channel selector is a 3 pin switch in which this "0X" is pin no.1, output of input register is pin no. 2, and the pin no.3 connected to the output register. Both the input and output register are controlled by the same clock SCLK. There are two pin at the output of the bridge one is the SCL serial clock line and other is SDA serial data line it is bidirectional both are controlled by the clock generator circuit .Data is transmit and receive from the Data register, it is the main switch of the channel selector which is connected to another 3 pin according to the address (A), R/W. If A = 1, R/W = 0 then it is connected with the input register, If A= 1, R/W = 1 then connected with output register .If A = 0, R/W = X.

Table 1 Channel Selector Logic

A	R/W	Data Register
0	X	Addr
1	0	MOSI
1	1	MISO

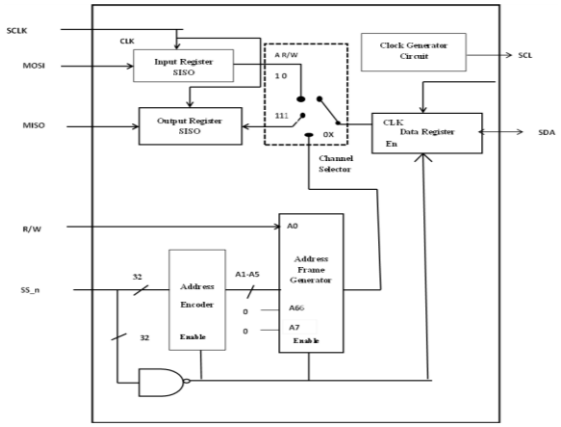

Figure 3 Architecture of SPI to I2C Bridge

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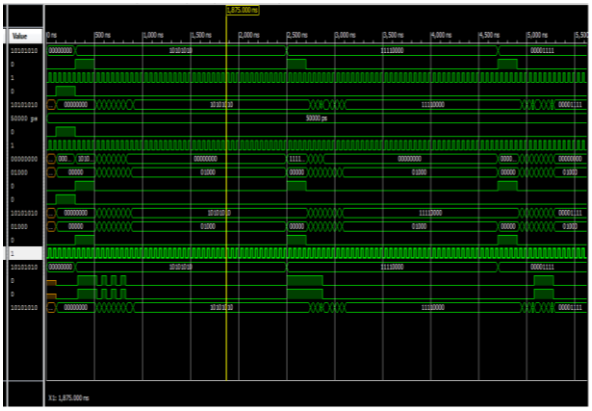
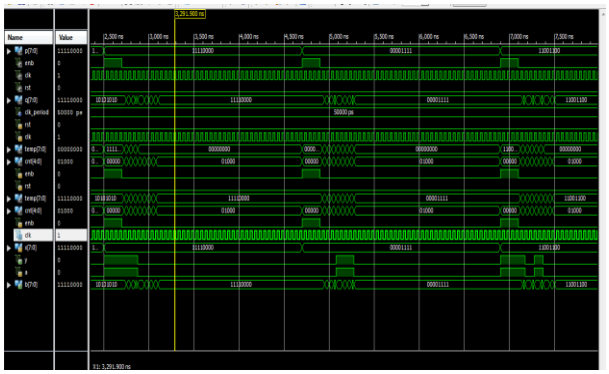
IV. SIMULATION RESULT

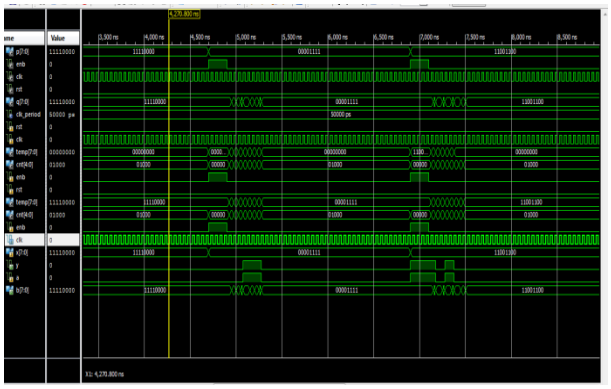
The SPI to I2C Bridge is designed by using Verilog and simulated using an Open Source Tools Icarus Verilog and GTKWave.Icarus Verilog is used for compilation or Simulation and GTKWave is used to analyze waveform.



Sending Data bit from 00000000 to 11001100



Sending Data bit from 10101010 to 11001100



Sending Data bit from 11110000 to 11001100

V. CONCLUSION AND FUTURE SCOPE

In this Paper the Simulation of the SPI to I2C Bridge is done by using Open Source Tools and these tools are advanced as compare to other tools. I2C is easily implemented in software. This work can be further extended to include, Dumping of Verilog code to FPGA to realize the exact hardware of the circuit. This will give an assessment of the area require, Bridge will also be design for Multimaster I2C device.

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