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# Review on a Compressor Design and Implementation of Multiplier using Vedic Mathematics

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**Abstract:** The Urdhva- Tiryagbhyam Sutra of Vedic mathematics and we have designed multiplier based on the sutra. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras which are discovered by Sri Bharti Krishna Tirthaji. We implement the basic building block: 16 x 16 Vedic multiplier based on Urdhva- Tiryagbhyam Sutra. This Vedic multiplier is coded in VHDL and synthesized and simulated by using Xilinx ISE 13.2. Further the design of array multiplier in VHDL is compared with proposed multiplier in terms of speed and memory. With the advent of new technology in the domain of VLSI, communication and signal processing, there is an ever going demand for the high speed processing and low area design. In this paper, introduces modified compressor based multiplier architecture. This modified structure uses the 4:2 compressor and 7:2 compressor architectures. In addition to that it uses Vedic mathematics to get a high speed multiplication operation and low area design. The design and experiments carried were carried out on a Xilinx Spartan 3E series of FPGA and discussed about the results of area and speed.

**Keywords:** High speed multiplier, 4:2 compressor, 7:2 compressor, modified architecture, vedic mathematics.

## I. INTRODUCTION

The Processor speed greatly depends on its multiplier's performance. This in turn raises the demand for multipliers high speed, at the same time maintaining low area and moderate power dissipation [1]. Over the past few decades, several new novel architectures are come for multipliers and have been designed and explored. Booth's [2] and modified Booth's algorithm based multipliers are quite popular in modern VLSI design but come along with their own set of disadvantages.

In these multiplier algorithms, the multiplication process, involves several transitional operations before received at the finishing answer. The intermediate stages include several additions, subtractions and comparisons which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand [3]. Since the speed is major concern, utilizing such type of architectures is not good approach since it involves several time consuming operations.

### 1.1. VEDIC MATHEMATICS

The Sanskrit word Veda‟ is derived from the root word „Vid‟, meaning to know without limit. The word „Veda‟ covers all Veda-sakhas known to the humanity. The Veda is a repository of all knowledge, fathomless, ever revealing as it's delved intense. It is mainly based on the 16 sutras which deal with various fields of mathematics such as algebra, geometry, calculus etc. Therefore the application of Vedic sutras to specific problems in Mathematics involves rational thinking, which helps the process improve intuition. It provides mental and superfast technique along with quicker cross-checking systems.

The Vedic math's converts complex calculations into a playful and blissful one which students learn with smiles. It is based on pattern recognition and hence allows for constant expression of a student's creativity, and it is to learn. The element of choice and the flexibility at each stage keeps the mind lively and alert to develop clarity of thought and intuition, hence a holistic development of the human brain automatically takes place during the process. It has an inbuilt potential to solve the problems of mathematics psychologically and also with anxiety.

## II. OBJECTIVE

With the advent of new technology in the domain of VLSI, communication and signal processing, there is an ever going demand for the high speed processing and low area design. In this project, introduces modified compressor based multiplier architecture. This modified structure uses the 4:2 compressor architectures.

In addition to that it uses Vedic mathematics to get a high speed multiplication operation and low area design. The design and experiments carried were carried out on a Xilinx of FPGA and discussed about the results of area and speed.

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## III. LITERATURE SURVEY

Vedic mathematics was proposed by former Jagadguru Sankaracharya of Puri and he proposed a set of 16 sutras (aphorisms) and 13 sub-sutras (corollaries) from the Atharva Veda and then he developed methods and techniques for amplifying the principles containing the aphorisms and their corollaries, founded by Swami Bharati Krishna Tirtha (1884-1960), and named it as Vedic mathematics. Hence there has been considerable literature on mathematics in the Veda-sakhas. Regrettably most of it has been gone to humanity until now. It has been evident from the fact that meanwhile, by the time of patanjali, about 25 centuries earlier, 1131 Veda-sakhas were known to the Vedic scholars and only about ten Veda-sakhas are presently in the knowledge of the Vedic scholars in the country. The Vedic sutras can be applied to various problems and Covers almost every branch of mathematics. They can be applied even to multiplex problems involving a large number of mathematical operations [2].

Chen et al (2003) presented low-power 2's complement multipliers by minimizing the switching activities of partial products using the radix-4 Booth algorithm. Before computation for two input data, the one with a smaller effective dynamic range is processed to generate Booth codes, thereby increasing the probability that the partial products become zero. By employing the dynamic-range determination unit to control input data paths, the multiplier with a column-based adder tree of compressors or counters is designed. To further reduce power consumption, the two multipliers based on row-based and hybrid-based adder trees are realized with operations on effective dynamic ranges of input data.

Wenet al (2005) a low power parallel multiplier design, in which some columns in the multiplier array can be turned-off whenever their outputs are known. In this case, the columns are bypassed, and thus the switching power is saved. The advantage of this design is that it maintains the original array structure without introducing extra boundary cells, as did in previous designs. Experimental results show that it saves 10% power for random inputs. Higher power reduction can be achieved if the operands contain more 0s than 1s. Compared with row-bypassing multipliers, this approach achieves higher power reduction with smaller area overhead.

VasefiFartashandAbid (2005) designed and simulated 4-bit ripple carry adders (RCA), 12-bit carry select adders (CSA), and a 4 times 4 Braun multiplier, based on lowest-number-of-transistor full adders. The designed full adders consist of 10 transistors and were used for n-bit adders with output voltage levels having a maximum of one threshold voltage (Vr) degradation. The 10 transistors adder achieved a 43.68% reduction in the power dissipation compared to the standard CMOS-28T adder. Power consumption can be further reduced by using an extra stack transistor. A 12- transistor adder was also designed for low area array multipliers.

Shanthala et al (2009) investigated various pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high throughput signal processing algorithms. The goal of this project is to design and VLSI implementation of pipelined MAC for high-speed DSP applications at 180nm technology. For designing the pipelined MAC, various architectures of multipliers and one bit full adders are considered. For checking the functionality of the whole system, spice code is written using the HSPICE by defining all the blocks in the circuit as the sub circuits.

Yu-Chi Tsao& Ken Choi (2012) proposed Area Efficient Parallel FIR Filter structure in which hardware savings for symmetric convolutions especially when the length of filter is long.

Ramkumar&Kittur (2012) proposed Low power and Area efficient carry select adder. In this work a simple and efficient gate-level modification significantly reduces the area and power of the CSLA. AddankiPurna Ramesh proposed radix-2 modified Booth algorithm MAC with SPST gives 7% less power consumption as compared to array MAC. Rekha K James, in her Ph.D thesis proposed efficient decimal MAC (Multiply Accumulate) architecture for high speed decimal processors based on IEEE 754-2008 Standard for Decimal Floating Point (DFP) Arithmetic. Shanthala et al proposed VLSI Implementation of Pipelined Multiply Accumulate Unit for Digital signal processing (DSP) applications at 180nm technology.

Kouretas &Ioannis et al (2013) presented techniques for lowpower addition/subtraction in the logarithmic number system (LNS) and quantifies their impact on digital filter VLSI implementation. The impact of partitioning the look-up tables required for LNS addition/subtraction on complexity, performance, and power dissipation of the corresponding circuits is quantified. Two design parameters are exploited to minimize complexity, namely the LNS base and the organization of the LNS word. A round off noise model is used to demonstrate the impact of base and word length on the signal-to-noise ratio of the output of finite impulse response (FIR) filters. In addition, techniques for the low-power implementation of an LNS multiply accumulate (MAC) units are investigated. Furthermore, it is shown that the proposed techniques can be extended to cotrans formation-based circuits that employ interpolators. The results are demonstrated by evaluating the power dissipation, complexity and performance of several FIR filter configurations comprising one, two or four MAC units.

### 3.1SUMMARY OF SURVEYED DESIGNS

- **Sri Bharti Krishna Tirthaji(1960):** Vedic mathmatics
- **L. Dadda(1965):** Some Schemes for Parallel Multipliers
- **Leonard Gibson Moses S and Thilagar M (2010):** Designed a high speed DSP algorithms using Vedic mathematics which is implemented in VLSI.
- **Manoranjan Pradhan, Rutuparna Panda, Sushanta Kumar Sahu(2011):**Speed Comparison of 16x16 Vedic Multipliers

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- **S.Kokila (2012):** Analyzed VHDL implementation of fast 32×32 multiplier based on Vedic mathematics. High speed, low power, less area and delay can be a achieved by designing multiplier.
- **R.P.Meenaakshisundari et.al. (2013):** Analyzed enhancing multiplier speed in fast fourier transform based on Vedic mathematics.
- **DigantaSengupta et.al. (2013):** Analyzed Vedivision - A Fast BCD division algorithm facilitated by Vedic mathematics to achieve a generalized algorithm for BCD division
- **Kavita and UmeshGoyal (2013):** Described FPGA implementation of Vedic multiplier which is implemented by using Gunakasamuchayah sutra.
- **Padmanabin Gopalakrishna and Gangavarapu Kiran Kumar (2013):** Described modeling of speed and area competent Vedic multiplier using Urdhva Tiryaghbhyam sutra.

## IV. VEDIC MULTIPLIER DESIGN

Urdhva-Tiryaghbhyamsutra: Urdhva-Tiryaghbhyam sutra is known as "vertically and crosswise" and it is a general multiplication formula which can be applied to all type of multiplication. The specialty of this sutra is that partial product generation and addition can be done simultaneously at the same time. It is more efficient in binary multiplication and it is suitable for parallel processing which in turn reduces delay in a design. The multiplication scheme can be explained by the following example as shown below in figure 1.1.

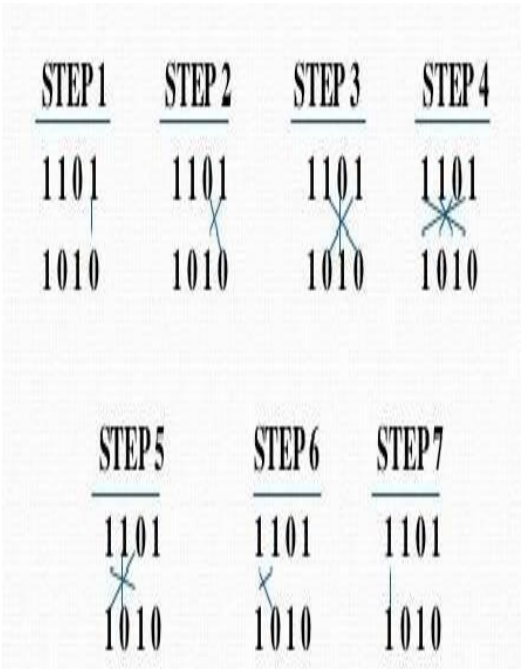


Fig. 4.1 Example of Urdhva-Tiryaghbhyam Using Binary Multiplication

This sutra is generally used for the multiplication of binary numbers and the multiplication formula can be applicable to all types of multiplication. In Vedic multiplier the computation time is less when compared with other multipliers and it is independent of clock frequency. Due to its regular structure it can be realized easily in a silicon chip [3].

Nikhilamnavatascaramamdastah: Nikhilam sutra is simply known as "All from 9 and the last from 10". The sutra can be very efficaciously applied in multiplication of numbers, which are nearer to basics like 10, 100, 1000 hence, to the power of 10[1]. The procedure of multiplication using the Nikhilam involves minimum number of steps, space, time saving and need only intellectual calculation. The numbers taken can be either less or more than that of the base considered. The dissimilarity between the number and the base is known as deviation. Deviation may be either positive or negative. The positive deviation is written without the positive sign and the negative deviation, is written using rekhank (a bar on the number). An example for nikhilam sutra is shown below in figure 1.2.

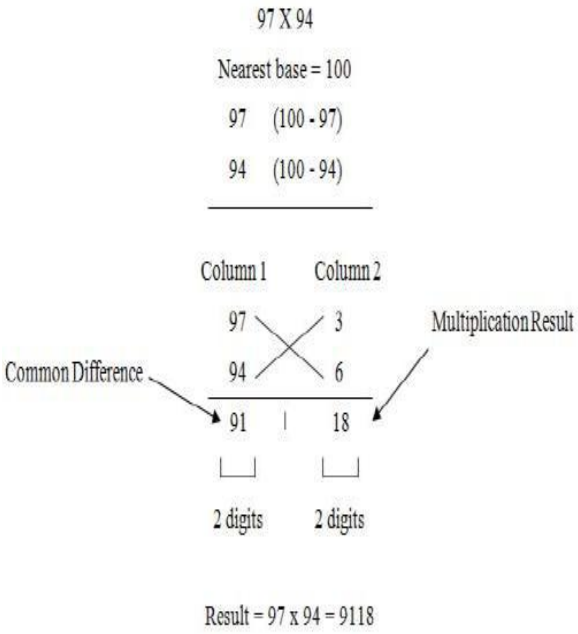


Fig.4.2 Example for Nikhilam Sutra

In various applications of digital signal processing, multiplication is one of the key components. Vedic technique eliminates the unwanted multiplication steps thus reducing the propagation delay in processor and hence reducing the hardware complexity in terms of area and memory requirement. We implement the basic building block: 16 x 16 Vedic multiplier based on Urdhva-Tiryagbhyam Sutra. This Vedic multiplier is coded in VHDL and synthesized and simulated by using Xilinx ISE 10.1. Further the design of array multiplier in VHDL is compared with proposed multiplier in terms of speed and memory.

The Urdhva- Tiryagbhyam Sutra of Vedic mathematics and we have designed multiplier based on the sutra. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras

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which are discovered by Sri Bharti Krishna Tirthaji. In this era of digitalization, it is required to increase the speed of the digital circuits while reducing the on chip area and memory consumption.

### 4.1 COMPRESSOR BASED ADDER

Several 4-2 and 7-2 compressor architectures have been used.Higher order compressors proposed used in the design. These compressors have been designed as counter of „1"s at the input bits. Two adder units and a Carry Look Ahead adder (CLA) unit for parallel addition of the outputs of the adder units. The 7-3 compressor is implemented using 4-3 compressor, a full adder and a CLA unit.

#### 4.1.1 3:2 Compressor

The 3:2 Compressors can add 3 inputs having a single bit and produces 2 bit output. The gate level structure of 3:2 compressors is as shown in Fig 4.1

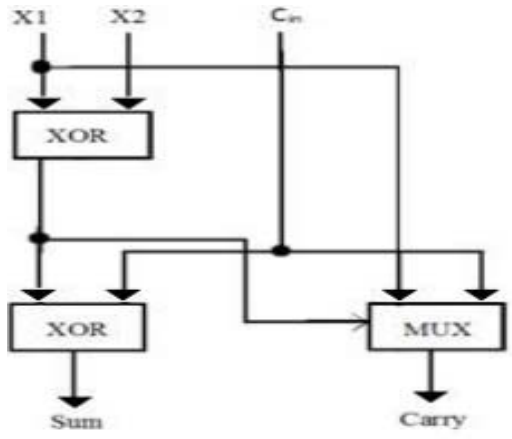


Fig 4.3 Gate Level Structure of 3:2 Compressors.

#### 4.1.2 4:2 Compressor

4:2 Compressors can add 4 single bit inputs and one carry input bit, which intern produces 3 bit output. Fig 3.2 shows the full adder design by using logic gates.

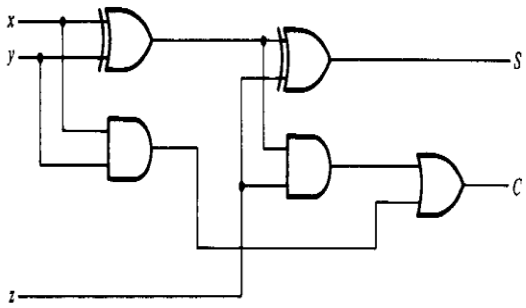


Fig 4.3 Full Adder Design by Using Logic Gates

The gate level structure of 4:2 compressors can be developed by using 3:2 compressors and it was shown in Fig 3.3. It can be observe that the critical path is smaller in comparison with an equivalent circuit to add 5 bits by using full adders and half adders.

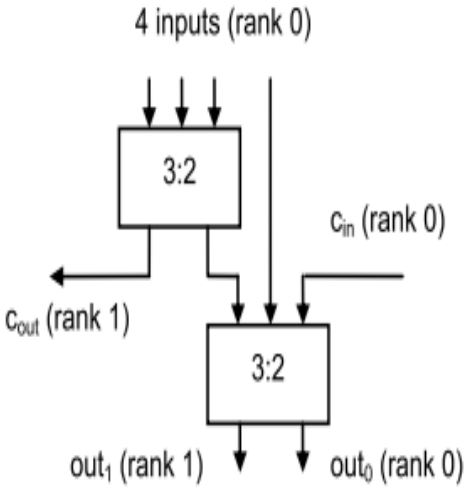


Fig 4.4 Compressor Architecture by Using 3:2 compressor.

### 4.2 COMPRESSOR BASED URDHWA TIRYAKBHYAM MULTIPLIER

The multiplication based on UrdhwaTiryakbhyam method requires more several full adders and half adders to add unnecessary partial products which lead to a large propagation delay. Fig 3.5 shows the Hardware architecture of 8x8 bit multiplier using 4:2 Compressor.So as part our novel structure approach, combined the compressor architecture and utilized the same in the existing Urdhwa based architecture in order to reduce the unnecessary partial products addition. The architecture for this design was shown in Fig 4.4.

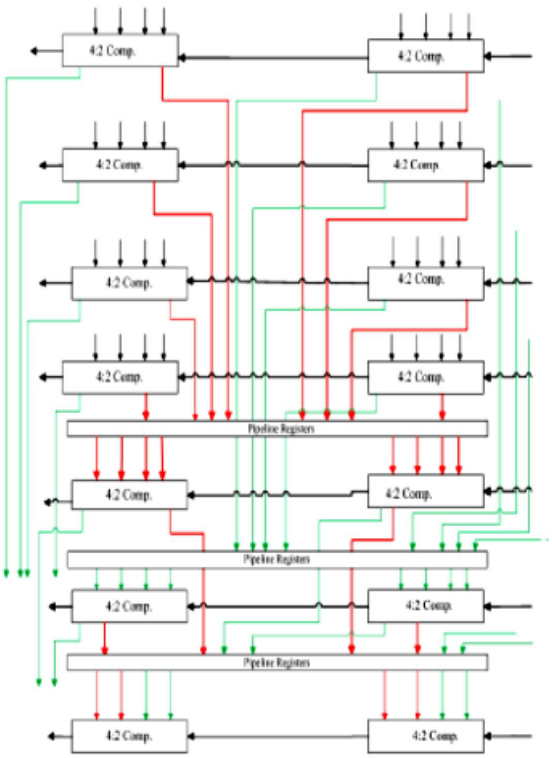


Fig 4.5 Hardware Architecture of 8x8 Bit Multiplier Using 4:2 Compressor

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The application of sutras saves a lot of time and effort in solving the problems, when compared to the formal methods presently prevailing in this field. Despite the solutions appear mysterious; the application of the sutras is perfectly logical and rational. The computation made on the computer chase in a way, the principles implicit in the sutras. The Vedic sutras provide not only methods of calculation, but also give a way of thinking for their application.

The Vedic math's converts complex calculations into a playful and blissful one which students learn with smiles. It is based on pattern recognition and hence allows for constant expression of a student's creativity, and it is to learn. The element of choice and the flexibility at each stage keeps the mind lively and alert to develop clarity of thought and intuition, hence a holistic development of the human brain automatically takes place during the process. It has an inbuilt potential to solve the problems of mathematics psychologically and also with anxiety.

## REFERENCES

[1]. A.D. Booth, "A Signed Binary Multiplication Technique," J. mech. Andappl. Math, vol 4, no.2, pp. 236-240, Oxford University Press, 1951.
[2]. L. Ciminiera and A. Valenzano, "Low cost serial multipliers for high speed specialized processors," Computers and Digital Techniques, IEE Proc. E, vol. 135.5, 1988, pp. 259-265.
[3]. M. Ramalatha, K. Deena Dayalan, S. Deborah Priya, "High Speed Energy Efficient ALU Design using Vedic Multiplication Techniques," Advances in Computational Tools for Engineering Applications, 2009, IEEE Proc., pp 600-603
[4]. www.google.com
[5]. www.wikipedia.com
[6]. www.study