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Performance and Analysis of Interleave Division Multiple access using Turbo Encoder

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Abstract: The efficiency of CDMA system is degraded with number of user increases. CDMA is limited by (MAI) and (ISI) Hence when number of user increases the BER performance also increased. The main limitation in CDMA is that it involves separate coding and spreading operations. A method to enhance the performance of IDMA System turbo codes can be applied to IDMA system, called Turbo coded IDMA System, which is presented recently for combing the advantages of turbo and IDMA. We use regular Turbo coder is used. IDMA uses repetition code. To mitigate MAI and ISI, turbo type iterative MUD (Multi User Detection) is used. In contrast to CDMA, IDMA uses the iterative chip-By-chip (CBC) detection algorithm to overcome intra-cell Interference. An interleave-division multiple-access (IDMA) system supports the presence of multiple users in a cell by resorting to a different interleaver per user. The results Show that the TURBO CODED IDMA is better than other FEC code like convolution code and LDPC code under the same Parameters. Turbo coded IDMA Provide high speed of communication services and low cost of receiver. Turbo codes are used in 3G/4G mobile communications. And in (deep space) satellite communications as well as other applications.

Keywords: AWGN Channel, BPSK Modulation, IDMA, Matrix Interlever, Random interleaver, Random inter leaver, Turbo Encoder.

1. INTRODUCTION

TURBO Coded IDMA scheme is the next generation mobile communication systems i.e. 4th generation (4G) are needed to support multiple services in different types of environments [1-3]. 4G is being developed to accommodate the QoS (quality of service) and required data rate such as wireless broadband access, Multimedia Messaging Service (MMS), video chat, mobile TV. This paper focuses the light on various multiple access techniques proposed in 4G communication systems. [6]

Turbo Encoder: Turbo codes (originally in French Turbo codes) are a class of high performance FEC codes. Turbo codes are used communications as well as other applications. A Turbo encoder is a parallel concatenation scheme with multiple constituent Convolution encoders. The first encoder operates directly on the input bit sequence, while any others operate on interleaved input sequences, obtained by interleaving the input bits over a block length.

The internal pseudorandom inter leaver spread the data sequence. The System block based Turbo Encoder block uses two identical 8-state recursive systematic convolutional encoders. Fig. show the basic configuration of turbo encoder, basically it is a recursive systematic encoder that employs two convolutional Encoders in parallel, where the second encoder is presented by an interleaver. The two recursive systematic convolutional encoder may be either identical or different. We observed that the nominal rate at the output at the turbo encoder is $R_{C=}1/3$.

However by puncturing the parity check bits at the output of the Binary convolutional encoder, we may achieve higher rate, such as rate 1/2 or 2/3. As in the case of concatenated block code, the Interleaver is usually selected to be a block pseudorandom interleaver that reorders the bits in the information sequence before feeding them to the second encoder. In effect, the use of two convolutional encoder in conjuction with the interleaver produces a code that contains very few code words of low weight .this characteristics does not necessarily imply that the free distance of the concatenated code is especially large, However, the use of the interleaver in conjunction with the two encoder result in code words that have relatively few nearest neighbors. That is, the code words are relatively sparse.

Hence the coding gain achieve by a turbo code is due in part to this feature, i.e. the reduction in the number of nearest neighboring code words that result from interleaving.

Benedetto and Montorsi (1996) have show that the number of nearest neighbors is reduced by a factor of N, where N is the block length of the interleaver.

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The second important aspect in achieving good performance with Turbo code is the use of iterative decoding based on the MAP criterion. The basic configuration of the iterative decoders Configuration shown in figure.

The iterative decoding algorithm usually employed in parallel concatenated convolution code is the BCJR algorithm described in the paper by Bahlet al. (1974) or some variation of this algorithm. We observed that the first decoder is provided with input from the demodulator corresponding to the information bits and the parity check bit P_1 .similarly the second decoder is provided with input from the demodulator corresponding to the Information bit and parity check bit P_2.

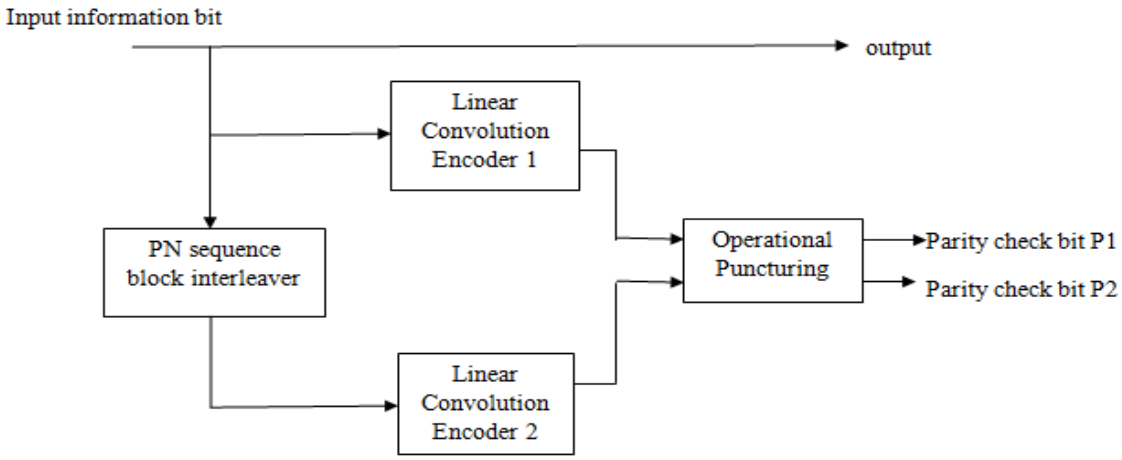

Fig1: Internal structure of turbo encoder.

2. TRANSMITTER CONFIGURATION

The received signal (r (j)) over AWGN channel for 'K' user is written as, $r(j) = \sum h_k x_k(j) + n(j)$, j=1,2.....J

Where h_k is the channel coefficient for user k and {n (j)} are samples of an AWGN with variance N0/2[5].

We assume that channel coefficients (h_k) are known a priori at the receiver. The receiver consists of an Elementary Signal Estimator (ESE) and a posteriori probability (APP) decoders (DECs) [7].The received signal r (j) which is to be de-interleaved and decoded with appropriate interleaver. For any receiver it is complex to retrieve the transmitted information by using various Multi User Detection (MUD) algorithms. In this IDMA receiver Elementary Signal Estimation (ESE) is used as detection algorithm. The ESE function is done as follows,

STEP 1. Initialize eDEC (x_k (j)) = 0

STEP2. Set E (xk (j)) = tanh (eDEC (xk (j)) / 2)

STEP3. Var (x_k (j)) =1- (E(x (j))) 2.

Find E(r (j) = Σh_k, E (x_k'' (j))

STEP4. Calculate Variance

$\text{Var}(r(j)) \Leftarrow \sum_{k'=1}^{K} |h_{k'}|^2 \text{Var}(x_{k'}(j)) + \sigma^2$

Finally find ESE function as,

$$e_{ESE}(x_k(j)) \Leftarrow 2h_k \frac{r(j) - E(r(j)) + h_k E(x_k(j))}{\text{Var}(r(j)) - |h_k|^2 \text{Var}(x_k(j))}$$

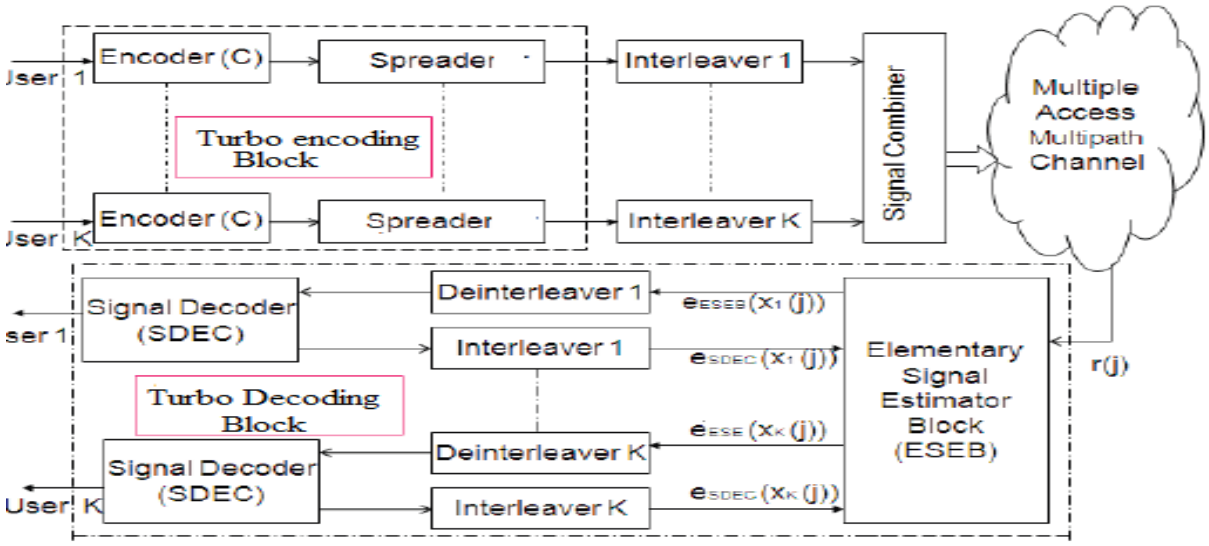

Fig 2: Transmitter and receiver configuration of turbo idma system with k user.

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Simulink model of transmitter and receiver structure of IDMA system:

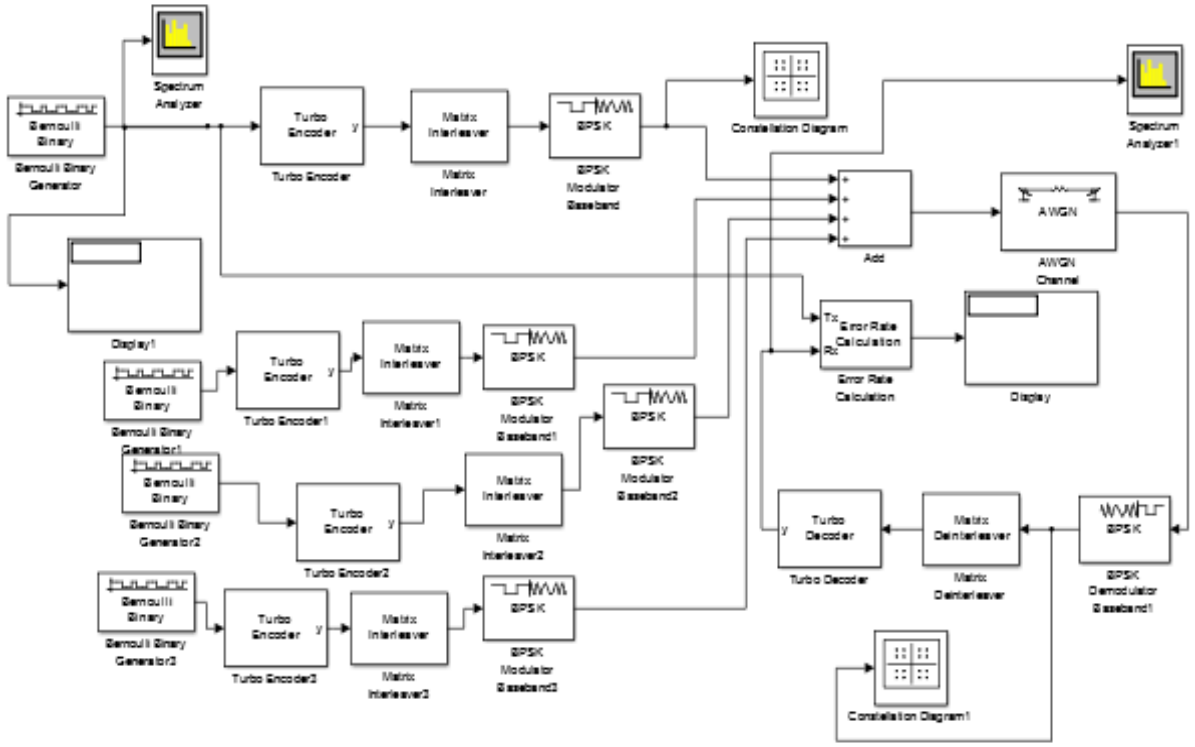
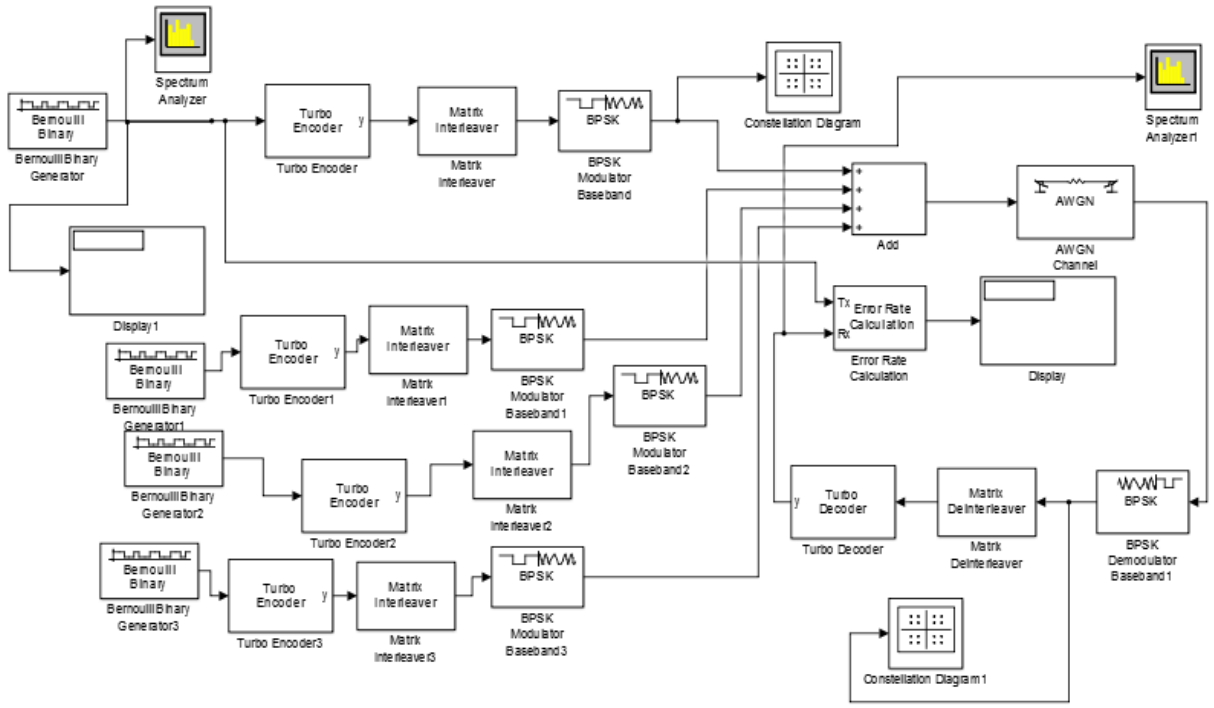


Fig 3: Simulink model of transmitter and receiver system:



Transmitter of Turbo coded idma system:

The transmitter of the turbo coded idma system consist of Bernoulli binary generator, Turbo encoder, internal random interleaver, matrix interleaver, BPSK modulation, and AWGN channel.[4]

Bernoulli binary generator: This block generates a binary signal with a Bernoulli distribution. The model requires three main parameters to be set:

1. Probability of zeros
2. Seed
3. Sample time

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In the simulation, probability of zeros is set to 0.5 means the same average number of ones and zeros occur in a particular time range. Seed defines the generator initial state and is set to 9876. The frame-based output with 180 samples per frame is to be set and output data type is set to be double.

Turbo Encoder: The turbo encoder is a forward error correcting code .That includes two recursive convolutional encoder and a pn sequence internal interleaver and punchring coder. The basic parameter of turbo encoder is Interleaver indices -:1:1.poly2trellis [4(13, 15)13]. Decoding algorithm True APP and chose decoding iteration.

Typically, four iteration are Adequate if the decoders are operating at a high enough SNR to achieve an error rate in the range10^{-5} to 10^{-6}, whereas, about eight to ten iteration may be needed when the error rate is in the Range of 10^{-5}, where the SNR is lower. [8]

Matrix Interleaver: Interleave the input vector by writing the elements into a matrix row-by-row and reading them out column-by-column. The product of Number of rows and Number of columns must match the input signal width. The matrix interleaver are converted total bit, in to row and coloum.

MODULATION OF IDMA: The processes by which some characteristics of a carrier are varied by an information signal. Here we have use BPSK (Binary phase shift keying)/QPSK. BPSK provide 180 deg Phase shift.while QPSK provide 90 deg.

Phase shift of carrier signal. This block accepts a column vector input signal. The input must be a discrete-time binary-valued signal. If the input bit is 0 or 1, respectively, then the modulated symbol is exp (jθ) or -exp (jθ), respectively, where θ represents the Phase offset parameter.

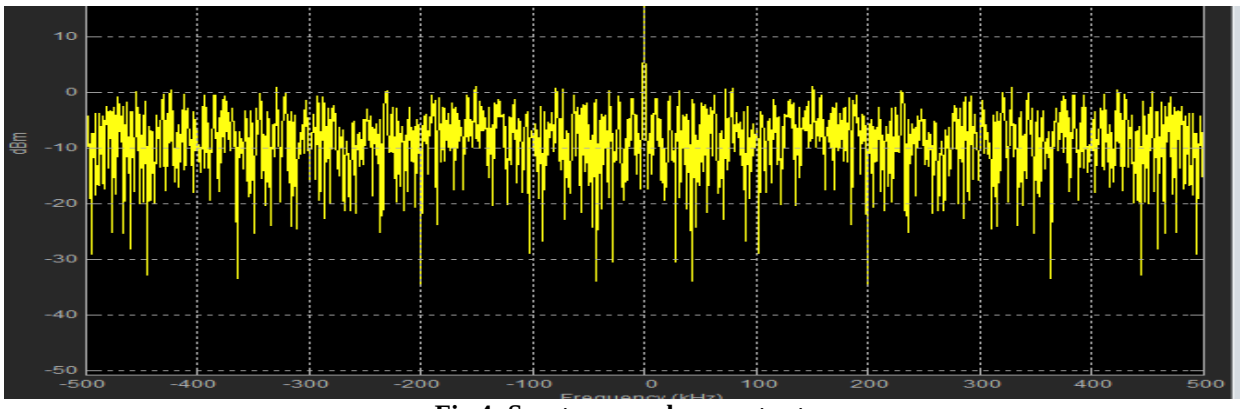

Fig 4: Spectrum analyzer output

AWGN Channel: The AWGN Channel block adds white Gaussian noise to a real or complex input signal. When the input signal is real, this block adds real Gaussian noise and produces a real output signal. When the input signal is complex, this block adds complex Gaussian noise and produces a complex output signal.
This block accepts a scalar-valued, vector, or matrix input signal with a data type of type single or double. The output signal inherits port data types from the signals that drive the block. All values of power assume a nominal impedance of 1 ohm.

Signal Processing and Input Dimensions:
This block can process multichannel signals. When you set the Input Processing parameter to frame based, the block accepts an M-by-N input signal. M specifies the number of samples per channel and N specifies the number of channels. Both M and N can be equal to 1. The block adds frames of length-M Gaussian noise to each of the N channels, using a distinct random distribution per channel.

BPSK Demodulator: The BPSK Demodulator Baseband block demodulates a signal that was modulated using the binary phase shift keying method. The input is a baseband representation of the modulated signal.

This block accepts a scalar or column vector input signal. The input signal must be be a discrete-time complex signal.

Matrix deinterleaver: Deinterleave the input vector by writing out row-by-row. The product of Number of rows and Number of columns must match the input signal width. The matrix deinterleaver convert Total bit in to, row and coloum.

TURBO DECODER: Decode input using a parallel concatenated decoding scheme that employs the a posteriori probability (APP) decoder as the constituent decoder. Both the constituent decoders use the same trellis structure and algorithm.
Use the poly2trellis function to create a trellis using the constraint length, code generator (octal) and feedback connection (octal). Here we have use Interleaver indices -:1:1.polly2trellis [4(13, 15)13]. Decoding algorithm True APP.[9]

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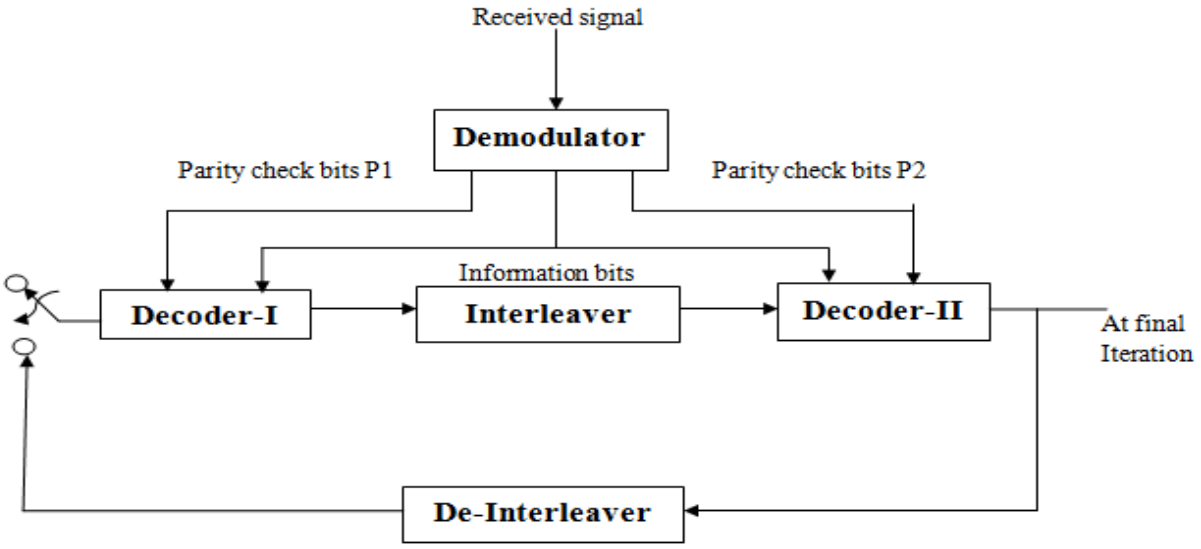

Fig 5: Turbo decoding

The Error Rate Calculation block

The Error Rate Calculation block compares input data from a transmitter with input data from a receiver. It calculates the error rate as a running statistic, by dividing the total number of unequal pairs of data elements by the total number of input data elements from one source. Use this block to compute either symbol or bit error rate, because it does not consider the magnitude of the difference between input data elements. If the inputs are bits, then the block computes.

3. RESULT AND DISCUSSION

Turbo idma scheme uses 4 iteration are adequate if the decoders are operating at a high enough SNR to achieve an error rate in the range 10^{-5} to 10^{-6}, whereas, about eight to ten iteration may we needed when the error rate is in the range of 10^{-5}, where the SNR is lower. The future work of the turbo coded idma scheme is to reduce large interleavers decoding delay and the computational complexity inherent in the iterative decoding algorithm.

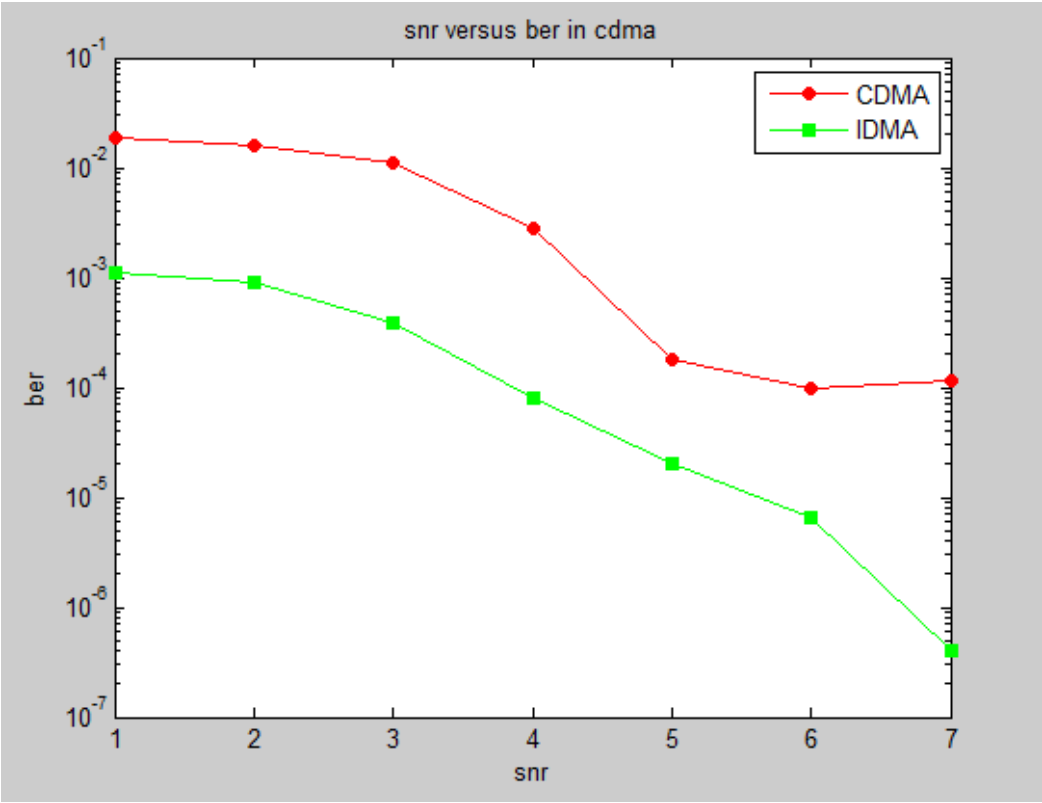

Fig 6: Compare between CDMA systems Turbo coded IDMA system system.

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4. CONCLUSION

In this paper, The Turbo coded IDMA show high speed of communication services and low cost of receiver. Basically the Turbo code is high performance forward error correcting code it minimize the bit error rate on lower snr. The per-user computational complexity of the chip by chip is independent of the number of users involved. The Turbo coded idma system provide Superior performance a rate ½ or 2/3 turbo code of block length $N=2^{12}$ with 6 iteration of decoding per bit, achieves an error probability of 10^{-5} at an SNR of 6 dB. The drawback of Iterative decoding is that it produce large decoding delay and computational complexity in the Iterative decoding algorithm. In most data communication system, however, the decoding delay is tolerable, and the additional computational complexity is usually justified by the significant Coding gain that is achive by the turbo code.

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