Design of a Low Power Two Stage Operational Amplifier using MT-CMOS Technology: A New Approach

Neha Shukla

P.G Scholar, Electronics and Communication Engineering, P.E.C University of Technology, Chandigarh, India

Abstract: The birth of 'Moore's Law' provided a great insight to electronic industry. As a result of which so many technologies are adapted to increase the number of components on integrated circuits. One of which is Scaling .As scaling of technology is adapted, performance and efficiency of devices is improved to a great extent. But on the other hand power dissipation has become a matter of great concern. And it becomes the main constrain when it comes to portability of any electronic device. The operational amplifiers need no introduction as this device has become an integral part of fields like instrumentation, automotive and so on. So, this paper is proposing a design of a low power operational amplifier using MT-CMOS Technology. Various technologies for low power dissipation are also considered in this paper along with their advantages and disadvantages.

Keywords: MT CMOS, Cadence, VT-CMOS, Opamp.

I. INTRODUCTION

The era today is a era of fast and competitive society which means that the basic requirement is every activity to be performed very fast. As operational amplifier is a very versatile device which performs numerous operation in various electronics applications/ There is a wide research is going on in the field of operational amplifier. This paper basically is divide into seven sections which starts with a question of "why there is need of low power"? and followed by various existing technologies for low power, their advantages and disadvantages are discussed .After that this paper will explain in detail about MT-CMOS technology.

II. NEED OF LOW POWER

Gordon Moore wrote a article named "CRAMMING MORE COMPONENTS ONTO INTEGRATED CIRCUITS." (April 19, 1965). In this article he made a simple calculation about the number of transistors on single IC. He was the DIRECTOR of research and development laboratory of FAIRCHILD National Semi-conductor .In 1965 there was the IC with 32 transistors, in 1966, the number of transistors increased to 64. So a very intellectual prediction was made that by "1975 the number of components per integrated circuit for minimum cost will be 65,000."That prediction came true in 1975 he modified his prediction that "component density doubles every year". This prediction still holds not only for microprocessors but also for DRAM technology where CMOS are used. To continue to improve the performance of the circuits and to integrate more functions into each chip, feature size has to continue to shrink. As a result the magnitude of power per unit area is growing and the accompanying problem of heat removal and cooling is worsening. Thus lots of money and time should be invested on cooling system and heat removal. So to avoid such thing there is a need of low power design. Portable battery powered applications are characterized by low power computational requirement. Another major demand for low power chips come from environmental concerns. Modern offices are now furnished with office automation equipments that consumes more power.

III. VARIOUS LOW POWER TECHNOLOGIES

There are many consequences for power dissipation like short channel effect (hot electron effect, latch-up, floating gate, velocity saturation and many more).These short channel effect arises only due to scaling. So various low power technologies are used to overcome this huge problem of power dissipation. There are some following technologies which were implemented with the thought of decreasing power dissipation in devices.

A. Clock Gating
Since power dissipation in VLSI is of two types. One is static and another is dynamic. There are separate reasons behind these types of power dissipation (due to internal leakage current). Since we know that if we decrease the power

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supply to any device, it will straight away reduce dynamic power consumption but at the cost of increased delay which is highly undesirable. So there is technology which was introduced with the motive of decreasing power consumption without entertaining the problem of delay .The technology was clock gating. It is basically based on a principle of disable the clock while it is not required. The gate is used for enabling and disabling the clock. The motivation is basically reducing the switching frequency by disabling the clock. So whenever the clock is not needed the output is not changed at all.
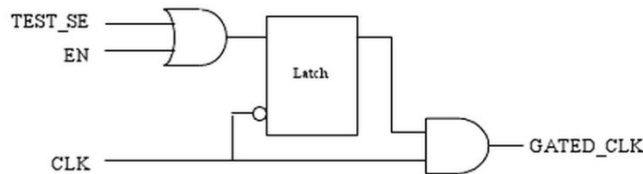
Figure 1: Clock Gating Circuit

B. Variable Power Supply
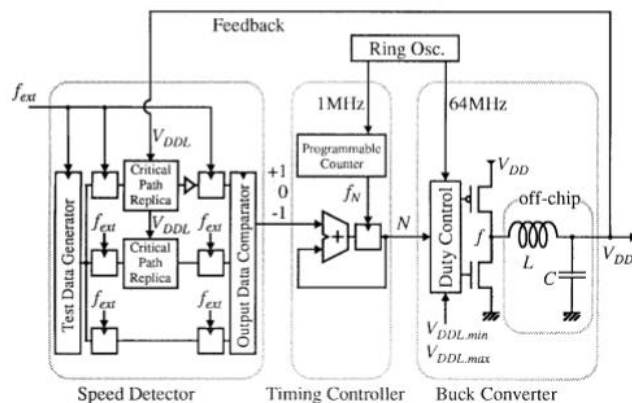
Figure 2: Variable Power Supply Circuit

This is variable VDD scheme. The buck converter generates a VDD for internal supply voltage. When VDDL is too low the speed detector will give output as 1and VDDL is too high it will give -1. This is versatile method to generate a variation in supply voltage.

C. VTCMOS

It is accomplished by using variable substrate to obtain variation in threshold voltage .It is entirely based on the fact that basically the doping density is varied to obtain variable threshold voltage.
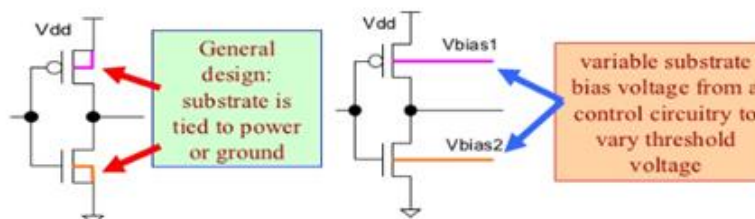
Figure 3: Variable Threshold Circuit

Advantages of individual technology:
1. VTCMOS is having considerable lesser area
2. Power reduction is considerable
3. Clock gating is highly effective to reduce dynamic power by controlling switching activity.
4. Variable power supply is a great example of scaling which reduce power dissipation in a very accurate way

Disadvantages of individual technology:
1. VTCMOS requires triple well or twin well technology for obtaining variable substrate
2. Clock gating introduces large area overhead.
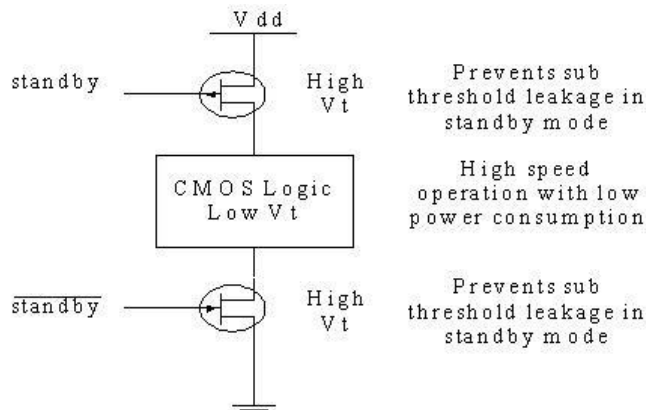
IV. INTRODUCTION TO MTCMOS

Figure 4: Power Gating Circuit

The word MTCMOS defines the operation itself as a circuit with multiple voltage. This is also known as power gating . This figure 3 illustrate that there is one MOS transistors between VDD and CMOS logic and another transistor is placed between ground and CMOS logic. The whole idea is to control leakage current which is the major cause for static power dissipation. Both these MOS transistors are having high V Twhile CMOS logic is having low V_T. When no VDD is applied, that mode is known as stabndby mode. So there will be open cirvuit between CMOS logic and ground. Hence no leakage current flow hence no power dissipation. While in normal condition it will work normally as CMOS logic. Its main advantage is it has lesser area overhead, considerable power reduction and lesser delay. This idea is utilized to make a opamp with MTCMOS technology. The purpose is to reduce leakage current in standby mode .Since opamps consist of a differential apmplifier and a gain amplifier followed by a buffer. The gain amplifier is used so that the gain of differential amplifier is increased. To design such circuit in cadence we need to assume some of the parameters which are:

1. SR (Slew rate)=5v/microsec
2. Load capacitance is of 10Pf
3. ICMR (+)=1.6V
4. ICMR(-)=0.8V

Along with these parameters we require atleast 10-12 MOS transistors (NMOS and PMOS).Cadence tool is used to simulate and obtain results. Some steps has to be followed ar as under:

1. Make a Opamp
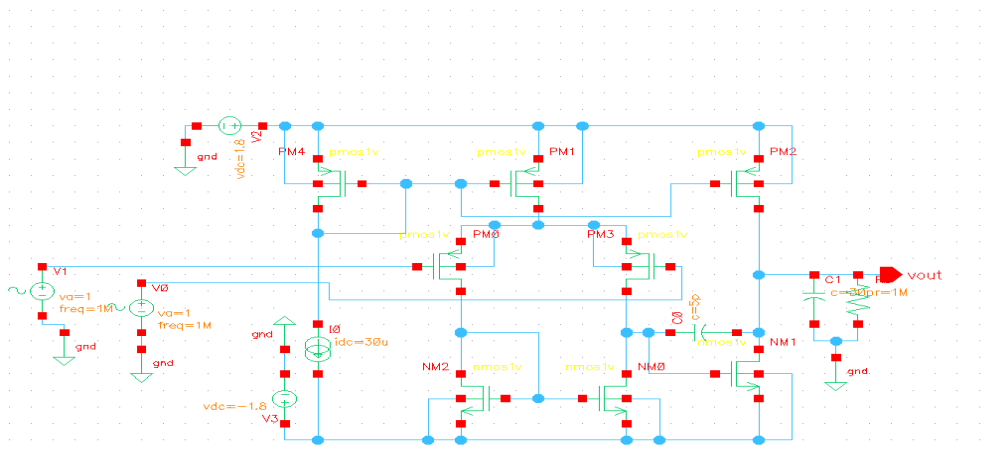This figure 5 is two stage operational amplifier.

Figure 5: Two Stage Opamp

Use of MTCMOS
For this, MOS transistor has to be inserted in between VDD and opamp and another MOS between ground and opamp. By using this the standby leakage current will be reduced as a result the power dissipation will also be reduced which is the fundamental requirement of any circuit.

V. CONCLUSION

Thus from these above facts and figures we came to result that MTCMOS technology is a very powerful technology as far low power VLSI is concerned. It is observed that MTCMOS technology in VLSI helps in reducing power dissipation to great extend and hence it should be used widespread to enhance the efficiency and battery life of any VLSI technology based device as it will lead to reduction on power dissipation.

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BIOGRAPHIES

Neha Shukla She is a P.G Scholar in P.E.C University of Technology Chandigarh, pursuing MTECH in VLSI Design. She has also published her paper in ICMTES-2017 & in IJIREEICE.