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Design 0.4v Low Power Class AB CMOS Operational Transconductance Amplifier

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Abstract: Importance of low voltage low power analog design techniques is increased due to modern trends towards use of battery operated portable electronics. This paper presents the low voltage power efficient class AB CMOS operational transconductance amplifier with enhanced gain and bandwidth operating at 0.4V. Complementary NMOS and PMOS differential pair is used to achieve rail to rail input stage are biased using two level shifter adaptive bias techniques to improve slew rate. Low voltage low power operation is achieved by operating transistors in weak inversion region. Class AB output stage, in which transistors connected in common source configuration, is employed. High CMRR is obtained by CMFF circuit which also biases the output stages. Operational transconductance amplifier (OTA) is designed in LTSPICE using 90nm DSM technology.

Keywords: OTA, weak inversion, adaptive bias, CMRR.

I. INTRODUCTION

Modern wireless devices and portable electronics require power efficient operation and enhanced power to performance ratio in order to decrease size and to extend the battery life. Transistors are widely practised basic building blocks for analog design as well as mixed signal systems.
OTAs have fast settling response besides power efficient and low voltage operation which is not limited by slew rate. As maximum output current is limited by the bias current, there is trade-off between power consumption and slew rate.
In analog design, the device consumes less power for desirable operation when operating in weak inversion region [1]. As primary goal is to save energy and increase battery life, weak inversion region is found to be more helpful for energy constrained applications.
Operational transconductance amplifier (OTA) is voltage controlled current source widely used for variety of analog applications such as sample & hold circuits, data convertors, switched- capacitor filters, buffer amplifiers, etc. [2].
The main aim this work to design fully differential two stage operational transconductance amplifier with improved gain using 90nm technology. The main features are power efficient and low voltage operation in weak inversion region, class AB output operation, two level shifter adaptive biasing and improved slew rate.

II. LITERATURE SURVEY

Effective implementation of the design needs deep study and analysis of various papers. Literature survey is as follows:
Rail to rail input stage is required such that circuit has to work faithfully at any common mode signal. PMOS and NMOS differential pairs are used to reach negative supply rail and positive supply rail. Full rail to rail common mode input range is achieved by placing PMOS & NMOS differential pair in parallel configuration [1].

As maximum output current is limited by bias current, input stage of classical class A op-amp failed to achieve power efficient operation and high slew rate. Bias current in weak inversion region is quite smaller. Adaptive bias circuit is used to overcome the problem. When large differential signal is applied, it boosts dynamic current above quiescent level [2]. Two level shifter (TLS) has double transconductance when compared with winner take all (WTA).
For effective operation of fully differential op-amp, high common mode is essential to reject common mode input signals. Common mode feed forward (CMFF) or common mode feedback (CMFB) can be used to achieve high CMRR. Output stage is also biased by CMFF [3].
Cascade compensation technique has advantage over miller compensation techniques. Miller compensation techniques failed to achieve high speed, high PSRR as compared to cascade techniques [4].
Conventional class AB output stage when connected in classical common drain configuration falls short rail to rail voltage. This issue is overcome by connecting the rail to rail output stage in classical common source configuration [5].
This paper is organized such that section III gives description of OTA, while section IV & V gives result for 90nm CMOS design and conclusion respectively.

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III. DESCRIPTION OF OTA

Conceptual block diagram of the proposed operational transconductance amplifier is shown in fig 1. This OTA is divided in two main parts: the first part containing the core of op-amp having class AB output stage and rail to rail complementary differential input stage, second part containing the common-mode feed-forward circuit (CMFF), where both core and CMFF circuits are composed by adaptive biased complementary input pairs.

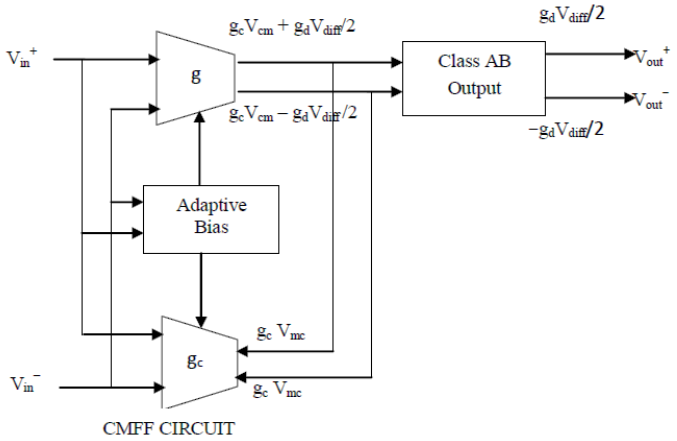

Fig.1: Conceptual block diagram of The Proposed Operational Amplifier [1].

Main operation of transconductance amplifier is to convert the input voltage current at differential input stage into output currents with respect to transconductance g_d & g_c which are transconductance of differential and common mode voltages respectively.

A. Rail – Rail Input Stage

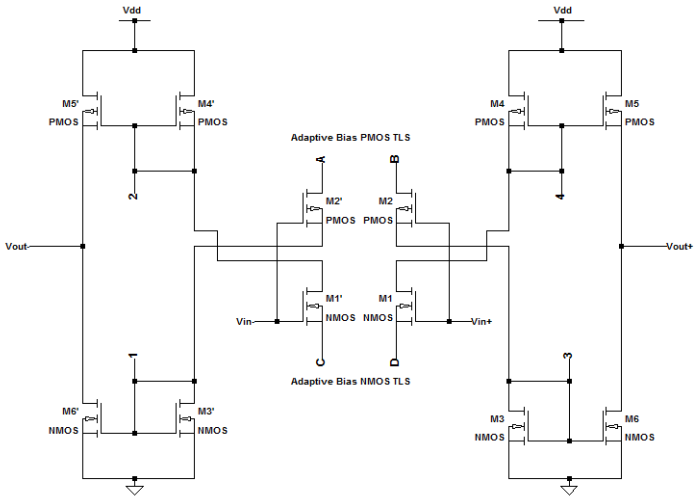

Fig. 2: Core of proposed op-amp with complementary rail to rail stages and class AB output stage

Complementary differential pairs are used to achieve full rail to rail operation. P-channel MOS device used to reach negative supply rail while n-channel MOS device used to reach positive supply rail.
As shown in fig. 2 NMOS and PMOS transistors (M1, M1' and M2, M2' respectively) operating in weak inversion region for low voltage operation are connected together parallel.

B. Class AB Output stage

The whole input cycle is amplified by Class A amplifier but when no input signal is applied, it remains active and consumes more leakage power. While Class B amplifier amplifies the half input cycle and gets off for other hall cycle which consumes less power than class A. Class AB amplifier is used to avoid trade between Class A & B. Operation of class AB amplifier is same as class B but it conducts small for remaining half cycle.

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As shown in fig. 2 for class AB output operation, transistors M5 andM6 are connected in common source configuration to ensure maximum output range.
All the transistors M3, M4, M5 & M6 operate in weak inversion region.

C. Adaptive Bias Circuit

In weak inversion region, as the bias current is usually very small, obtaining large output current is quite difficult.
When large differential input signal is applied, adaptive bias circuit ultimately boosts dynamic current. While it keeps maximum current levels above the quiescent current. High slew rate and low voltage and power efficient operation is achieved by adaptive bias circuit. Two level shifter (TLS) is used over winner take all (WTA) as adaptive bias technique to obtain boosted slew rate. Following fig shows NMOS and PMOS two level shifter respectively.

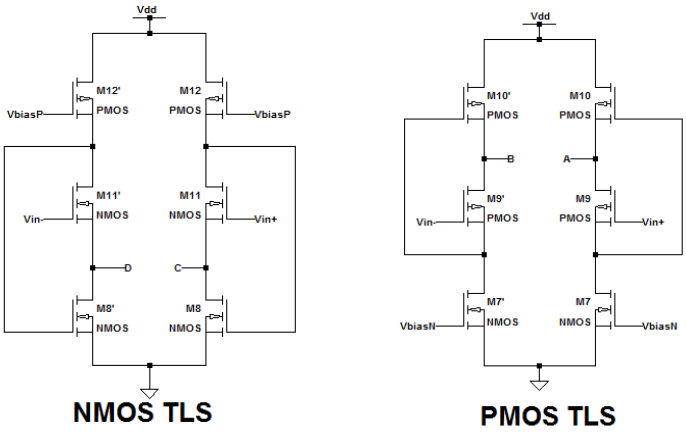

Fig. 3(a): NMOS Two level shifter (b): PMOS Two level shifter

PMOS and NMOS differential pairs used for full rail to rail input stage are biased by PMOS TLS and NMOS TLS respectively. All the transistor in two level shifter such as M8(M8'), M9(M9'), M10(M10') and M11(11') are operate in weak inversion region except M7(M7') and M12(M12'), these operates strong inversion region.
In case of NMOS TLS, All the transistors of TLS are off for $V_{in} < V_{th}$ except M12(M12') operates in deep triode region. As V_{in} sufficiently increases above threshold voltage, small standby current is generated which biases the rail to rail differential pair and helps to achieve low power operation and improved slew rate under dynamic condition.
The operation of PMOS TLS is same as NMOS TLS.

D. CMFF Circuit

To reject common mode signal, high CMRR is needed. CMFB and CMFF are used to obtain high CMRR.

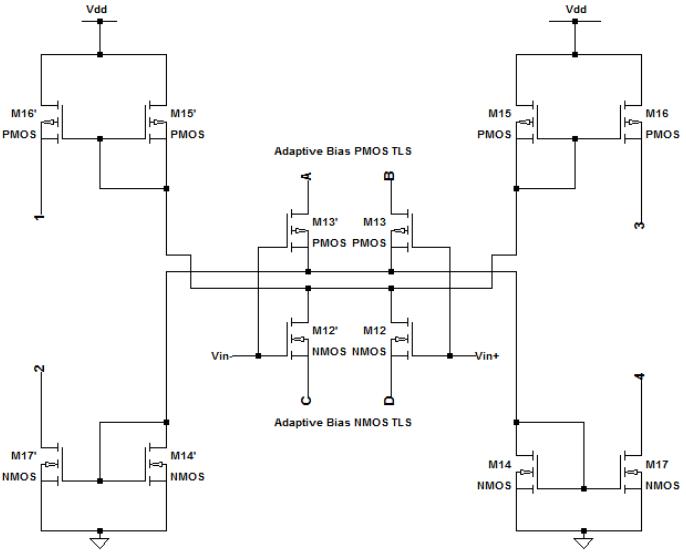

Fig. 4: CMFF Circuit

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Disadvantage of CMFB is complex circuitry due to presence of detector followed by comparator.
CMFF circuit enhances the CMRR as well as removes the dependences of output current I_{out}+, I_{out}-. It also biases the output stages of proposed op-amp. Fig 4 shows the schematic of CMFF circuit.
Transistors of CMFF circuit operate in weak inversion region. Current generated by M12-15 and M13-14 are added to the core op-amp by means of M16 and M17 respectively.

IV. RESULTS AND DISCUSSION

Performance of proposed op-amp is expected to be better than previous ones which is seen from comparison between this work and formerly proposed operational amplifiers is shown in Table 1 which explains the performance of proposed OTA. Referring to simulation results which are taken as primary results from operational transconductance amplifier biased using WTA adaptive bias technique are shown in fig 5,6and 7. Fig 5, 6 shows DC gain of 44.24dB and unity gain bandwidth of 363 kHz and phase margin 88° respectively while transient response is shown in fig. 7.
The proposed OTA is being designed with 0.4V DC supply voltage in LTSPICE tool using the low cost 90nm technology for CMOS. Proposed OTA will be designed for open loop DC gain greater than 50dB with unity gain frequency 1MHz in which load capacitance 10pF connected at each output. Power consumption for proposed OTA will be less than 5µWatts.

Table1. Comparison between op-amp performances

Parameter	[1]	[6]	[7]	This work (Expected)
Supply Voltage	0.8V	0.4V	0.4V	0.4V
Technology	180nm	90nm	90nm	90nm
DC gain	51dB	44dB	51dB	>50dB
Unity Gain BW	40kHz	365kHz	870kHz	1MHz
Slew Rate	0.12V/µs	0.05 V/µs	0.1V/µs	>0.1V/µs
Phase Margin	65°	88°	77°	>65°
Power	1µW	4µW	4.78µW	<5µW

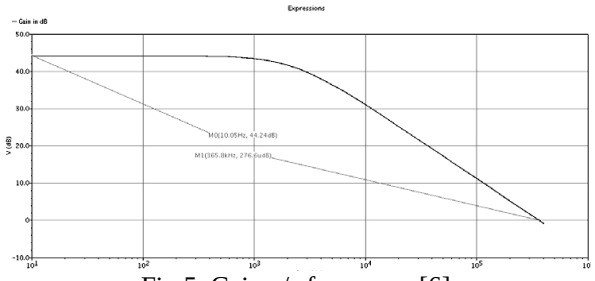

Fig 5. Gain v/s frequency [6]

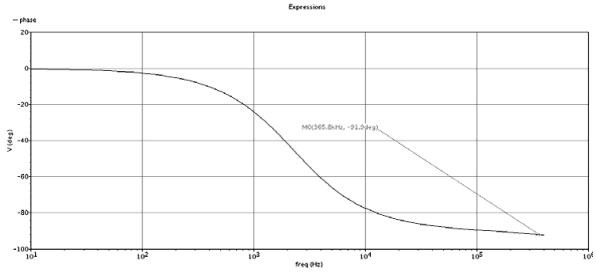

Fig 6. Phase v/s frequency [6].

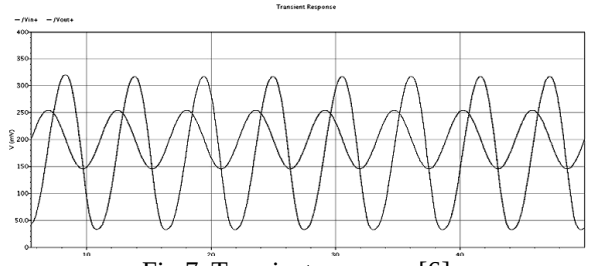

Fig 7. Transient response [6]

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V. CONCLUSION

Fully differential Class AB CMOS OTA with low power and low voltage is proposed with enhanced DC gain and bandwidth depending on the need to reduce power reduction and increased demand of portable battery equipped devices. It is clear from expected results that proposed OTA is efficient than previous one. Operations are carried out at very low supply voltage for proposed OTA to achieve low voltage power efficient operation and could have wide range of applications in analog circuits. Proposed OTA is designed using low cost 90nm DSM technology to reduce chip area.

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