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A Review on Soft Errors and Different Fault Tolerance Techniques

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Abstract: With fabrication technology reaching nanolevels, systems are becoming more prone to manufacturing defects with higher susceptibility to soft errors. Soft errors caused by particles strike in combinational parts of digital circuits are a major concern in the design of reliable circuits. Several techniques have been presented to protect combinational logic and reduce the overall circuit Soft Error Rate (SER). Such techniques, however, typically come at the cost of significant area and performance overheads. A comprehensive review on the soft error generation and different fault tolerance techniques used, are presented in this study. After the overall concepts and general ideas are presented, representative works as well as new progress in the techniques are covered and discussed in detail.

Keywords: Fault tolerance, Soft errors, Single event upset, Single event transient, Soft error tolerance.

I. INTRODUCTION

Soft errors arise from single event upsets (SEU) [1], which are caused by energetic particles (neutrons and alpha particles). Device scaling and density increasing make integrated circuits become more and more susceptible to soft errors. Satisfying soft error requirements is increasingly challenging for high-performance, deep-submicron CMOS [2] circuit applications. Aggressive scaling of the power supply voltage, reduction in the minimum feature size, and the use of flipchip packaging has increased the susceptibility of a circuit to soft error events. Memory arrays can be especially prone to soft error events due to their small cell size and infrequent changing of logic states. For these reasons as well as the ease of testability, memory elements have been used to perform much of the soft error characterization performed to date. To reduce the susceptibility of soft error events in the memory arrays, the implementation of circuit based solutions to protect the memory arrays from soft errors has become standard practice at the expense of a larger die size. Fault tolerance is a major concern in safety critical applications. This issue has been studied by the scientific community for decades but the technology progress, with the advent of nanometre technologies, and the increasing complexity of current circuits pose new challenges and difficulties to solve.

In this paper, different fault tolerance methods used to overcome soft errors are described. Circuit designers must add some SE protection features into a circuit during the design phase at the expense of performance loss.
The compromise between soft error rate (SER) reduction [11] and performance penalty as well as the time spent on addressing and managing the SE problem is ultimate goal of the battle against SEs. Technology scaling and architectural movement profoundly affects the increase in SE vulnerability of combinational logic circuits. Not only do small technology node circuits have very low electrical masking [4] against SE, super-pipelining can also reduce logic masking of logic gates between pipeline stages. Moreover, an increase in clock frequency can increase the probability that a glitch induced by SE can propagate to a latch. For soft error protection, various approaches including hardware, software, and coding based techniques, which are applicable to storage elements, have been studied. Error Correcting Codes (ECCs) are widely used to recover bit flips in conventional memories.

Fault detection/tolerance techniques are used when fault avoidance alone cannot economically be used to meet reliability requirements during design.

II. A GATE-LEVEL RADIATION HARDENING TECHNIQUE

A gate-level radiation hardening technique [3] for cost effective reduction of the soft error failure rate in combinational logic circuits is described. The key idea is to exploit the asymmetric logical masking probabilities of gates, hardening gates that have the lowest logical masking probability to achieve cost effective tradeoffs between overhead and soft error failure rate reduction. The asymmetry in the logical masking probabilities at a gate is leveraged by decoupling the physical from the logical (Boolean) aspects of soft error susceptibility of the gate. Gates are hardened to single-event upsets (SEUs) [11] with specified worst case characteristics in increasing order of their logical masking probability, thereby maximizing the reduction in the soft error failure rate for specified overhead costs (area, power, and delay).Gate sizing for radiation hardening uses a novel gate (transistor) sizing technique that is both efficient and accurate.

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A. Problem Statement

Given a mapped combinational circuit composed of gates from a technology library. For each gate g in the circuit, several different sizes 1, 2, . . . , k are available in the library, each of which implements the same logic function but differs in one or more of the following aspects—area, delay, drive strength, and power consumption. The gate sizing problem for SEU immunity is to select optimum sizes for each (or a subset) of the gates in the combinational logic circuit such that the objective function—defined by the susceptibility of the logic circuit to SEUs (i.e., the soft error failure rate of the logic circuit)—is minimized.

B. Proposed Algorithm

netlist – technology mapped version of the logic circuit
Coverage – desired coverage
Constraints – overhead; possibly area, delay, and/or power
SensitizationQ – priority queue of gates
Fault – Simulate(*netlist*);
For each gate g ϵ *netlist*
    Do Enqueue(*sensitizationQ*,g, Psensitization(g))
While coverage is not met and constraints are not violated
    Do Size-SEU-Immunity(Extra-Max*(sensitizationQ*))
        Updated-Coverage-Constraints(*netlist*)
        Dequeue(*sensitizationQ*)

Fig. 1. Radiation Harden (netlist, coverage, constraints)

The pseudocode for the proposed procedure for radiation hardening is presented in Fig. 1. The first step is to rank all the gates in the circuit in descending order of their sensitization probability using the method Fault-Simulate as follows. Since the probability of logical masking of a node depends on the probability of each input pattern being applied to the circuit, an efficient way to calculate the probability of logical masking is to simply simulate the system with a typical workload for some number of clock cycles. For each clock cycle, fault simulation can be performed on each gate to determine if it is sensitized to one or more outputs/latches/flip-flops. Nodes that are only sensitized for a very few input patterns will have a negligible effect on the overall soft error rate (since their probability of being sensitized is extremely low) and can, hence, can be ignored for radiation hardening. A less accurate alternative to simulating the system with a typical workload would be to just apply random patterns at the primary inputs.Note that the fraction of cycles where a node may assume a logic 0 value may differ significantly from the fraction of cycles when the node assumes a logic 1 value. As a direct consequence, there can be a significant difference between the logic 0 and logic 1 sensitization probabilities of a gate, especially if there is reconvergent fanout in the logic circuit. Since this paper focuses on continuous symmetricgate sizing, the logic 0 and logic 1 sensitization probabilities are collapsed (summed) when the gates are inserted into the priority queue sensitizationQ.

Gates are dequeued from sensitizationQ in decreasing order of their collapsed sensitization probability (increasing order of logical masking probability). The gate sizing routine Size- SEU-Immunity symmetrically sizes both the nMOS and the pMOS transistors in a library gate. Once the minimum size for SEU immunity is determined for a gate, the transistor sizes (both nMOS and pMOS) are updated using

$$(W/L)updated = \max\{(W/L)original . (W/L)min\}$$

Note that the scaling of the gate is done such that the ratio of the sizes of the nMOS and pMOS transistors in the original library gate remains unchanged. The gates are processed in decreasing order until the coverage objective is met or any of the constraints are violated. The routine Update-Coverage-Constraints first updates coverage, which is defined as

$$\text{Coverage (percent)} = 100\,(\Sigma(\text{candidates gc})\,Ps(gc) / \Sigma(\text{all gates g})\,Ps(g)) \quad (1)$$

In (1), Ps(•) returns the collapsed sensitization probability of a gate. Candidate gates gc are all the gates that may be sized for SEU immunity as they are dequeued from sensitizationQ. Thus, the percentage of propagated SEUs over all the cycles is reduced (in percent) by an amount that equals coverage for the worst case parameters, since the gates have been sized such that the SEUs will not propagate even if a sensitized path exists. The coverage metric is used to estimate the reduction in soft error failure rate, without computation of the exact soft error failure rate of the original and hardened circuits. Note that 90% (50%) coverage corresponds (approximately) to an order of magnitude (factor of 2) reduction in the soft error failure rate for the chosen charge range (worst case SEU parameters).

C. Coverage and Soft Error Failure Rate Reduction

In order to verify that there is a significant correlation between coverage determined using sensitization probability and soft error failure rate reduction that includes electrical and temporal masking factors, a Monte Carlo-based simulation framework similar to that described in [3] was implemented to estimate the reduction in soft error failure rate of circuits. The charge used for simulation was the worst case charge used for radiation hardening. The site for particle strikes and the input pattern were chosen randomly. Since the runtime of this SPICE-based simulator is exorbitant (over 10 hours for 100 000 patterns), experiments were run on small circuits from the MCNC benchmark suite [2] to verify this correlation.

The reduction in the soft error failure rate can be estimated as

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Reduction (percent) = 100 (1 – Σ(all gates g) Asized(g)nsized(g)/ Σ(all gates g) Aunsized(g)nunsized(g))

The coverage determined using sensitization probability of gates is a good and computationally efficient metric to estimate the reduction in the soft error failure rate in logic circuits.

D. Order of Processing
When gates are dequeued from sensitizationQ, it is possible that a gate may be sized after one or more of its fanin gates have been sized. This perturbs the soft error sensitivity of the gates in the immediate fanin of the gate, since the increase in the gate's input capacitance was not accounted for when the fanin gates were originally sized. Since the gates are processed one at a time, the procedure Radiation-Harden has to be run multiple times till the changes in gate sizes stabilize. The experiments with three passes of Radiation-Harden indicate that the impact of this effect on the overall performance of the algorithm is negligible. Area, delay, and power overhead change by less than 3% on average across all the benchmarks and process technologies. There are two reasons for this observed behavior.

1) First, the sensitization probability of a fanout gate usually exceeds that of its fanin gates. As a result, the number of cases where the fanin is processed before the fanout is less than 44.1% of the gates that are sized on average.
2) Second, fanin gates usually have a high sensitization probability only if they have significant fanout . However, such gates are driven by gates with higher drive strength from the technology library. Such gates are relatively more immune to SEUs. This mitigates the perturbation effect of sizing them before their fanout. When such high drive strength gates are excluded, the experiments indicate that less than 12.3% of the gates that are sized (6.8% of total gates) fall into this category.

E. Design Constraints
Sizing the transistors in a gate affects the three major design constraints: 1) area; 2) power consumption; and 3) delay, which can be integrated into the method Update-Coverage- Constraints. Since the constraints are updated after each gate is sized, the algorithm terminates as soon as one of the constraints is violated. Area information is obtained from physical layout of the standard cell library. Area changes in discrete steps as (W/L)min increases. This is because in most standard cell libraries, gates of drive strength 1 and 2, 3 and 4, etc. usually have the same cell area. Power changes continuously as the gate is sized. However, switching activity at each of the gates can be obtained during Fault-Simulate and can be used to estimate the increase in power after each gate is sized using a simple load model. If either area or power constraints are violated and Radiation-Harden terminates, the reduction in the soft error failure rate will be maximized since the gates were processed in descending order of their collapsed sensitization probability.

Delay is the most difficult constraint to handle, since sizing changes not only the drive strength of a gate, but also the input and output capacitances. The effects of sizing a gate are thus not localized from a delay perspective, since all the gates in the transitive fanin and transitive fanout are impacted by the change in capacitance. The load-dependent nature of delay means that the problem of gate sizing for delay isNP-complete. Recomputing delay after each gate is sized may be computationally expensive, so it may be done only if the gate is on a critical path. However, delay is minimally impacted by the sizing procedure proposed in this paper.

III. CHARACTERIZING INPUT PATTERNS OF LOGIC GATES

Soft error estimation and mitigation method [4] consists of three main parts: (1) vulnerability identification, (2) weighted and timing aware gate sizing, and (3) input reordering.

3.1. Vulnerability Identification
As mentioned, the most important and challenging part of a soft error mitigation technique is to find the most vulnerable gates/paths in circuits. It should be noted that in a soft error mitigation technique based on selective protection of gates, the exact SER of gates is not desired rather we need to accurately rank the gates based on their contribution in the overall circuit SER. Therefore, the factors that have very slight or similar effect on all logic gates can be neglected. As described in [7], the SER of a circuit due to SETs can be computed according to (2).

$$SER = \Sigma SER(Gi) \quad (2)$$

The SER of gate Gi, i.e., SER(Gi), can be computed according to (3).

$$SER(Gi) = PGP(Gi) \times EPP(Gi) \times LP \quad (3)$$

In this equation, PGP(Gi) is the Pulse Generation Probability (PGP) at the output of gate Gi due to a particle strike to the transistors of the gate Gi. EPP(Gi) is the propagation probability of transient pulses from the output of gate Gi to at least one of the circuit sequential elements, and LP is the latching probability of a transient pulse in the sequential elements. As described in [6], due to low logic depth and hence high operational frequency in today's digital circuits, the effect of latching-window masking on the overall SER of the circuit has significantly decreased. On the other hand, the latching-window masking effect highly depends on the pulse width and the clock period. This means that the location of a particle strike does not considerably affect the circuit LP [1]. Thus, the latching probability of a transient pulse with a specific width is almost the same for all gates. However, if we intend to accurately measure the SER, this assumption would be a source of a negligible inaccuracy, but this

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inaccuracy would not affect the outcome of our ranking. The other factors, i.e., the pulse generation probability and error propagation probability play an important role in the SER of logic gates and their corresponding SER rankings. Following we will explain how we estimate these two factors.

3.1.1. Probability of transient pulse generation

The pulse generation probability of gate Gi is computed according to (4), where n is the number of gate's inputs.

$$PGP(Gi) = \Sigma\ PGPv(Gi) \times Pv \quad (4)$$

In (4), PGPv (Gi) is the pulse generation probability at the output of gate Gi when its input value is equal to v ($0 <= v < 2^n$). In this equation, Pv is the probability that the input value of gate Gi is equal to v. Using this equation, the effect of input values on the probability of pulse generation at the output of the gate is accurately considered. The probability of pulse generation at the output of gate Gi can be calculated by (5), where m is the number of transistors in gate Gi.

$$PGPv(Gi) = \Sigma\ Ad(Tf) \times F \times K \times e\text{^}(Qcrit(v)(Tf)/Qs) \quad (5)$$

In (5), Ad(Tf) is the drain area of transistor Tf ; F is the neutron flux, K is a constant, independent to the supply voltage and doping profiles, QCrit(v)(Tf) is the critical charge of transistor Tf when the input value of gate Gi is v, and Qs is the charge collection slope which strongly depends on the supply voltage and doping. The parameters F and K are common for all transistors of a circuit. The critical charge of a transistor in a logic gate depends on the state of the transistor and its position in the gate. Thus, to extract the critical charge of a transistor in a gate, it is necessary to take into account the effect of all possible input values of the gate. The critical charge of a gate's transistor highly depends on the value of the gate's inputs. This will result in different vulnerability for the gate.

Based on (4) and considering different values of PGPv for different values of v, it is obvious that the probability of transient pulse generation (PGP) strongly depends on the probability of input values (Pv). A straightforward way to consider the effect of input patterns when estimating the SER of a circuit is to assume that the probability that a line holds logical value of ''1'' or ''0'' is 0.5, i.e., the signal probability of a line in the circuit is assumed to be 0.5. To investigate the validity of this assumption, we have carried out a set of simulations for all ISCAS'89 benchmark circuits. For each circuit, we have performed two different experiments. In the first experiment, it is assumed that the signal probability of all circuit primary inputs are 0.5, i.e., it is assumed that input patterns have been distributed uniformly. In the second experiment, it is assumed that the signal probability of all circuit primary inputs are equal to either 0.1 or 0.9 with the same probability.

3.1.2. Error propagation probability (EPP)

Electrical and logical masking are two factors affecting the propagation of a transient pulse. However, in order to rank the gates based on their sensitivity, computing only logical masking is sufficient. This is because in nanometer technology, the effect of electrical masking has been significantly decreased due to reduced nodal capacitances and circuits supply voltages. In addition, both logical and electrical masking factors of a gate depend on the distance of the gate to the primary outputs. This means that the closer a gate to the primary outputs, the more its logical and electrical masking factors. In fact, it is uncommon that a gate has a high probability of logical masking while having low probability of electrical masking and vice versa [1]. To compute the probability of logical masking effect, we use a statistical analysis method presented in [5,9]. In this method, a set of probabilities is propagated from each gate towards primary outputs and memory elements. These probabilities are:

- P0: the probability that the node has the correct logic value of 0.
- P1: the probability that the node has the correct logic value of 1.
- Pa: the probability that the node has an erroneous value that is propagated from the error site within an even number of inversions.
- Pā: the probability that the node has an erroneous value that is propagated from the error site within an odd number of inversions.

For the output of a gate, these probabilities are computed according to the gate type and the set of probabilities related to the gate's inputs [11].

3.2. Weighted and timing aware gate sizing process

It is assumed that before protecting a circuit, the designer identifies the maximum allowable area and performance overhead. The problem statement here is how the allowable area overhead can be shared among the vulnerable gates in order to gain maximum robustness against particles strike using gate sizing approach.

After computing the sensitivity of logic gates, we determine a threshold, called sensitivity threshold, such that only the gates having higher sensitivity than the sensitivity threshold are considered for protection. The sensitivity threshold is defined as a fraction of the highest measured gate sensitivity. The allowable area overhead should be shared among gates having a sensitivity greater than the sensitivity threshold. However, it should be noted that there is always a limitation on the amount of gate upsizing. This is because of three main reasons that each one determines a restricting factor for upsizing. These three factors define a maximum level of upsizing for a gate, called Maximum allowable Upsizing Factor (MUF) as detailed in the following:

1. Upsizing a gate would increase the amount of its inputs capacitance. This would violate the allowable output capacitance of the gates in fan-in defined in the technology library. To calculate the MUF of a gate for acceptable fan-out capacitance of its fan-in gates, for each fan-in gate, it determine the maximum capacitance which can be added. Then, MUF1 is determined by tracing different upsizing

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factors starting from the area budget of the target gate using the binary search algorithm to find the proper value which does not violate the maximum determined capacitances.

2. Upsizing a gate would have a negative impact on the circuit paths delay. To determine the MUF of a gate such that the maximum acceptable delay is not violated, it need to upsize the gate for different factors and then check whether the delay restrictions have been violated or not. We also use the binary search algorithm started from the given area budget of the target gate to find the most proper value of MUF2.

3. The SER of a gate becomes saturated as the gate size increases, i.e., after a specific threshold, upsizing would not decrease the gate SER tangibly. The saturation threshold for each library gate is pre-computed by applying different upsizing factors to the library gates.

Therefore, it is probable that the available area budget that can be assigned to a gate for upsizing is greater than its MUF. In such cases, the additional area is returned to the source to be assigned to other gates.

3.3. Input reordering

It has been shown in [9] that the critical charge of a gate depends on the spatial order of its inputs, i.e., input reordering in a gate would have impact on the gate SER. In other words, an effective inputs reordering of a gate can reduce its PGP. To achieve more reduction in SER without additional overhead, we combine the proposed method with the input reordering technique proposed in [8]. Reordering gates' inputs has, however, two main challenges:

1. Input reordering can only be applied to symmetric gates, since reordering the inputs of a non-symmetric gate may change the gate functionality.

2. The effect of latching-window masking may be altered since the propagation delay of paths may be affected. This challenge appears when two different transient pulses converge together.

IV. SELECTIVE-TRANSISTOR-REDUNDANCY-BASED DESIGN

The selective redundancy technique [10] is applied to protect the transistors of a circuit that have relatively high POFi j. Sensitive transistors that have relatively high POF are identified based on fault simulation of random input patterns. Different arrangements of nMOS and pMOS transistors are proposed for each gate for various transistor protection scenarios.

Algorithm 1 highlights the steps of the proposed method. Initially, the POF [10] of circuit under test is computed by first computing the POF of each transistor. The proposed algorithm applies transistor protection until the circuit POF reaches a predefined protection threshold, or a certain area overhead constraint is met. Each time, the algorithm selects a transistor with the highest POF. The effect of a transient fault on the selected nMOS (pMOS) transistor is suppressed or reduced by duplicating and scaling the widths of a subset of transistors necessary for providing the protection. Once a transistor is protected, the POF of all transistors in the circuit is updated. Protecting a transistor in a gate gi affects the selection/hit probability of all transistors in the circuit. Therefore, after protecting a transistor in a gate, the POF of the selected transistor is reduced significantly, while the POF of the remaining transistors may increase or reduce slightly. The circuit area, POF of all transistors, and POFC are updated after each transistor protection is applied. The transistor with maximum POFi j is selected for protection in the next iteration. The process is repeated until the desired protection threshold is reached or the maximum area overhead constraint is met. The protection threshold Th takes the value between [0%, 100%] and represents the reliability of the circuit required to be achieved. Increasing Th will result in more transistors being protected and vice versa.

Algorithm 1 STR Algorithm
Require: Gate level circuit, Th or Over Head
1: Th: Required circuit reliability in %
2: Over Head: Required area overhead in %
3: POFij: Circuit POF due to fault hit at j^{th} transistor of Gate i
5:
6: Compute random pattern fault detection probability of each gate g, using fault simulator
7: For all transistors compute POFij
8: Compute **POFc**
9: TotalArea = CircuitArea + (CircuitArea x OverHead)
10: **while** ((**POFc**>=(1-Th))or(CircuitArea < TargetArea))
Do
11: Pick a transistor trans ij with the highest POFij
12: Protect trans ij
13: Update CircuitArea
14: Update POFij of transistors
15: Update **POFc**
16: **end while**

V. CONCLUSION

In the future, as designs become more complex and as the soft error failure rate of logic circuits becomes unacceptably high, there will be a need for gate-level techniques for radiation hardening. The gate sizing technique for radiation hardening presented in this paper targets soft error failure rate reduction by selectively sizing the most sensitive nodes in a logic circuit. One of the most effective approaches to mitigate these types of errors is selective hardening, i.e., hardening a subset of gates to achieve the best protected circuit for a certain amount of overheads. STR-based fault tolerance technique can be applied to achieve a given circuit reliability or

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enhance the reliability of a circuit under a given area constraint. The technique is based on estimating the POF of each transistor and iteratively protecting transistors with the highest POF until the desired objective is achieved. Transistors are protected based on duplicating and scaling a subset of transistors necessary for providing the protection.

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BIOGRAPHIES

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