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Extension of Lifetime and Efficiency of NAND Flash Memory using Coding Theory

C. Poovarasi[1], B. Priyanka[2], S. Shandiya[3], S. Lakshmi[4]

UG Student, Department of Electronics and Instrumentation, Panimalar Engineering College[1,2,3]

Assistant Professor, Department of Electronics and Instrumentation, Panimalar Engineering College[4]

Abstract: In general, as the number of program/erase cycles increases over time, number of errors also increases in NAND flash memories. Hence, these memories suffer from write/read disturbs, data retention errors, bad block accumulation. Also, reliability of MLC memory is lower due to reduced gap between adjacent threshold levels. This causes for continuous scaling down of NAND flash memories. In order to improve the unwavering quality and performance of the chip, combinations of techniques are proposed in the paper. The aim of the paper is to prevent the data from being stored in a block that is bad to reduce power consumption and to place the data in the exact location rather than being stored in an equivalent address according to the mapping table to improve the performance of the memory using coding theory(Error Correction Code).Thereby, realizing higher efficiency, reliability and support longer lifetimes of NAND flash memory.

Keywords: NAND, retention error, unwavering, threshold.

I. INTRODUCTION

Each NAND flash memory cell can withstand only limited number of program and erase cycles, beyond that the particular block will lose its tolerance. Thus, leading to the accumulation of bad blocks, which increases the bit error rate for each block of the memory. Also, once a flash cell is programmed, the injected charge is trapped on the floating gate even if the power is not applied [1]. when data are stored in a flash memory cell, an already-programmed flash cell gradually loses charge from its floating gate. It can eventually alter the stored value and cause an error, called a retention error which is most common in MLC type flash memory [2].All these becomes a problem with scalability, reliability and viability of flash memory.

To overcome all these issues and to lower power consumption, provide faster access and larger storage capacities multiple bad block managing techniques had evolved in the past.L.P.Chang recommended to implement a wear levelling algorithm to monitor and spread the number of write cycles per block. The wear levelling algorithm ensures that equal use is made of all the available write cycles for each block thus, preventing wastage of pages [3].Wang and Wong proposed a technique to combine the healthy pages of multiple bad blocks to form a smaller set of virtually healthy blocks and to utilize them [4].Liu et al proposed a static trigger wear levelling strategy which forces static data to move overall memory space according to the trigger condition so as to avoid some certain datablocks being damaged in advance [5].X. Jimenez observed that every block deterioratessignificantly at different rate. Hence, he proposed an idea to transfer the stress of deterioration from weakest pages to strong pages so as to relieve them and improve the yield of the block [6].Later, an advanced local page-level address mapping strategy was proposed by Debao Wei. It focuses on the page endurance of NAND flash memory [7].

This paper proposes a set of design technique to extend the lifetime of NAND flash memory.

1. We maintain the page status using four states namely valid, invalid, free and bad that will avoid the data from getting placed in a bad location.
2. We use Hamming error correction and detection to place the data in the exact location rather than placing it in an equivalent address which improves the performance of the memory.

II. OVERVIEW OF NAND FLASH MEMORY

NAND flash memory is a type of non-volatile storage technology that does not require power to retain data. An important goal of NAND flash development has been to reduce the cost per bit and increase maximum chip capacity. NAND has a finite number of write cycles. NAND failure is usually gradual as individual cells fail and overall performance degrades, a concept known as wear out. NAND flash handles this problem by declaring some of the blocks as bad blocks [8].Similarly, for n-bit multi-level cell (MLC) NAND flash memory, the threshold voltage of each cell can be programmed to 2n separate states. Each state corresponds to a non-overlapping threshold voltage window. Cells programmed to the same n-bit value have their threshold voltages fall into the same window, but their exact threshold voltages could be different [9].In addition, when datas are stored in a flash memory cell, an already-

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programmed flash cell gradually loses charge from its floating gate. It can eventually alter the stored value and causes an error, called a retention error which occurs unintentionally while the neighboring page is being programmed [2].

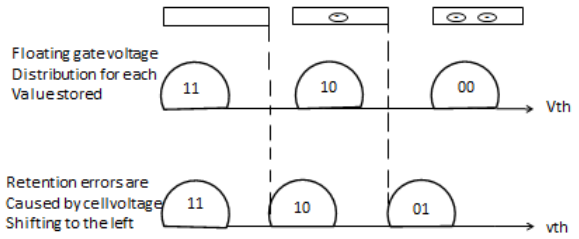

Fig. 1 Retention error model of flash memory. (a) Normal threshold voltage distribution. (b) Shifted threshold voltage distribution.

III. METHODOLOGY

Systems and Methods are provided for increasing the number of writes to a page of non-volatile memory before the pagemust be erased. Instead of writing a data word directly to memory, a codeword is written to the memory location. The codeword is selected to minimize overwrite (e.g., bit-flipping) and to maximize the spread of wear across memory cells. Error control coding (ECC) is essential for correcting soft errors in Flash memories. In such memories, as the number of erase/program cycles increases over time, the number of errors increases. NAND Flash memories suffer from write/read disturbs, data retention errors, bad block accumulation. Also, reliability of MLC memory is lower due to reduced gap between adjacent threshold levels. NAND flash memory has been used extensively in portable embedded devices, PCs, and large scale servers as the secondary storage device because of its fast access, low power consumption, large storage capacity, and resistance to shocks. To realize the high storage capacity and low cost, NAND flash memory is continuously scaling down.

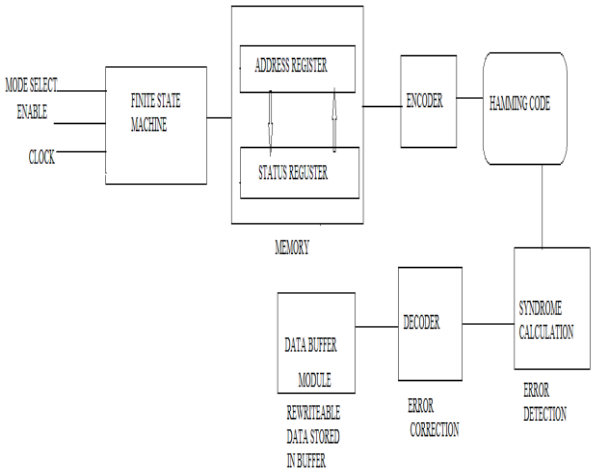

Fig. 2 Block diagram of proposed strategy.

To enhance the reliability and support longer life-times, combinations of hardware and software techniques are used. The proposed system comprises of storing data in memory using ECC and register modules. Finite state machine generates different states based on mapping model. Register stores vector in memory array using hamming code. This code generates data based on syndrome whose vector undergo for correcting and detecting errors. This process improves the lifetime as well as performance of the chip.

A. Algorithm

Herein, we have suggested algorithms that illustrate the process of performing read, write operations in the proposed strategy.

Algorithm 1 Write operation

Input: A logical sector number (lsn#A), lsn page content.
Output: Write the content to the physical page.

1. **For** each write request **do**
2. Check the mapping table in RAM and NANDflash.
3. **If**lsn#A exists in mapping table then,
4. Obtain psn pw1according to the table.
5. **If**the pw1 status is free then,
6. Write the page content to pw1.
7. Goto step 13
8. **Else**
9. Find a free page pw2 or pw3,…..according to the psn table.
10. Write the page content to the found location.
11. Goto step 13
12. **End if**
13. Check**if**lsn=psn(Hamming code) then,
14. Write the page content to lsn
15. Mark lsn status as valid and update the table.
16. **Else**
17. Perform ECC and correct the error.
18. Write the content to corrected location.
19. Mark the status of the location as valid and update.
20. **End if**
21. **Else**
22. Declare invalid.
23. **End if**
24. **End for**

The proposed strategy issues read operation after the file system initiate the read request. Algorithm 2 describes the process of read operation.

Algorithm 2 Read operation

Input:A logical sector number (lsn#A).
Output: Read the content from the physical page.
1. for each read request **do**
2. check the mapping tablein RAM and NAND flash.

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3. Obtain the psnpr (mapping to lsn#A) according to the mapping table.
4. Read the page content from the pr.
5. Operate the BCH error correction process and obtain the BER of read page.
6. Ifthe BER exceeds the error correction capability of BCH then,
7. Mark the psn status as "bad".
8. Else
9. Read operation.
10. End if
11. End for.

IV. RESULT AND ANALYSIS

To evaluate the efficiency and performance of NAND flash memory using proposed strategy, we used CPLD (Complex Programmable Logic device) as our hardware experimental platform and XILINX as software platform for programming CPLD kit.

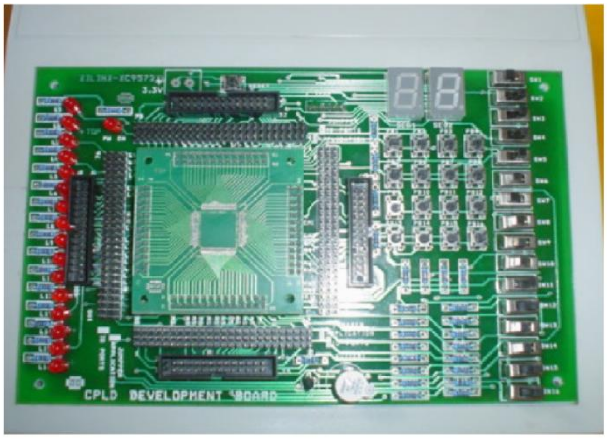

Fig. 3 CPLD kit: Hardware platform.

We connected our hardware platform on to the host computer using USB interface and examined successfully the power, area and delay parameters of the proposed strategy with the existing method.

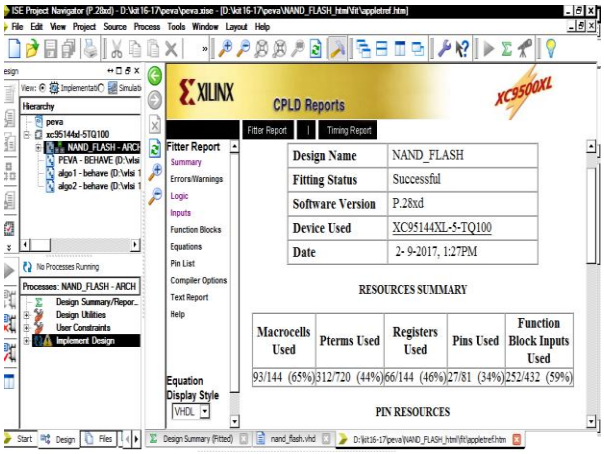

Fig. 4 Evaluation of power consumption and area used using existing system in NAND flash memory.

In the Figure, the power is represented as macrocells used and it is 65% and area is denoted as function blocks used which is 59%. Whereas in analysing the proposed system, we could find that the percentage of power and area had been reduced.

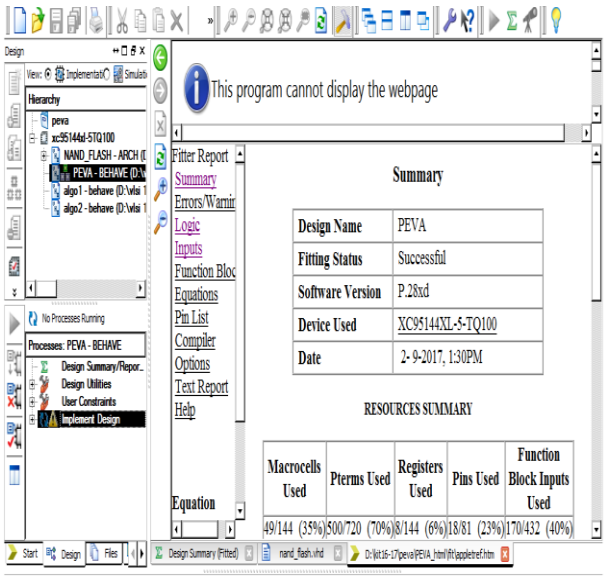

Fig. 5 Evaluation of power consumption and area used in proposed strategy in NAND flash memory.

From the above figure, the power is examined as 35% and the area as 40% which is much smaller than the existing method.Based on the experimental data from the analysis, We find that the power,area had been reduced and efficiency, performance had been improved.

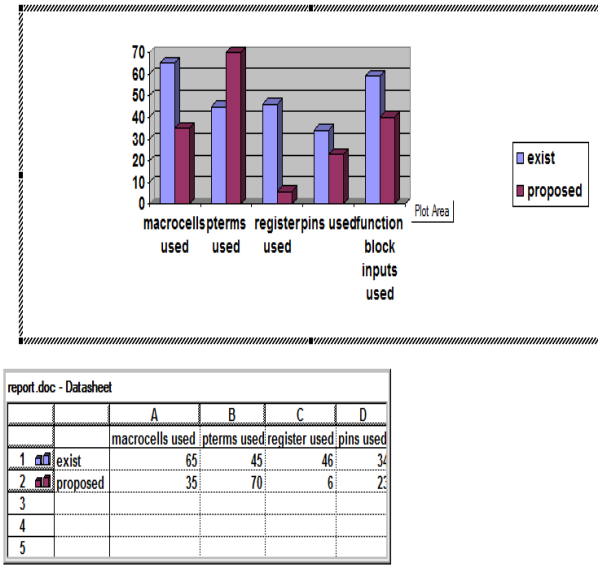

Fig. 6 Shows an example of a graph that illustrates the comparison between existing and proposed strategy.

To illustrate the progress of the proposed system, we also use MODELSIM as our software platform and read-write operation is being tested.

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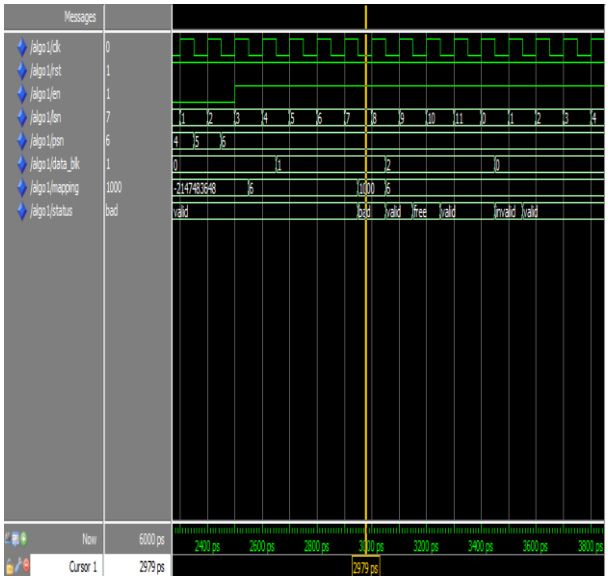

Fig. 7 Read operation performed in Modelsim software.

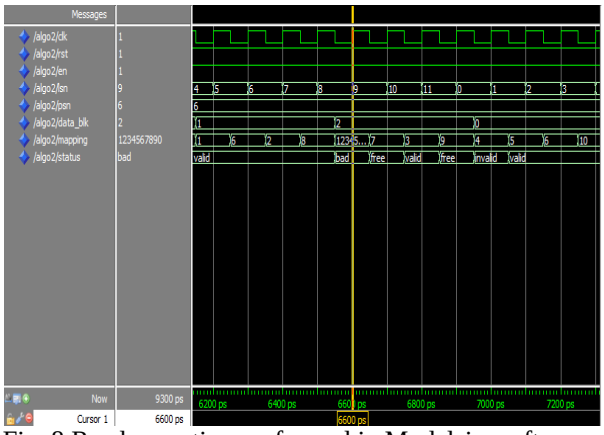

Fig. 8 Read operation performed in Modelsim software.

Thus, the performance and efficiency of NAND flash memory has been analysed and verified using set of system and methods.

V. CONCLUSION

In this paper, new strategy is being proposed to improve the lifetime of NAND flash memory. The main aim of the paper is to exploit the lifetime potency of each page in a block so as to increase the efficiency and performance of flash memory.

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