ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

IJARCCE

International Journal of Advanced Research in Computer and Communication Engineering

NCRICT-2017

Ahalia School of Engineering and Technology

Vol. 6, Special Issue 4, March 2017

A Novel Approach of improving the Performance Enhancement of in As /Si Tunnel FET

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Abstract: The designed In As/ si hetrojunction double gate tunnel FET (H-DGTFET) is a type of tunnel FET which only gives a moderate performance enhancement in MOSFET technology. Through this project we can improve the performance enhancement of In As/Si. For this we analyse the threshold voltage, gate dielectric, channel length. Here the threshold voltage of the device is extracted by using a constant current method. DC characteristics and analog RF performance are investigated for different doping profiles. A highly doped layer is placed in the channel near the source- channel junction, and this decrease the width the depletion region ,which improves the ON-current (Ion) and the RF performance further more we use Tunnel FETs with a high-k gate dielectric which have a smaller threshold voltage shift than those using Sio2,while the threshold slope for fixed values of Vg remains nearly unchanged .here three types of tunnel fets are simulated. homogeneous structure ,heterogeneous structure and pnpn model of tunnelfet are the main three structures. Comparing these structure different doping will give much more current and high performance characteristics. Through this a new novel model of tunnel fet structure has been simulated.

Keywords: homogeneous structure, heterogeneous structure, pnpn tunnel fet model.

I. INTRODUCTION

As we know that CMOS technology is growing day by day. For the better performance enhancement various parameters are taken and modelled . This will result the low power high frequency application transistor. Compare to MOSFET,TUNNEL FET gives the better on current and the performance characteristics of the tunnel fet is much higher.

Generally a good transistor for better performance should satisfies the three main conditions.

- Steepness
- On/off ratio
- Current density /conduction density

Steepness is the minimum switching that will posses a transistor. Generally the value steepness is 60mv/Dec. Decreasing this will value will result the good performance and high on/off ratio. On/off ratio will give the amount of current that is used to operate the transistor. This value also needed to be high. Generally the ratio is 10^6:1.current density is generally used for miaturizationthe old specification is 1v:1Ma.new is 1 milli-mho/micro. For the better steepness there are two methods

- Modulate the tunnelling barrier
- Density of the state switches

Modulation of the tunnelling barrier is occur by giving reverse voltage or gate voltage. But this will reduces the current density. For the better current density increase the thickness by doping this will give good steepness. If the alignment of the conduction and valence band are perfect ,the conduction rate will become high. Thus through density of the state switches the barrier become thin and the get good steepness .

Another important parameter of good transistor is the material which chosen. Here 2 different structures are considered.

- Homogeneous structure
- Heterogeneous structure

The better performance enhancement is generally depend on the barrier width ,as the width of the barrier decreases the current increases. Through heterogeneous structure the barrier width is reduced. Thus we obtain a high current from heterogeneous structure compare with homogeneous. Additional to this two gate are provided. This will result in the formation of bilayer heterogeneous strucute.through this tunnelling occur over a large overlap region rather than just at the source to drain channel region. Also

- provide highest on state conductance, Dopant diffusion

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- Dopant placement
- Implant damage
- Eliminates parasitic paths (improved electrostatic design.

In order to increase the current we need to change the doping profile, material, structure. Through
this project the current will be increased by changing doping profile.

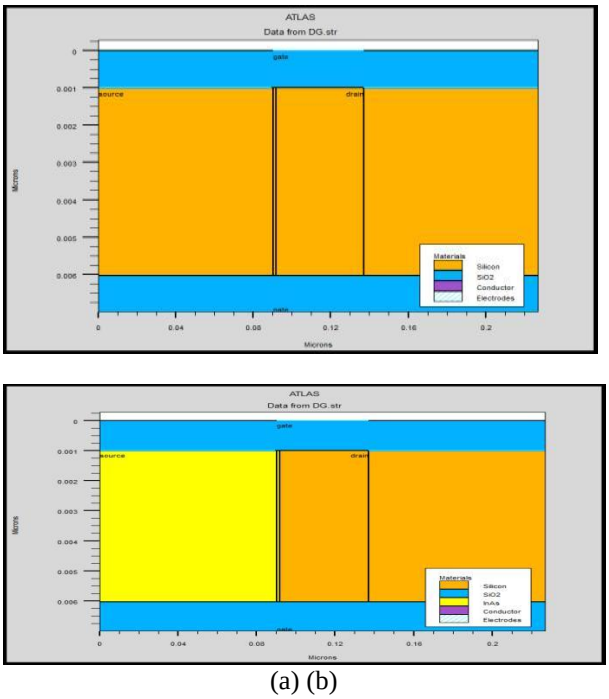
II. DESIGN AND SIMULATION SETUP

The three schematic structure of the device are shown in the figure …here the result are simulated by using TCAD SILVACO ATLAS tool. The three structure contain same base structure but different in material composition as well as doping .operation of the device is based on the intrinsic channel region which is related to the source and drain.as the structure changes the current value also changes.

A. Homogenous structure

Fig3.(a) Shows the homogeneous structure of the developed model.in which the material for source ,drain and the for channel are same. This is the simplest and quick process of developing a sample n+ layer homogeneous structure.as the gate voltage increases from 1v to 10v,the width of the barrier become decreases. Thus conduction will increases and the overall performance also increases.

B. Heterogeneous structure



(a) (b)

Fig.3(a),(b) shows the homogeneous ,heterogeneous runnel fet

III.RESULT AND DISCUSSION

The main aim of the cmos technology is making a device with low power and giving maximum current at low voltage.by using heterogeneous structure tunnel fet as shown in figure 3(b).the current will change gradually. Thus mostly we are using heterogeneous structure. Material which is using here are InAs/Si.

The source is heavily doped with 1x1e20.n type material .and the channel length is 45nm.the heavily doped reagion is composed of 2nm width of InAs n+material.and the doping concentration is 1e18.Drain and the channel uses silicon material with doping concentration of 1e17 n type and p type material aoxide thickness is 1nm and the permittivity is 1.21 with work function 4.56

This region elaborate the comparison between proposed pnpn model with the heterogeneous and the homogeneous model of tunnel fet.

As the model parameters, device structure changes the DC characteristics also changes. Here fig shows the drain current versus gate voltage of three structures. From the figure..4(a) it is clear that there is a small current increase in homogeneous structure .since the original tunnel fet will gave only less than 10nm ampere current.

From the homogeneous structure the as shown in figure 4(b) again the current increase from nm to micro ampere.in the homogeneous structure the maximum current obtained is 7x10^5 A.in heterogeneous structure 100micro A. as the size of the structure decreases the subthreshold value also decreased.After optimization with doping the maximum current achieved is 5mA

The fig4.(c) shows the optimized value of hetrojunction tunnelfet.

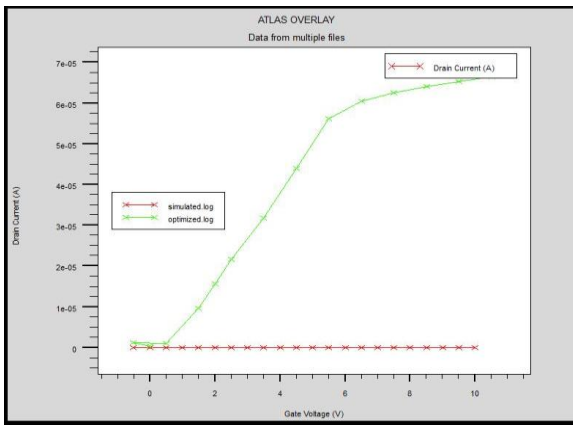


Fig.4(a) the drain current versus gate voltage graph of homogeneous tunnel fet

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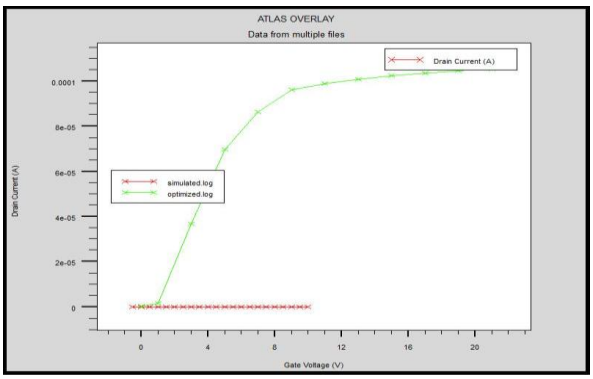

Fig.(b)the drain current versus gate voltage of hetrojunction InAs/Si tunnel fet

CONCLUSION

In this project phase ,the different structures for better current in tunnel fet are analyzed. There are considered two structure one is homostrucutre and other is hetrostructure of InAs/Si.comparing to these structure hetrojunction structure will provide much more current.By differet doping characteristics are also added. Thus the current gradually increased from 100 micro A to 5milllie A.

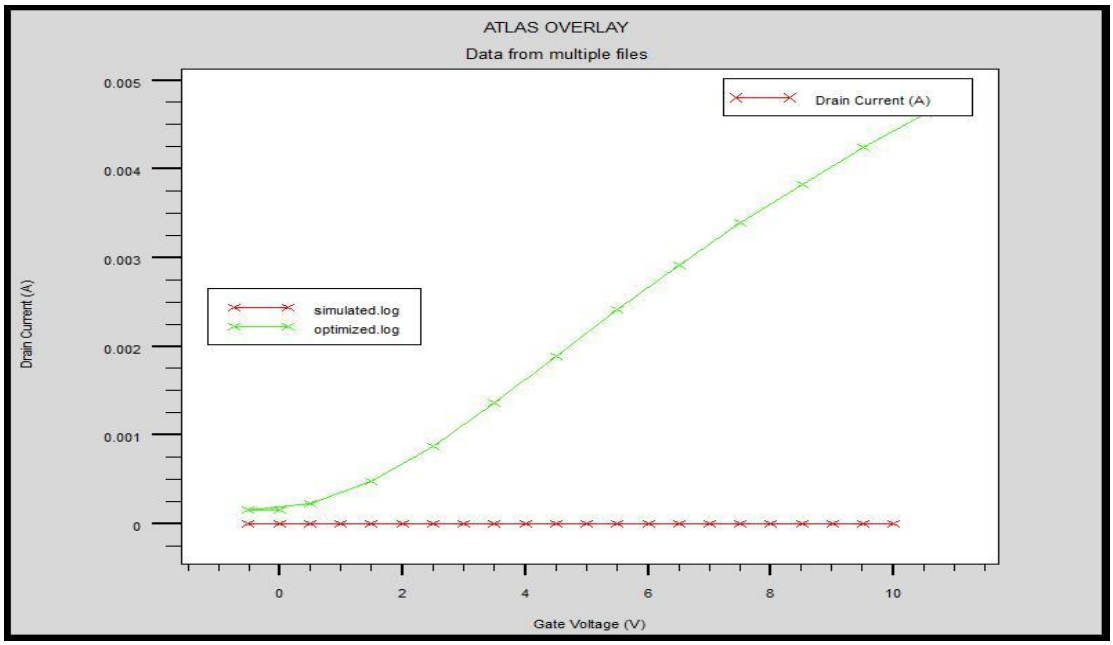

Fig.4(b)changeddoping model of InAs;Si structure drain current.

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