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Design of High Performance and Low Power Content Addressable Memory with Parity Logic and Precharge Free Techniques

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Abstract: Content-Addressable Memory (CAM) is useful for high-performance forwarding, which performs the search in a single clock cycle. In a CAM, the user supplies the content to be searched, and the CAM gives back the address location or performs association. There are several things needs to be satisfied to extract an efficient CAM from those challenges. So in this era the necessity special design is needed to satisfy the problems which are designed in the proposed system. In proposed framework, used a novel technique named as Hybrid CAM. Hybrid architecture of parity and precharge free logic which is designed with both NAND and NOR type CAM. The NOR type Match Line (ML) is always provide a parallel operation such that the data bits are proceeded into the CAM array with parallel manner. The use of NOR cell makes the drastic reduction of delay in the circuits. At the same time power is also reduced reasonably. The hybrid CAM architecture, the combination of parity logic and precharge free technique will distribute an effective energy level and high speed compared to the previous system.

Keywords: Content-Addressable Memory, Hybrid architecture, precharge free technique.

I. INTRODUCTION

In a modern era, the purpose of memory storage gets increased and speed of the memory device is gets higher / slower according to the amount of data fed into the processor. Speed of the processor will varies according to the size of the memory device. In order to reduce the power boost up the performance of a storage device a special set up is placed beneath of RAM. A unique Memory which is placed before the RAM to improve search operation of processor .The size of the device is smaller when compared to the RAM. So area wise it will not affect the RAM operation and performance. It is suitable for various applications. As it performs the contrary function of search operation, it will fetch the address/data from the memory in a single clock cycle. CAM is designed to make fast word search for larger word lengths. The 512mb size of CAM cell makes it area efficient. If it take address as input then the out performs the data. So we can fetch the binary out data when multiple character inputs are given. Existence of several types of CAM cell architecture that gives various valuable results like low power, high speed, high performance. In VLSI design process delay and power takes a vital role to produce an effective output. Delay means the number of clock cycles per bit. Moreover, the higher the speed the higher the performance. As well as the power consumption also considerable. So an efficient low power and high performance devices are the major part of memory systems. Speed takes a maximum performance in processors. Power is an efficient parameter in memory devices. When the circuit is performed in high speed is so calls high speed device. The hybrid CAM architecture (i.e.), the combination of parity logic and precharge free technique will distribute an effective energy level and high speed compared to the existing system. In existing system CAM cells are designed with 45nm CMOS technology. Using NAND type Match Line (ML) schemes CAM cells are provide high performance such as low power consumption. NAND type MLs is preferred only for CAM with small word length. But the precharge free and discharge all with on match line policy to avoid the large number of Short Circuit (SC) paths. The serial operation of data bits which is responsible for low power consumption. The amount of delay is ignored in NAND ML CAM. In proposed framework, we used Hybrid architecture of parity and precharge free logic which is designed with both NAND and NOR type CAM. The NOR type Match Line (ML) is always provide a parallel operation such that the data bits are proceeded into the CAM array with parallel manner. The use of NOR cell makes the drastic reduction of delay in the circuits. At the same time power is also reduced reasonably.

II. RELATED WORKS

There are many types of CAMs available with low power and high performance. The hybrid architecture such that the combination of parity and delay reduction technique is the recent design with better fruition. The literature survey provides an overview of various existing techniques for high speed high performance and their significance.

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Telajala Venkata Mahendra, Sandeep Mishra, and Anup Dandapat (2017), developed a precharge-free ML structure with inadequate search performance. In this brief, a self-controlled precharge-free CAM (SCPF-CAM) structure is proposed for high-speed applications. The proposed architecture is useful in applications where search time is very crucial to design larger word lengths. An SCPF-CAM structure is for high-speed applications, which exhibits the least ML delay among the compared designs. this scheme avoids the PRE phase and nullifies the dependence between CAM cells in a word due to the self-control scheme. This gives an advantage to perform more searches within a stipulated time.

Mohammed Zackriya V and Harish M. Kittur (2016), proposed a novel Content Addressable Memory (CAM) architecture with a simple but very effective precharge controller is presented. CAM is a hardware search mechanism that precharges all its match lines (MLs) during the precharge phase, and a search is performed during the evaluate phase. With unique words stored in a CAM, all the MLs except the one, which matches with the search word have to be discharged for every search cycle. The MLs that mismatch will anyway drain the charge during the evaluation phase, here, those mismatching MLs are predicted early during the precharge phase to terminate the full precharging of such lines.

Sandeep Mishra and Anup Dandapat,(2016), Ternary Content Addressable Memory (TCAM) is a hardware search engine used to speed up the searching through pre-stored contents rather than addresses. The supplementary don't care (X) state suits the TCAM for many network applications but requires large design area and consumes high power. This brief reports state of the art architecture of TCAM which reduces the search (compare) energy dissipation through the adaptive match-line controller by blocking the evaluation in the subsequent cells when a mismatch or invalid match-line data originates.

In this brief, state of the art architecture of TCAM has been presented that reduces the energy consumption by using Adaptive match-line controller. The proposed LAAM reduces the undesired comparison for invalid match-line data based on the decision function. Presented results conclude that the proposed LAAM functions at a low voltage supply of 0.6V and can reduce the macro area by 48% with comparable match-line delay metric making it suitable in high-density design requirements.

Yen-Jen Chang, and Tung-Chi Wu (2015), In this paper, they invented a new CAM word architecture, called Master–Slave Match Line (MSML) design, which aims to combine the master–slave architecture and charge refill minimization technique to reduce the CAM power dissipated in the match lines (MLs). Unlike the conventional design, where only one single ML is used, our design uses one Master-ML (MML) and several slave-MLs (SMLs) to perform the search operation. By sharing the MML charge with only them is matched SML, our design can minimize the MML charge refill swing, such that the ML power consumption can be reduced effectively.

Naoya Onizawa, Shoun Matsunaga, Vincent C. Gaudet, Warren J. Gross and Takahiro Hanyu, (2014) ,This paper introduces a reordered overlapped search mechanism for high-throughput low-energy Content-Addressable Memories (CAMs). Most mismatches can be found by searching a few bits of a search word. To lower power dissipation, a word circuit is often divided into two sections that are sequentially searched or even pipelined. Because of this process, most of match lines in the second section are unused. Since searching the last few bits is very fast compared to searching the rest of the bits, we propose to increase throughput by asynchronously initiating second-stage searches on the unused match lines as soon as a first-stage search is complete. For circuit implementation, each word circuit is independently controlled by a locally generated timing signal rather than a global signal. This allows the circuits to be in the required phase for their own local operation: evaluate or precharge, instead of having to synchronize their phase to the rest of the word circuits, which greatly reduces the cycle time.

Chua-Chin Wang, Chia-Hao Hsu, Chi-Chun Huang, and Jun-Han Wu, (2010), they developed a self-disabled sensing technique can choke the charge current fed into the ML right after the matching comparison is generated. Instead of using typical NOR/NAND-type CAM cells with the single-ended ML, the proposed novel NANDCAM cell with the differential ML design can boost the speed of comparison without sacrificing power consumption.

In addition, the 9-T CAM cell with disabled read-out circuit provides the complete write, read, and comparison functions to refresh the data and verify its correctness before searching. The choking current method to reduce the unnecessary dc currents, the power consumption is significantly reduced. Moreover, the comparison process has been accelerated by a positive loop to reduce the unwanted power dissipation. In addition, the decoupled read-out circuit has verified the data before searching, even if 6the supply voltage is reduced for the sake of power saving.

Igor Arsovski, Ali Sheikholeslami (2003), A current-saving match-line (ML) sensing scheme is proposed that substantially reduces the energy per search without compromising search speed. The proposed sensing scheme consumes only less amount of bits/search, a considerable percentage of power reduction compared to previously report sensing schemes, to achieve a search time in a array implemented in a 0.13µm CMOS process.

III. PROPOSED MEHODOLOGY

Hybrid architecture of parity and precharge free logic which is designed with both NAND and NOR type CAM. The NOR type Match Line (ML) is always provide a parallel operation such that the data bits are proceeded into the

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CAM array with parallel manner. The use of NOR cell makes the drastic reduction of delay in the circuits. At the same time power is also reduced reasonably. Here we have advantages such as, High performance attained in the means of delay. NOR type CAM cell is applied for parallel operation. Precharge free technique is proposed. Power is minimized.

Architecture

The architecture of CAM cell is shown in figure 1.4 which explains the operation of payload CAM cell. It will take a large amount of data bits and produce multiple binary outputs.

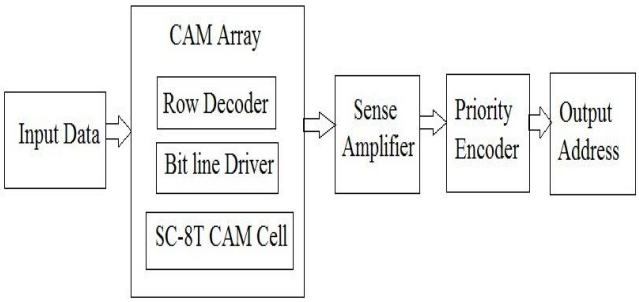

Fig 3.1 Architecture of CAM Cell.

CAM stores the data in its memory through bit line drivers. The input data driver feeds the search content to CAM, which performs the search operation. It produces the match address, if any stored data matches with the search content. A sense amplifier is used access the match information (hit/miss). Each search is performed followed by a precharge phase, a constraint to the faster search frequency.

3.1 IMPLEMENTATION PROCESSES

- Design Of Parallel CAM Cell
- Hybrid Architecture
- Search Operation
- Energy And Performance

3.2 PREQUEL DESIGN

3.2.1 Design of Parallel CAM Cell

Recently, in high-speed networks such as gigabit Ethernet and Asynchronous Transfer Mode (ATM) switch, high-speed lookup tables are necessary to satisfy the requirements of these leading-edge applications In order to achieve a powerful data searching function, the data comparison of CAM architecture is implemented in parallel operation. In the parallel comparison, all valid data stored in CAM are compared with the input data simultaneously. The parallel cells are designed by placing the NOR type CAM cells in the CAM array. These cells are processed the data bits into the array with payload operation so there is no need for waiting until the previous bit processing. A CAM array finally consists of 8T CAM cell (8 transistors) design to precede the data bits into the bit line driver and sense amplifiers. The power and delay takes major credits for an efficient memory product. So the parallel architecture of NOR cell will provide high speed operations due to this the delay drastically reduced.

3.2.2 HYBRID ARCHITECTURE

3.2.2.1 Precharge Free

Novel hybrid architecture of CAM cell is designed to produce high performance. Hybrid in the sense we are combining the parity logic and precharge free technique together to get high performance in the delay basis and low power. Initially the control bits are set to zero to avoid precharge. Then the search bits are pushed into the system. The designers preprogrammed the device for both match and mismatch conditions. If the data and control bits are matched the logic will be one. If mismatch occurs then the logic will be zero. The low logic value automatically drained to GND. So precharge free logic refers CAM precharge and evaluates all the ML for every precharge cycle during the negative and positive level, respectively, of the Pre signals. A few works are based on breaking down the complete word into segments, and the segments are arranged in a parallel, hierarchical, or butterfly manner. And some results are based on selectively precharging the MLs by precomputation. They majorly suffer from the following.

The speed of search operation is limited by the precharge cycle. NOR-type ML experiences SC current during the precharge phase. NAND-type ML experiences charge sharing problem.

The proposed CAM architecture that is free of all the above shortcomings, which are present in the existing CAMs. In the proposed CAM, 8-T CAM cells from the basic building block. This is different to the NAND-type ML in the existing system. The parallel NOR type (ML) cell is designed. Now the bits are entered into the circuit, If the search bit

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matches the stored bit, then ML will get charge from BL .If it do not matches with the stored bit it will automatically drained to zero.

5.2.2.2 Parity Logic

Parity logics are often works in the memory systems. For content addressable memories the parity logic is applied to reduce the power consumption. For next bit the match line need not to be precharge because it is a precharge free technique. Parity check in the sense we are reducing the amount of switching for unnecessary low logic (zero) signals. An XOR circuit is placed closed to the proposed NOR type parallel CAM cell to check how many ones and zeros are functioned into the circuits. It has the knowledge to give the switching power for high level signals which produce logic '1' as output. So the parity of even ones and odd zeros are produced by the XOR circuit. Parity checking is done on number if search bits simultaneously because for 4x4 array the control and data bits are low in amount. So we are increasing the signal iteration to get an efficient product. The flow chart of parity check in CAM shown below,

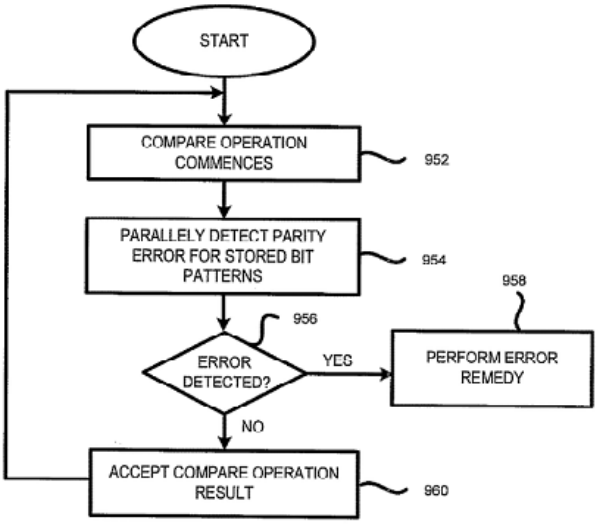

Figure 3.2 Flow Chart For Parity Checking

3.3 SEARCH OPERATION

3.3.1 Row Decoder

The search operations are classified into two ways such as read operation and write operation. During read cycle the input data are fed into the row decoder. It depends on the type of memory, some just use the intersection of the selected row and selected column. Some read a whole row or column into an internal buffer then select the individual item in the row with the other selector. , it is the fact that only one bit from one row and one column is accessed. If the memory is more than one bit wide, for example an 8-bit memory, there are effectively 8 identical 'planes' of memory cells, each having the same number of rows and columns and each selected simultaneously when addressed. One bit is written to or read from each plane giving the appearance of the data being 8-bits wide.

3.3.2 Bit Line Drivers

Bit-lines are "metallic" stripes perpendicular to the word lines and are physically connected to the source/drains of the cell-transistors. In other words, the bit-lines are the lines through which information is written/read to/from the memory cells. Information is read from the cell, or written into the cell by the so called sense-amplifiers - each bit-line is connected to a sense-amplifier. As with word line-drivers, the sense-amplifiers cannot be made too big, i.e. to be high performing, due to place limitations on the chip. However they should be good enough in order to read and write the information into the cells correctly.

3.3.3 Sense Amplifier

In modern computer memory, a sense amplifier is one of the elements which make up the circuitry on a semiconductor memory chip (integrated circuit); the term itself dates back to the era of magnetic core memory. A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bit line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

Modern sense-amplifier circuits consist of two to six (usually four) transistors, while early sense amplifiers for core memory sometimes contained as many as 13 transistors. There is one sense amplifier for each column of memory cells, so there are usually hundreds or thousands of identical sense amplifiers on a modern memory chip. As such, sense amplifiers are one of the only analog circuits in a computer's memory subsystem.

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3.3.4 Priority Encoder

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority encoder.

5.4 ENERGY AND PERFORMANCE

Power and delay both are dependent parameter. For high speed one system takes high potential to operate at maximum speed. If low power is applied the system will slow. But through an effective design of hybrid CAM structure of precharge free and parity logic one can attain minimized power and geared up performance. NOR type CAM cell is modified by adding an XOR circuits leads to low power consumption with the high speed unlike a conventional CAM architecture. The delay is enormously reduced compared with the existing technique by using the parallel architecture. Here delay is calculated how much time the signal will take to settle. So ain the equation number 1, the settling time can be defined as the time taken by the signal from low (0) to high level (1) logic.

$$settling\ time = \frac{signal\ speed}{time\ perid} \qquad \text{---------->1}$$

$$s_t = \frac{s}{t} \qquad \text{---------->2}$$

Speed and power Performance are improved in the parallel CAM architecture. The precharge free logic which deserves low power feature since it protects the CAM array from an additional power supply.

IV. RESULT AND DISCUSSION

4.1 THROUGHPUT

Throughput can be defined as how many number of data bits are transferred per clock cycle.

$$Throughput = \frac{number\ \ of\ bits\ transferred}{clock\ \ cycle}$$

Circuit diagram of 8TCAM cell

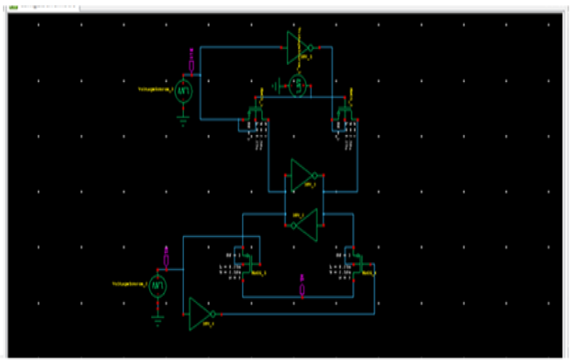

Figure 4.1 An 8T CAM Cell

The output of a single 8T cam cell describes the match and mismatch condition for both low and high level logic. If signals are matched the output will be '1' so the wave will rise to high level. If signals are not matched there will be a falling output. For high level logic the signal rised to one.

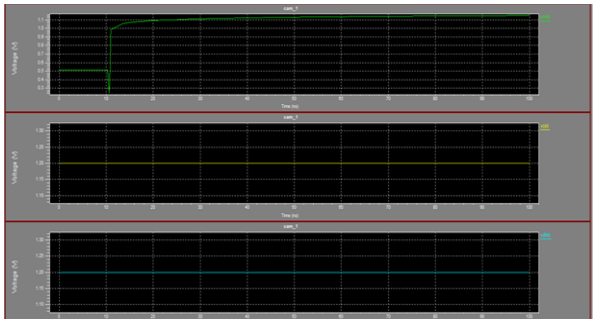

Figure 4.2 High Logic For Match Condition

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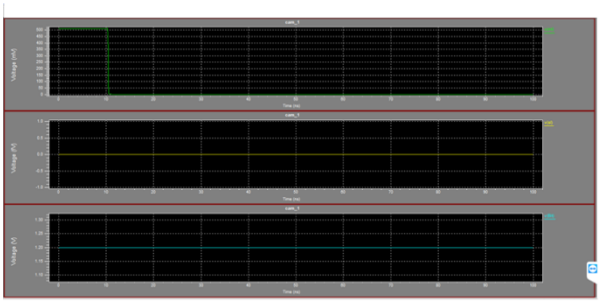

Figure 4.3 Low Logic For Mismatched Condition.

4.2 COMAPRISON WITH EXISTING SYSTEM

4.2.1 EXIXTING SYSTEM

The existing serial design of CAM cell has more delay and it takes more time to settle.

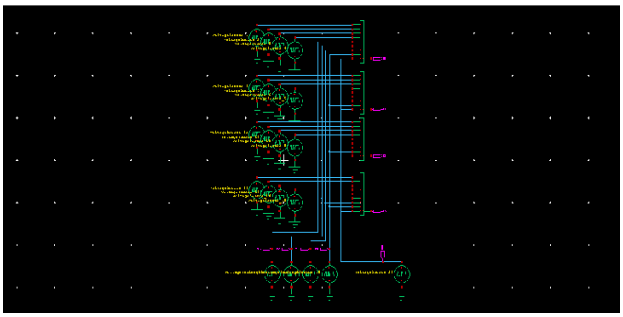

Figure 4.4 Existing Serial Design

The below output wave describes how much time taken by the circuit to reach from logic '0'to logic '1'. The figure will show around 10-60ns taken by the signal to settle.

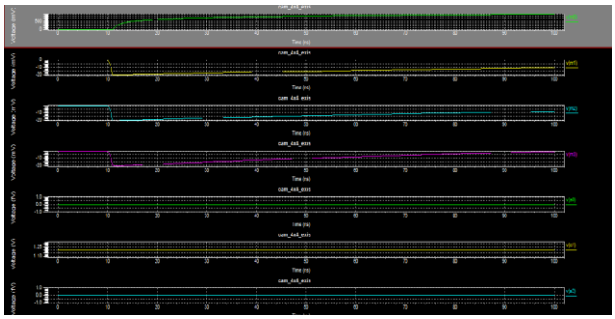

Figure 4.5 Larger Delays In Existing System

4.2.2 PERFORMANCE ANALYSIS

Proposed parallel architecture of CAM cell shown below,

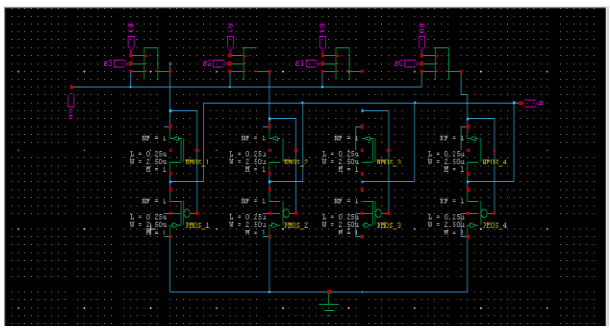

Figure 4.6 Proposed Parallel CAM Design.

The proposed CAM cell is modified with the adding of XOR circuit power consumption.

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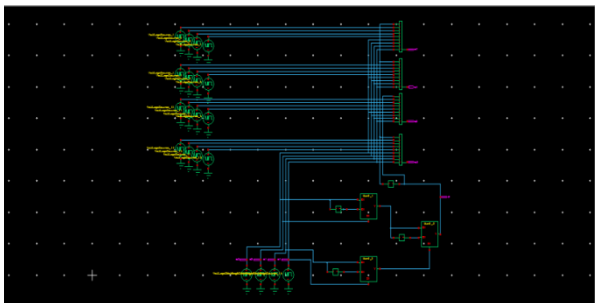

Figure 4.7 Proposed Design With Modification.

The output waveform of proposed system describes that the delay is reduced,

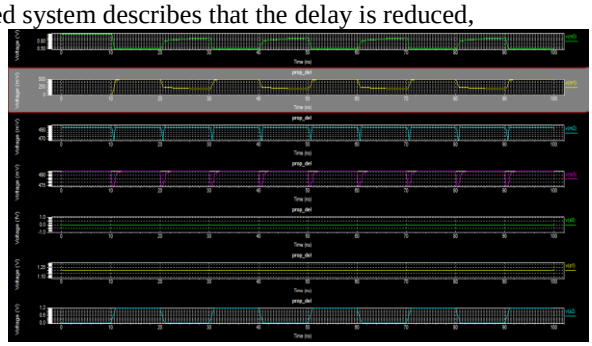

Figure 4.8 Settling Time for proposed Signal.

The following figure shows the modified CAM cell deign with reduced delay,

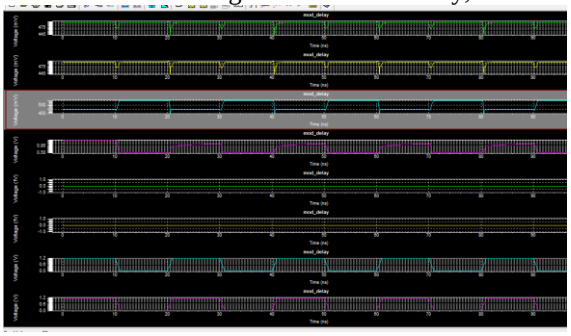

Figure 4.9 Modified CAM With Delay Reduction.

4.3 POWER ANALYSIS

The average power of CAM varies according to the technique used. The average Power consumption for existing system is shown below,

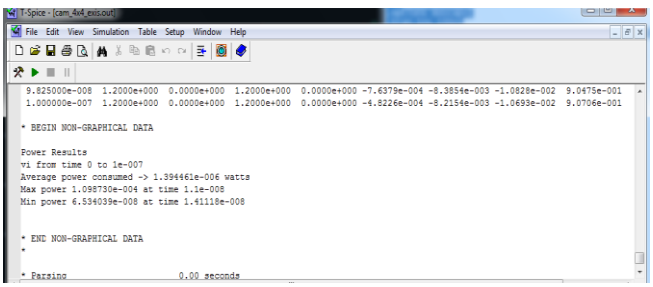

Figure 4.10 Average Power for Existing System

The average power for existing system shown below,

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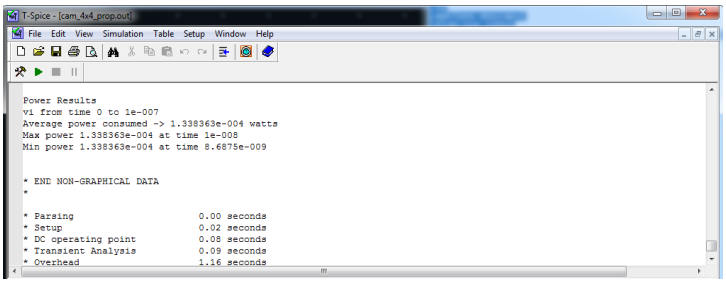

Figure 4.11 Average Power For Existing System.

Modified CAM which consumes less average power compared with existing system.

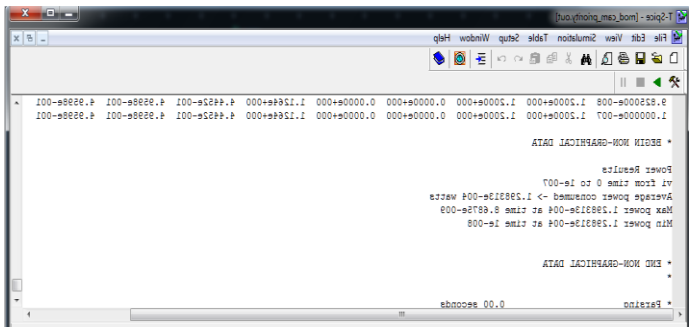

Figure 4.12 Modified CAM Power Consumption.

6.4 PERFORMANCE COMPARISON

The following table evaluates the average power consumption of content addressable memory for various techniques. This table explains the average power reduced in modified design in a reasonable amount.

Serial number	CAM designs	Average power consumption
1	Serial design with single cell match line	1.39 watts
2	Proposed parallel design	1.33 watts
3	Modified CAM design with hybrid design.	1.29 watts

Table 4.1 Power Comparison

Based on the results the table shows that power reduced for proposed design.

Serial number	CAM designs	Time taken to settle
1	Serial design with single cell match line	10-60ns
2	Proposed parallel design	10-20ns
3	Modified CAM design with hybrid design.	1-2ns

Table 4.2 Delay Comparison

Based on the table the results show the amount of delay is reduced.

V. CONCLUSION

Thus the parallel hybrid architecture of content addressable memory is performed based on the CAM cell design to get high performance and low power. The NOR type CAM cells are responsible for high speed operations and maximize delay reduction. Modified design with parity check and recharger free logic which produce an efficient amount of minimized power. For future work, this design will be extended to provide area reduction, improved storage space. The CMOS design process can be modified to the latest technology to minimize the size if the product. In addition to that the match line schemes further redesigned to extract an efficient content addressable memory.

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