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# Power Distribution in Portable Two-Way Radio Design Efficiency Improvement

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**ABSTRACT**: **In the 2-way radios market, long battery life has becomes an essential & critical customer requirement for communications during critical public safety or rescue missions. Thus in tandem with this need, various researches have been conducted by industry players to reduce the current consumption of the design with minimum sacrifices on product performance. This paper attempts to describe various key strategies that can be adopted in the design of portable two ways radio design in optimizing the efficiency of the power distribution network in the radio and design guidelines on selection and implementation of switching regulator in radio to reduce the overall current drain consumption.**

**Keywords**: **Battery life, current drain reduction, efficiency, switching regulator**

## I. INTRODUCTION

### *A. Customer Requirement & Literatures Reviews*

Longer battery life has become an essential requirement to the customer during critical mission operations. For example, fireman on duty in a critical rescue mission (forest fire) may require substantially more than 8 hours of operation adhering to the 5 % (Transmit) – 5 % (Receiving)- 90 % (Idle) cycles [4], [6], [12]. Carrying additional battery packs may be a quick solution, however it becomes so impractical to carry so many of them along during critical mission. Increasing the capacity of the battery packs might be another alternative to solve this dilemma but with trade-offs in additional product mechanical dimensions, additional weight and increase in the overall product development cost. In tandem with this need, various researches have been conducted by industry players to reduce the current consumption of the design with minimum sacrifices on product performances.

In 2008, Dongsuk Lee, Hyunseok Nam, Youngkook Ahn & Jeongjin Roh presented a paper on a 1.5 MHz 300 mA buck switching regulator design using CMOS 0.18 um technology for the application of mobile devices and emphasize the importance of using switching regulator to achieve high efficiency and exceptional current driving capability [3]. Meanwhile in 2011, Jia Wang, Deyuan Gao, Ran Zheng, Hu C. & Yann Hu presented a paper on design of low drop out regulator using CMOS 0.35 um process to meet the low material and low noise requirements to internally supply the internal analog circuit [7]. In 2010, Ong G.T. & Chan P.K presented a paper on design of new micro power high power-supply-rejection (PSR) regulator without using op-amp for the application of micro power sensor circuits [15].

All of these research papers are published in the area of single stage DC to DC converters in both linear and switching topologies in which could be adopted directly into the design of mobile devices with the battery input of 3.6 V; e.g. mobile phones, a platform without a need for multi stages voltage conversion. That is the reason why hardly any paper been published with the overall design architecture of DC power distribution which requires multiple stages of voltage conversions, e.g. portable two-way radio.

The battery input to portable two way radio is commonly used at 7.5 V instead of 3.6 V. This is mainly due to the need of power amplifiers which resides in transmitter section in the portable radio to be powered by 7.5V [11].

Raising the battery input voltage to 7.5 V will inherently widen the voltage conversion gap from the battery input to the lowest regulated voltage required to power up the internal circuitries in the portable radio and posing unnecessary power conversion loss on the voltage conversion chains. Hence the motivation of this research is to propose strategies that could be employed by portable radio designer to improve the overall efficiency of the power distribution architecture of a portable radio which uses 7.5 V battery input.

This paper is organized with the general overview of the of portable two way radio architecture, radio controller architecture, DC power distribution in portable radio with the analysis of the efficiency on all the regulated supplies in the portable radio and a case study in Section I.

Key strategies in reducing the current consumptions in reference to the case study are also presented in Section II with actual efficiency characterization on LTC1877 switching regulator evaluation kit. Layout and noise considerations for switching regulator in portable radio are also discussed in Section II. Future improvement is also outlined for the existing radio power DC distribution in Section II. Finally, summary and conclusions are drawn in Section III.

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Vol. 1, Issue 9, November 2012

### *B. Overview of the General Architecture of Portable Two Way Radio*

In general, a typical portable two-two way radio consists of the following sub-sections as shown in Figure 1.0 [8][17]:-

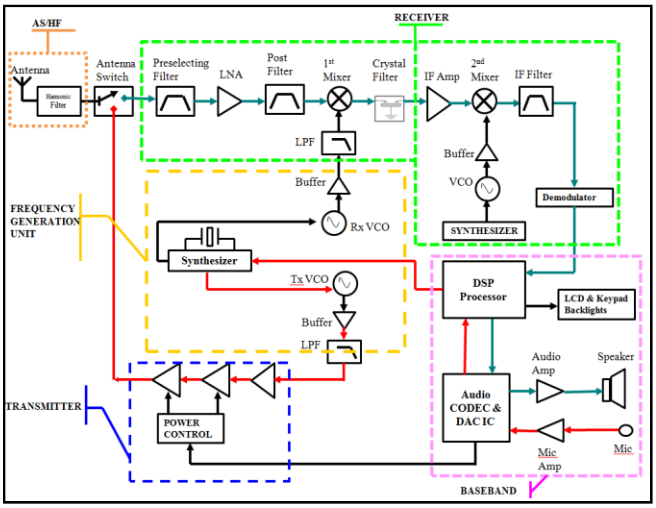

Figure 1.0: Typical radio architecture block diagram [8][17]

The baseband controller section consists of the power management, audio, processor/microcontroller & memory, LCD & keypad backlights and interface sections. The power management sub section works as the section to provide regulated power supplies to the internal radio sub sections to power up the radio and the processor/microcontroller unit works as the section for data transmission in between the baseband section with the receiver, transmitter and frequency generation unit (FGU) section.

Audio codec & amplifier section works as the section to convert the digital data from the processor to analog format and subsequently amplifying the analog signal and transmitting it to the speaker. The audio codec also takes in analog information from the mic and converting it to digital format to be processed by the processor/microcontroller. LED & Backlights section works as the section to enhance the readability of the radio LCD & keypad system in dark condition.

Whereas, frequency generation unit (FGU) section consisting of voltage controlled oscillators and phase locked loop circuits works as the section to generate a stable carrier radio frequency signal for modulation purposes. Receiver section in which consists of low noise amplifier, RF filters and mixers works as the section to down convert /mix down the received modulated signals in RF frequency to meaningful digital data before sending it over to the processor for further processing. Meanwhile, amplifier section works as the section to amplify the modulated signal (after FGU section) to desired RF output power before transmission via antenna and the power control section works as the feedback loop to control the output transmission power of the radio.

Last but not least, antenna & harmonic filter section is the section where the modulated signal gets transmitted or received by the radio.

### *C. Typical Baseband Controller Architecture in Portable Two-Way Radio*

Typical controller architecture of in the portable two-way radio is investigated. In this case, Motorola MOTOTRBO series portable radio service manual which is available in the public domain is used as a reference and case study as shown in Figure 1.1 [11].

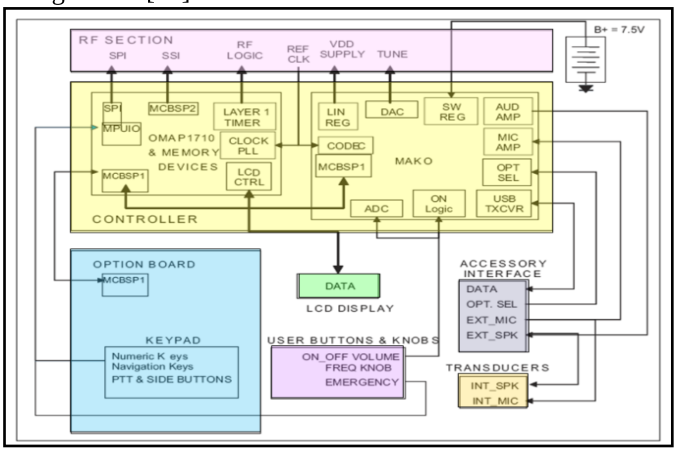

Figure 1.1: Baseband controller block diagram *[11]*

In reference to the service manual [11], the controller section consists of four main integrated circuits (IC). They are:-

1) *OMAP1710 Host/DSP Processor:*
   The processor has dual-core architectures which integrates a TMS320C55x DSP core and a high-performance ARM926EJS core. The core of OMAP is powered with 1.4 V and the periphery and I/O interfaces are powered with 1.8 V.
2) *Flash:*
   The Flash memory IC is a 64 Mbit CMOS device which is supplied with 1.8 V. The Flash memory has its 23 address lines and 16 data lines connected to the External Interface Module (EIM) of the OMAP IC through the EMIFS_ADDR (23:1) and EMIFS_DATA (15:0) busses. The Flash memory contains host firmware, DSP firmware, code plug data, and tuning values.
3) *SDRAM memories:*
   The Synchronous DRAM (SDRAM) is a 128 Mb high-speed CMOS device which is designed to operate at 1.8 V low-power memory system. The SDRAM has 13 address lines and 16 data lines connected to the EIM of OMAP IC through

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*Vol. 1, Issue 9, November 2012*

SDRAM_ADDR (12:0) and SDRAM_DATA (15:0) busses.

4) *Audio/Power Management chip (MAKO):*
The MAKO IC provides DC power distribution and audio processing (i.e. audio amplification and analog-to-digital/ digital-to-analog conversions). It consist of Switching and Linear regulators, 1 W audio amplifiers, 16-bit Voice CODEC, 11-channel 10-bit A/D Converter, 10 bit D/A Converter, support 2xUSB "OTG" transceivers, One-Wire Option Detect, and GCAI ports.

## D. Radio Power DC Distribution

In MOTOTRBO portable two-way radio, MAKO power management IC is used to provide various regulations to the internal circuitries in the radio to power up the radio as shown in Figure 1.2 [11].

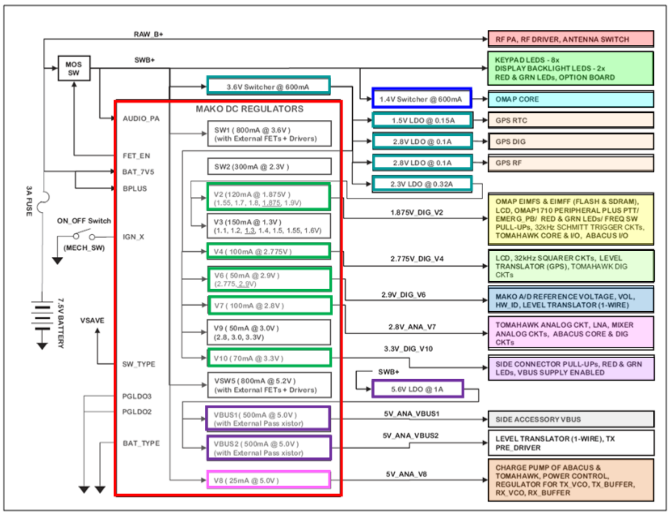


Figure 1.2: Motorola MOTOTRBO radio power DC distribution *[11]*

Voltages that were used in the MOTOTRBO radio are:-

1) 7.5 V (RAWB+ & SWB+)
2) 5.6 V (5.6 V external Low Dropout Linear Regulator @1 A load capability)
3) 5.0 V (VBUS1 & VBUS2 internal MAKO Low Dropout Liner Regulators @500 mA load capability, V8 LDO @25 mA)
4) 3.6 V (3.6 V external Switching Regulator @600 mA load capability)
5) 3.3 V (3.3 V - V10 internal MAKO LDO @70 mA load capability)
6) 2.9 V (2.9 V – V6 internal MAKO LDO @50 mA load capability)
7) 2.8 V (2.8 V external Low Dropout Linear Regulators @100 mA load capability; 2.8 V internal V7 MAKO LDO @100 mA load capability)
8) 2.775 V (2.775 V – V4 internal MAKO LDO @100 mA load capability)
9) 2.3 V (2.3 V external Dropout Linear Regulators @320 mA load capability)
10) 1.875 V (1.875 V- V2 internal MAKO LDO @120 mA load capability)
11) 1.4 V (1.4 V Switching Regulator @600 mA load capability)

## E. Efficiency Analysis of the DC Power Distributions

Various voltages from the gap of 7.5 V (battery input) down to 1.4 V were used to power up the internal circuitry of the radio. Inherently, these involve series of multiple voltage conversions in which will significantly affect the overall efficiency of the voltage delivery at the respective power line. The analysis of the efficiency of the power delivery at each regulated power lines are summarized in the Table I:-

TABLE I.

ESTIMATED CALCULATION OF THE EFFICIENCY OF POWER DELIVERY AT EVERY POWER LINES

| Power Conversion | Total Efficiency (Calculated) |
|---|---|
| 7.5V(SWB+)→5.6V (LDO)→5V (VBUS1 LDO) | 5V /7.5V =66.67% |
| 7.5V(SWB+)→5.6V (LDO)→5V (VBUS2 LDO) | 5V /7.5V =66.67% |
| 7.5V(SWB+)→ 5V (V8 LDO) | 5V /7.5V =66.67% |
| 7.5V(SWB+)→ 3.6V (Switcher) → 3.3V (LDO) | - By assuming that the efficiency of voltage conversion from 7.5V to 3.6V at 90%. Total efficiency = (90% x 91.66)/100 =82.49% |
| 7.5V(SWB+)→ 3.6V (Switcher) → 2.9V (LDO) | - By assuming that the efficiency of voltage conversion from 7.5V to 3.6V at 90%. Total efficiency = (90% x 80.55)/100 =72.49% |
| 7.5V(SWB+)→ 3.6V (Switcher) → 2.8V (LDO) | - By assuming that the efficiency of voltage conversion from 7.5V to 3.6V at 90%. Total efficiency = (90% x 77.77)/100 = 69.99% |
| 7.5V(SWB+) → 3.6V (Switcher) → 2.775V (LDO) | By assuming that the efficiency of voltage conversion from 7.5V to 3.6V at 90%. Total efficiency = (90% x 77.08)/100 = 69.37% |
| 7.5V(SWB+)→ 3.6V (Switcher) → 2.3V (LDO) →1.875V (V2 LDO) | - By assuming that the efficiency of voltage conversion from 7.5V to 3.6V at 90%. Total efficiency = (90% x 52.08)/100 =46.87% |
| 7.5V(SWB+)→ 1.4V (Switcher) | - By assuming that the efficiency of voltage conversion from 7.5V to 1.4V at 80%. |

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Vol. 1, Issue 9, November 2012

The efficiency of the voltage conversion of LDO is calculated based on the following formula;

$$Efficiency\_of\_LDO = \frac{Output\_voltage}{Inpu\_voltage} \times 100\,\% \qquad (1.0)$$

Meanwhile the efficiency of the switching regulator will depends on the load current but in reality it is feasible to get to 90 % mark easily [1, 13]. The calculated efficiency (with assumption) of the power regulation in the MOTOTRBO radio ranges from 46.87 % up to 90 %.

## II. STRATEGIES OF CURRENT CONSUMPTION REDUCTIONS IN PORTABLE TWO-WAY RADIO

The key strategies in achieving saving in current consumption at battery input of portable two-way radio are:-

(a) Minimization of the power conversion lost in the power conversion line up in the portable radio by employing high efficiency regulator (switching regulator).

(b) Utilization of single and direct voltage conversion topology.

In order to be able to gage how these strategies will help in reducing current consumptions at battery input (7.5 V), let's consider the following case study (by leveraging and make some assumptions on the design from MOTOTRBO portable two-way radio).

**Case Study:**

Let's assume that the following power delivery topology [7.5 V → 3.6 V (Switching regulator) → 2.3 V (LDO)→ 1.4 V (LDO)] is used with OMAP 1710 processor (drawing about 150 mA @1.4 V at Standby/ Idle mode).

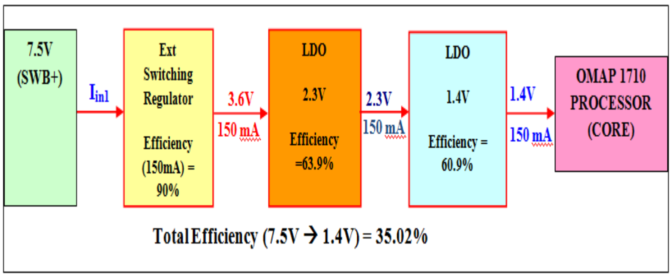


Figure 2.0: Example of three stages of power conversion topology

The calculated total efficiency from 7.5 V → 1.4 V, drops significantly to 35.02 % with three stages of power conversions.

$$I_{in1} = \frac{V_{out} \times I_{Out}}{Vin \times Efficiency} = \frac{1.4V \times 150mA}{7.5V \times 0.3502} = 79.95mA \qquad (2.0)$$

Inherently this reflects that ***79.95 mA will be seen at the battery input (7.5 V)*** at idle mode if such multiple power management topology is used. In order to reduce the current drain at the SWB+ (7.5 V), the efficiency of voltage regulation from 7.5 V to 1.4 V must be increased. This goal could be easily achieved by the implementation of high efficiency switching regulator, for eg, LTC1877 from Linear Technology which performs direct voltage conversion from 7.5 V to 1.4 V to power up the OMAP processor as illustrated in Figure 2.1.

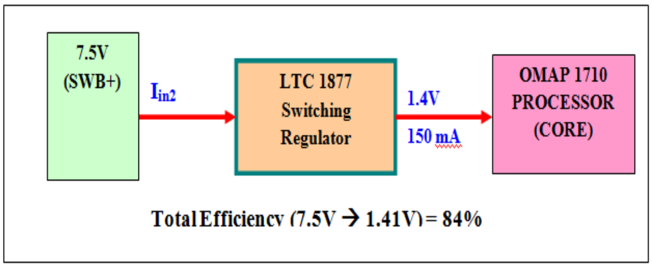


Figure 2.1: Direct single power conversion topology

With the direct voltage conversion as shown in Figure 2.1, the current drain drawn at 7.5 V (SWB+),

$$I_{in2} = \frac{V_{out} \times I_{Out}}{Vin \times Efficiency} = \frac{1.4V \times 150mA}{7.5V \times 0.84} = 33.33mA \qquad (2.1)$$

Thus, the current saving attributed by the change at 7.5V, $I_{Save1}$
$= I_{In1} - I_{In2}$
= (79.95 – 33.33) mA
= ***46.62 mA*** ***(~58 % current saving from 79.95 mA)*** (2.2)

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*International Journal of Advanced Research in Computer and Communication Engineering*
*Vol. 1, Issue 9, November 2012*

*A. Schematic & External Components Configurations for the 1.4 V Regulation to OMAP Processor*

The schematic for the step down voltage regulation from 7.5 V to 1.4 V is shown in Figure 2.2 and the LTC 1877 evaluation kit is illustrated in Figure 2.3.

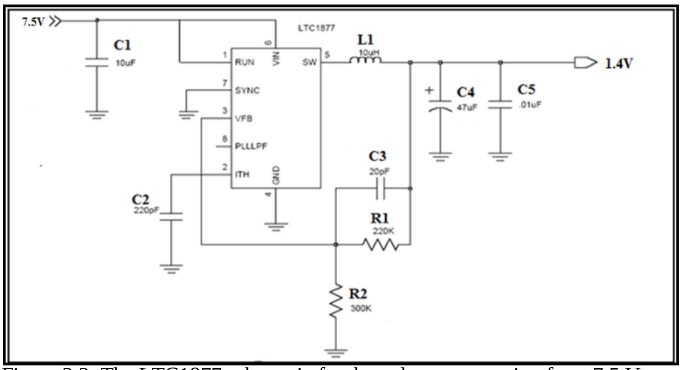


Figure 2.2: The LTC1877 schematic for the voltage conversion from 7.5 V to 1.4 V**.**


Figure 2.3: Evaluation Kit of LTC1877 switching regulator

1) *Output Voltage Programming:*

In order to get $V_{OMAP\_CORE} = 1.4V$ :

$$R1 = R2 \times \left[\frac{1.4}{0.8}\right] - R2 = 0.75R2 \qquad (2.3)$$

TABLE II.

TABLE OF VALUE FOR RESISTORS

| R1 | R2 |
|---|---|
| 220 kΩ | 300 kΩ |

2) *Inductor Value Selection:*
10 uH shielded inductor (L1) from TDK (VLF3010AT-100MR49) is selected because it is able to support the maximum rated output current of 490 mA while on the same time could be used to keep the ripple current across the inductor at the minimum acceptable level as according to following formula:

$$\begin{aligned}\Delta I_L &= \frac{1}{fL} V_{out} \left(1 - \frac{V_{Out}}{V_{In}}\right) \\ &= \frac{1.4}{(550 \times 10^3)(10 \times 10^{-6})} \left(1 - \frac{1.4}{7.2}\right) \\ &= 205mA. \end{aligned} \qquad (2.4)$$

Using a smaller inductor value may seems more feasible in this application however as far as inductor ripple current is concerned; it would be wise to choose an inductor with a higher value so that the inductor ripple current could be kept minimum [18].

3) *Input and Output Capacitors Selection:* Input capacitor (C1) of 10 uF with the voltage rating of 16 Vdc from Murata (GRM31CR71C106KA36E) is selected to prevent large voltage transient at the input [14].

Output capacitor (C2) from Sanyo POSCAP (10TPB47M) is selected at 47 uF (with ± 20 % tolerance, Vdc 10V rating & $ESR@100KHz = 70m\Omega$) so that the output voltage ripple is kept minimum [16].

$$\begin{aligned}\Delta V_{OUT} &\cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right) \\ &\cong (208 \times 10^{-3})\left(0.07 + \frac{1}{8 \times 550 \times 10^3 \times 47 \times 10^{-6}}\right) \\ &\cong 15.6mV \end{aligned} \qquad (2.5)$$

*B. Bench Measurements of the Efficiency of LTC 1877 Switching Regulator (7.5 V → 1.4 V)*

LTC 1877 switching regulator is configurable to work in two different modes known as the Pulse Skipping Mode (Mode/ Sync = GND) and Burst Mode operations (Mode/ Sync =Vin).

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*International Journal of Advanced Research in Computer and Communication Engineering*
*Vol. 1, Issue 9, November 2012*

1) *Pulse Skipping Mode (PSM Mode, Sync= GND):*
Pulse Skipping Mode is also known as the low noise mode. The advantage of Pulse Skipping (PSM) mode is lower output ripple and less interference to the audio circuitry [13]. However a slight decrease of the efficiency will be observed in this mode.

The measurements of the Vin, Vout, Iout and Efficiency of the switching regulator in PSM mode is tabulated in Table III.

TABLE III.

VIN, VOUT,IOUT AND IIN BENCH MEASUREMENT OF LTC1877 EVALUATION KIT IN PSM MODE.

**Efficiency Vs Load Current (LTC 1877) in Pulse Skipping Mode (Mode/Sync =GND) (Low noise mode)**

| Vin (V) | Vout (V) | Iout (mA) | Iin (mA) | Efficiency |
|---|---|---|---|---|
| 7.49 | 1.43 | 5.11 | 1.53 | 0.64 |
| 7.47 | 1.43 | 10.38 | 2.83 | 0.70 |
| 7.49 | 1.43 | 21.00 | 5.40 | 0.74 |
| 7.49 | 1.43 | 30.00 | 7.50 | 0.76 |
| 7.49 | 1.43 | 43.60 | 10.50 | 0.79 |
| 7.49 | 1.43 | 51.70 | 12.30 | 0.80 |
| 7.48 | 1.43 | 63.90 | 15.00 | 0.81 |
| 7.48 | 1.43 | 72.10 | 16.70 | 0.83 |
| 7.48 | 1.43 | 80.70 | 18.60 | 0.83 |
| 7.47 | 1.43 | 91.60 | 21.00 | 0.84 |
| 7.47 | 1.42 | 104.90 | 23.80 | 0.84 |
| 7.47 | 1.42 | 115.20 | 26.10 | 0.84 |
| 7.47 | 1.42 | 120.10 | 27.20 | 0.84 |
| 7.46 | 1.42 | 131.50 | 29.70 | 0.84 |
| 7.46 | 1.42 | 158.10 | 35.50 | 0.85 |
| 7.48 | 1.42 | 192.00 | 43.00 | 0.85 |

The efficiency graph of PSM mode is shown in Figure 2.4.

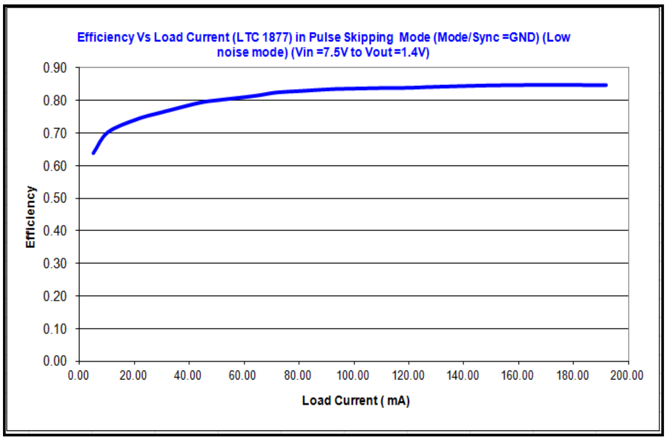


Figure 2.4: Efficiency of LTC 1877 in PSM mode(Vin =7.5 V, Vout =1.4 V)

2) BURST Mode (PSM Mode, Sync= Vin):
Operating LTC1877 in Burst mode will indeed give the maximum and higher efficiency compared to PSM mode. However operating the chip in this mode may create potential noise issue as the switching frequency of the chip may drift.

The measurements of the Vin, Vout, Iout and Efficiency of the switching regulator in BURST mode is tabulated in Table IV.

TABLE IV.

VIN, VOUT,IOUT AND IIN BENCH MEASUREMENT OF LTC1877 EVALUATION KIT IN BURSTMODE.

**Efficiency Vs Load Current (LTC 1877) in BURST Mode (Mode/Sync =Vin )**

| Vin (V) | Vout (V) | Iout (mA) | Iin (mA) | Efficiency |
|---|---|---|---|---|
| 7.49 | 1.43 | 5.10 | 1.18 | 0.83 |
| 7.48 | 1.43 | 10.17 | 2.34 | 0.83 |
| 7.50 | 1.42 | 20.40 | 4.60 | 0.84 |
| 7.49 | 1.41 | 30.00 | 6.80 | 0.83 |
| 7.49 | 1.41 | 41.00 | 9.30 | 0.83 |
| 7.49 | 1.41 | 53.00 | 11.90 | 0.84 |
| 7.48 | 1.41 | 62.80 | 14.10 | 0.84 |
| 7.48 | 1.41 | 74.30 | 16.80 | 0.83 |
| 7.48 | 1.41 | 80.80 | 18.20 | 0.84 |
| 7.47 | 1.41 | 91.30 | 20.50 | 0.84 |
| 7.47 | 1.41 | 100.30 | 22.60 | 0.84 |
| 7.47 | 1.41 | 114.90 | 25.90 | 0.84 |
| 7.46 | 1.41 | 126.20 | 28.50 | 0.84 |
| 7.46 | 1.42 | 134.40 | 30.30 | 0.84 |
| 7.46 | 1.42 | 150.50 | 33.90 | 0.85 |
| 7.48 | 1.42 | 192.00 | 43.00 | 0.85 |

The efficiency graph of BURST mode is shown in Figure 2.5.

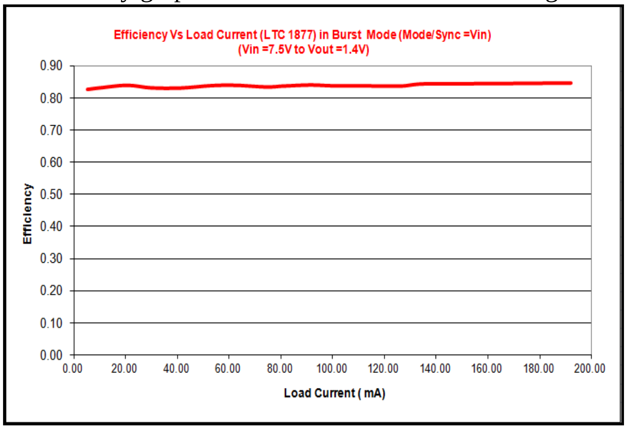


Figure 2.5: Efficiency of LTC 1877 in Burst mode (Vin =7.5 V, Vout =1.4 V)

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*Vol. 1, Issue 9, November 2012*

### *C. Layout and Noise Considerations for Switching Regulator in Portable Radio Design*

No doubt that any circuit designer will agree that switching regulators are usually noisy due to the nature of switching. However in consideration that switching regulator does help in reducing the current at battery input significantly, a compromise in design will have to be made. Various methods are employed to minimize the effects of noise from the switching regulators. Among them are:-

1) Switching regulators and its external components must be placed as far as possible from the sensitive circuitry (eg. VCO circuitry) that is sensitive to noise performance.
2) Inductor connected at the output of the switching regulator is typically the hotspot to the switching noise. The switching noise could be minimized by using the shielded inductor.
3) The power ground traces should be kept short, direct and wide.
4) At any instance, the output of the switching regulator is needed to power up a device which is sensitive to noise; a low dropout regulator (LDO with high power supply rejection ratio) can be placed in between the output of the switching regulator and the supply input to the device as shown in Figure 2.6

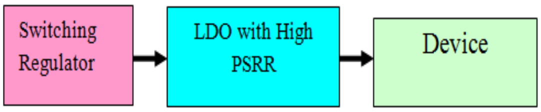


Figure 2.6: Recommended topology for noise sensitive applications.

5) Switching frequency of the switching regulators must be selected in such a way that its fundamental frequency and its harmonics will not coincide with the critical frequency used in the radio design. Selecting switching frequency at MHz range may give the advantage of smaller parts but may sacrifices the efficiency percentage.

### *D. Suggestion for Future Improvement on the MOTOTRBO Portable Radio Power DC Distribution*

In MOTOTRBO portable radio DC Distribution design, the overall calculated power regulation efficiency of the 1.875 V (V2 regulator) is about 46.87 %, which is very low and inefficient as shown in Figure 2.7.

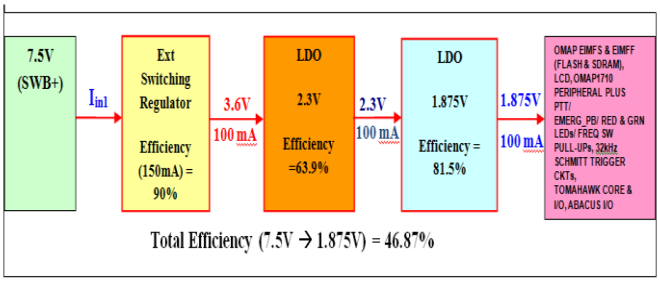


Figure 2.7: V2 Regulation topology in MOTOTRBO portable radio

The V2 regulation (1.875 V) in the MOTOTRBO portable radio power delivery line up could be further simplified and optimized by adopting the key strategies which were discussed in Section II. Thus, the recommended power conversion line up for V2 regulation is illustrated in Figure 2.8.

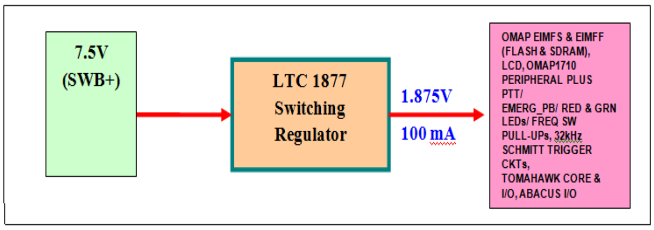


Figure 2.8: Recommended improvement on the V2 regulation in MOTOTRBO portable radio.

## III. CONCLUSION

In the portable two ways radio DC distribution design, it is crucial to keep the efficiency of the voltage regulations from the battery input to the lowest regulated voltage as high as possible so that power losses contributed by the voltage conversion stages could be kept minimum so that current saving at the battery input could be achieved; thus prolonging the battery life of the radio. This could be simply achieved by utilizing high efficiency regulators (switching regulators) to regulate the devices that are insensitive to switching noises and will potentially consume significant amount of current (e.g. processor or digital circuits). Stages of voltage conversion are best kept at maximum of two stages so that power losses attributed to voltage conversion are at minimal level. With this simple strategy in place, radio designers could offer better battery life specification to the customers without the need to increase the size of the battery capacity while keeping the development cost at bay.

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