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FPGA Synthesis of Fuzzy Based Simple Traffic Controller

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Abstract: This objective of this paper is to design, simulate, and synthesis a simple, suitable and reliable VLSI fuzzy processor for controlling the traffic lights. The performance of fuzzy techniques using Matlab are analysed and compared with FPGA one. While designing the fuzzy processor Level sensor and weighting time of the vehicles are taken as parameters. Fuzzy techniques with minimum rules such as a two input homogeneous fuzzy technique is analysed. The parallel architecture is incorporated in this design with independent functional units. These functional units process the data simultaneously by which the processing speed is enhanced. The fuzzy system with Triangular input- output, are simulated and synthesized for various values of Level sensors using VHDL. The simulated and synthesized Field programmable Gated Array (FPGA) fuzzy processor closely follows the mat lab version.

Keywords: Fuzzy Processor, VLSI, FPGA synthesis, Level sensors, Weighting Time

I. INTRODUCTION

The Fuzzy models have supplanted many conventional technologies in various scientific applications and engineering systems, especially in control systems and pattern recognition. The approach to implement fuzzy logic systems may be software only, hardware only, or a mixture of both. Suitability of an implementation approach depends mostly on the application type and performance requirements [16]. The partitioning of the solution to its software and hardware parts can be done with respect to different criteria for example, response time, reliability, price etc. The software part requires a processor, on which it will run, while the hardware part can be in the form of functions implemented as functional units and used as the standard blocks available at design time from a digital design library. In recent years, Field Programmable Gated Array (FPGA) technology has been used to implement fuzzy logic for solving real world problems, such as image processing, fuzzy database, medical diagnosis, and Industrial engineering applications.

The goal of this paper is to design, simulate, and synthesis a simple and robust VLSI fuzzy processor for efficient Traffic light control. The level sensors and weighting time of the vehicles are the input parameters.

The organization of the paper is as follows; the section I introduces the concept for Fuzzy system design. The materials and methods are explained in the section II. VLSI Design and simulation of homogeneous Fuzzy system is discussed in section III. Section IV elucidates the FPGA Implementation of Fuzzy system. Results are discussed in the section V, and the paper is concluded in section VI.

II. MATERIALS AND METHODOLOGY

The basic block diagram of the fuzzy traffic light controller is shown in Fig.1.The level sensors and weighting time of the vehicles are input to the fuzzy system, each inputs are having five linguistic variables .To manage the Traffic movement of five roads and achieve maximum utilization of five roads at the same time red green and yellow time phase should be extended or reduced based on the weighting time of vehicles and level sensor values.

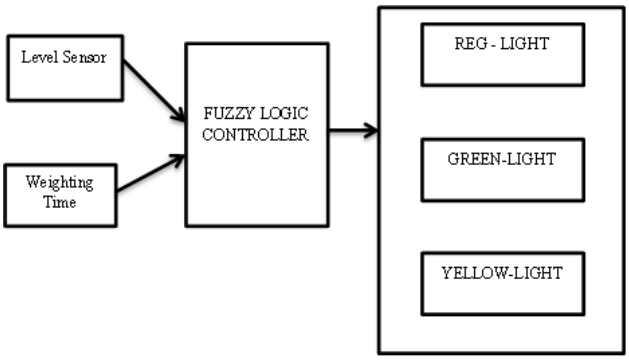

Fig.1. Functional diagram of Fuzzy Traffic light controller

A Simulation of Fuzzy Traffic Light Controller

The basic structure of fuzzy system includes four main modules such as Fuzzifier, defuzzifier, inference engine and knowledge base. The fuzzy controller controls the traffic light based on the input from level sensor and the weighting time of the vehicle. Weighting time of the vehicle is measured by using counters and it should be cleared every time during green phase and will start to

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count during Red light phase. Here we assume that wire loop embedded in the road. Electric current, run through the loop, creates the magnetic field. When a car bumper interferes with this field, a signal is sent to level sensor it control the traffic light based on the measured the signal value. The level sensor should be placed on each road. There are five level sensors used on five roads.

B Fuzzy Membership Functions

The fuzzy (*Mamdani type*) system with two inputs and one output along with the Center of Gravity (COG) Defuzzification method is selected. The weighting time input is fuzzified with five linguistic variables like *very low, low, medium, high and very high* using triangular membership functions . The other input is level sensors, with five linguistic variables xsmall, small, medium, large, verylarge. This fuzzy system performs well with the following five **Fuzzy Rules** (Fr) in the rule base such as

Fr1: *IF levelsensor is xsmall AND weighting time is very low, THEN output traffic light is red-high*

Fr2: *IF levelsensor is xsmall AND weightingtime is low, THEN output traffic light is red-medium*

Fr3: *IF levelsensor is xsmall AND weightingtime is medium, THEN output traffic light is yellow-high*

Fr4: *IF levelsensor is xsmall AND weightingtime is high, THEN output traffic light is yellow-medium*

Fr5: *IF levelsensor is xsmall AND weightingtime is very high, THEN output traffic light is Green –low*

Likewise 25 rules are created for controlling traffic light on single road. The linguistic fuzzy membership functions are illustrated in figures 2a, 2b, 2c, 2d and 2e.

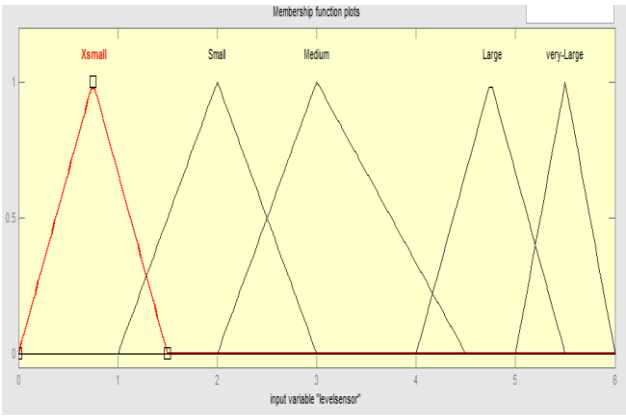

Fig. 1a. Input membership function (level sensors) of the homogeneous fuzzy system

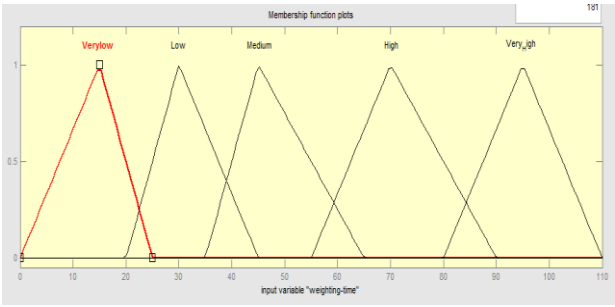

Fig. 2b. Input membership function (weighting time) of the homogeneous fuzzy system

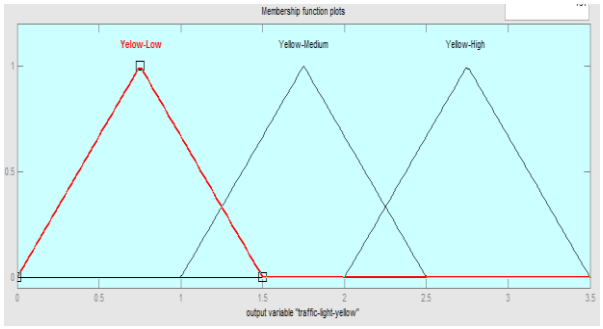

Fig. 2c. Output membership function (Yellow light) of the homogeneous fuzzy system

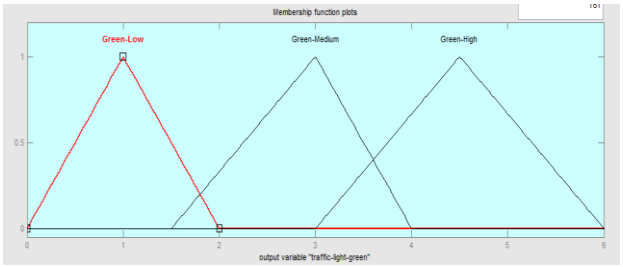

Fig. 2d. Output membership function (Green light) of the homogeneous fuzzy system

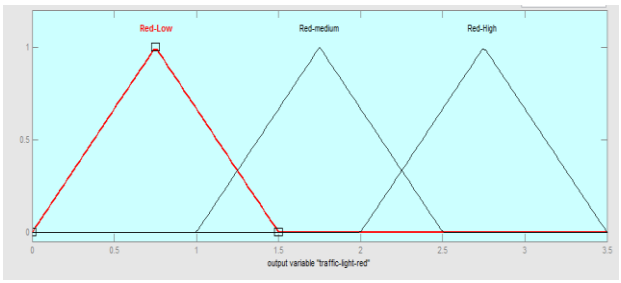

Fig. 2e. Output membership function (Red light) of the homogeneous fuzzy system

VLSI implementation of Fuzzy processor is discussed in the following section of the paper.

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III VLSI IMPLEMENTATION

In the last two decades or so, by far the strongest growth area of the semiconductor industry has been in silicon VLSI technology. The sustained growth in VLSI technology is fueled by continued shrinking of transistors to ever-small. The benefits of miniaturization, higher packing densities, higher circuits speeds and lower power dissipation have been key in the evolutionary progress leading to today's computer and communication systems that offer superior performance, dramatically reduced the cost per function and much reduced physical size in comparison with their predecessors.

A. *Architecture of Fuzzy Processor*

Figure 3, shows the Fuzzy processor's logical architecture for VLSI simulation and mentioned by Giuseppe ascia et al [19]. The internal organization includes the following blocks:

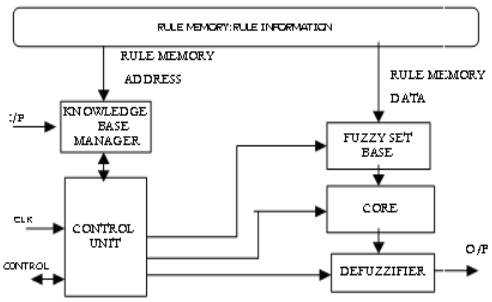

Fig **3.** Fuzzy Rule Architecture for VLSI Simulation

Fuzzy set base- A digital memory that contains the fuzzy sets related to input variables with codes stored in the rule memory. Its internal organization allows the fuzzy set base to directly supply the core with the membership degrees (alpha values) of the input variables during the computation of a premise for each rule. Likewise, during conclusion processing, the fuzzy set base supplies the relative fuzzy set.

Core- it assesses a stream of fuzzy rules in the pipeline and possesses an internal organization that allows parallel assessment of up to four antecedents per rule. The core can also store partial processing results if more than one rule involves the same inference.

Defuzzifier- This unit forms the defuzzification block and provides an output value proportional to the Maximum of fuzzy inference output.

Control unit- Coordinator of the processor's internal activities, this unit also interacts with components outside the processor through the signals mentioned earlier.

Rule memory- For passing information about a rule to the processor, this memory contains the code of the membership functions associated with each variable in fuzzy rule's premise and conclusion.

The processor communicates through the

- Input bus, through which the processor receives, input values; rule memory data, a digital bus through which the processor receives information it needs to identify the membership function in an active rule's premise and conclusion;
- A rule memory address, which stores a KBM-generated value that points to the rule memory location containing information about the active rule to be processed;
- The control bus, a set of digital lines through which it is possible to control fuzzy processor functions and supply the necessary signals for interactions outside the processor; and
- The output bus, an analog signal representing the defuzzified output value.

The VLSI design procedure of Fuzzy processor is discussed in the following section of the paper.

B VLSI Design Procedure of Fuzzy Processor

The VLSI design and simulation using Verilog HDL (Hardware Description Language) [17] is undertaken for the Homogeneous fuzzy system for the efficient traffic control in different roads on same time. This fuzzy system is modelled with input and output ports. The other necessary variables are declared as memory registers to hold the processing values. The triangular membership functions are evaluated from the functional parameters like deviation slope and centre value of level sensor is modelled. As for as the simulation result is concerned the system performs well and gives correct results in all linguistic regions of the weighting time and level sensors. Table 1 shows VHDL simulation results for the Two input Homogeneous fuzzy system. Towards the better understanding of simulation process of the homogeneous fuzzy system a sample of five Level sensors and weighting time values in the different regions are selected and analysed.

Table 1 depicts the calculation of membership function and the formation of Rule base for a given value of Level Sensors and Weighting of the vehicles. If the given Level

TABLE1.
Simulation Results for Fuzzy Processor system

LEVELSENSORS (TRIANGLE MEMBERSHIP FUNCTION)					WEIGHTING_TIME(TRIANGLE MEMBERSHIP FUNCTION)					Output TRAFIC_LIGHT		
XS	SMALL	MED	LARGE	VERY LARGE	VL	LOW	MED	HIGH	VERY HIGH	RED	YEL	GREEN
1.34	-	-	-	-	22.4	-	-	-	-	RM		
-	3.02	-	-	-	-	-	30.4	-	-		YH	
-	4.02		-	-	-	-	43.6	-	-		YL	
-	-	-	4.86	-	-	-	-	93.5	-			GM
-	-	-	-	5.26	24.6	-	-	-	-			GL

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sensors placed in the overlapping region then all the selected linguistic variable membership functions were calculated. The output traffic light is calculated by MAX defuzzification process. For example if the measured level sensors is 1.34. This falls under two linguistic variables (X small and Small) in Measured level sensor. Hence, both the membership values are calculated, finally maximum membership value is extracted by KBM generated values. Likewise, membership function values are calculated for weighting-time also. Maximum value is decided as an output traffic-light signal value for the level sensors. Finally output traffic signal is determined by rules in the rules base. To establish the best output traffic signal state in the overlapping region of the linguistic variables the above mentioned simulation is performed. This condition is simulated in XILINX and the same is depicted in the figure 4.

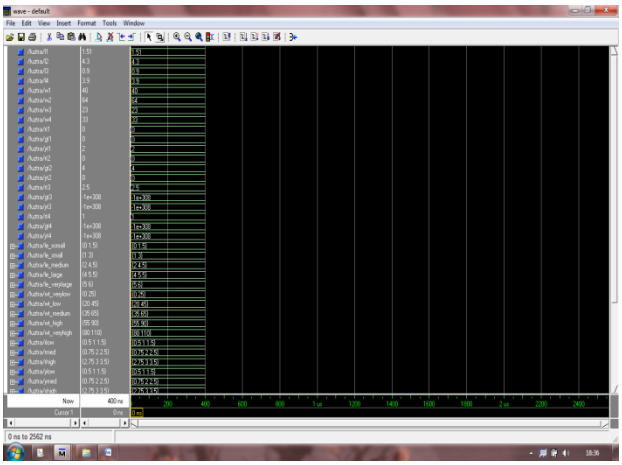

Fig.4 VHDL Simulation of Traffic condition for Fuzzy Processor

IV VHDL SYNTHESIS AND PROGRAMMING XILINX BOARD (SPARTAN 3) USING ISE

The synthesis process transforms the VHDL model into a gate –level net list. The target net list is assumed to be a technology – independent representation of the modeled logic. The target technology contains technology – independent generic blocks such as logic gates and register-transfer level (RTL) blocks, such as arithmetic-logic-units and multiplexers, comparators interconnected by wires. In such a case, a second program called RTL module builder is necessary. The purpose of this builder is to build, or acquire from a library of predefined components, each of the required RTL blocks in the user-specified target technology. Having produced a gate-level net list, a logic optimizer reads in this net list and optimizes the circuit for the user-specified area and timing constraints. These area and timing constraints may also be used by the module builder for appropriate selection or generation of RTL blocks. Different synthesis system support different VHDL subsets for synthesis. Since there is no direct object in VHDL that means a latch or a flip-flop, each synthesis system may provide different mechanism to model a flip-flop or a latch. Each synthesis system defines its own subset of VHDL language including its own personalized modeling style.

Spartan -3 family offers densities ranging from 50,000 to five million system gates. It is programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCL) that collectively control all functional elements and routing resources. Spartan-3 FPGA platform also allows the user to make significant changes while keeping original device pin outs thus eliminating the need to re-tool PC boards.

We can easily upgrade, modify, and test the designs even in the field itself. Embedded capabilities make Spartan-3 devices ideal as coprocessors or pre-and post-processors, offloading highly computational functions from a programmable DSP to enhance system performance.

A Synthesis of Fuzzy System

The synthesis part of the fuzzy system includes 3 main blocks, Triangle membership function for two inputs and Fuzzy state level comparison. Synthesis of fuzzy system shows that only less part of the resources is used for the VHDL synthesis process. The homogeneous Fuzzy system uses numerous components to synthesis the output Function. By using the RTL schematic internal components also be analysed. SIRM Triangle input and Triangle output system uses number of Flip flops, Comparator and gates for the synthesis Process. Figure 5 shows the VHDL synthesis of the Fuzzy traffic controller. The results and discussion are elucidated in the next section of the paper.

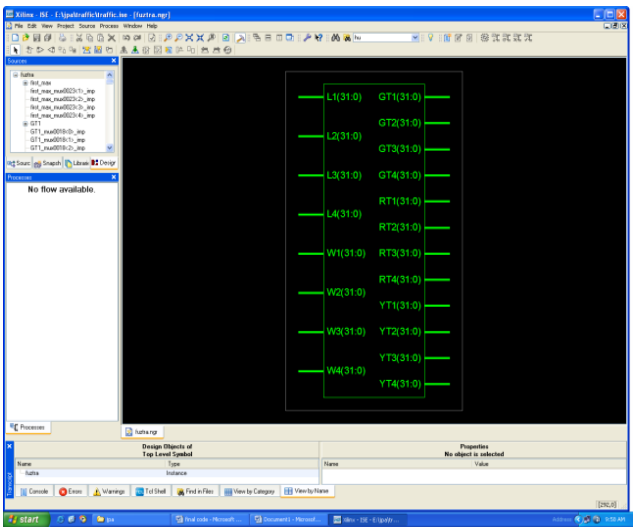

Fig.5 VHDL Synthesis of Fuzzy Processor

V. RESULTS AND DISCUSSION

Homogeneous fuzzy system operation with Triangle input membership and Triangle output function are

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analyzed by various methods Like Matlab, VLSI simulation, and FPGA synthesis. All these approaches provide different types of results. Hence a Performance comparison is needed whereby the advantages of one over the other can be easily validated and the best method found out. A Graphical representation of performance of the MATLAB modelled homogeneous Fuzzy system; VLSI simulation and FPGA synthesis are compared. From this comparison it inferred that FPGA synthesis also closely follows the existing MATLAB with higher degree of Performance. Homogeneous fuzzy system is effective for traffic light control in both during rush and normal hours when compare to the multi- input non fuzzy system which miserably fails in other convention light controls.

Several reasons to justify for the performance are

i. Higher rate of classification
ii. Lower False Level
iii. System closely follows the **MATLAB**

VI. CONCLUSION

VLSI design and synthesis of fuzzy systems such as two inputs homogeneous was under taken to control the Traffic light. For different sensor values the above systems are tested. The results show that the average performance is 98.28 and which closely follows the performance of system developed by MATLAB simulation. The VLSI simulation is done with arithmetic operations for scaled up parameter values, which is actually floating point value. Synthesis of this design is difficult because of the scaled up values. This will increase the simulation time and the processing time in synthesized hardware. Hence the system is suitable for off-line diagnosis. For on-line diagnosis, the same design can be synthesized by incorporating floating point arithmetic operations which may settled with better results. Further research is in the direction of Application Specific IC (ASIC) implementation of SIRM (Triangle input- Triangle output) fuzzy system which effectively enhance the performance in the time complex city of the system

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BIOGRAPHY

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