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Investigation of Key Parameters Affecting Current Consumption in CMOS Based Design and Processor Power Consumption Saving Features for Portable Two-Way Radio System Design

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ABSTRACT: **In the latest portable two-way radio design, processors have been widely used as the main 'heart' to control the whole operations of the radio during idle, receiving (Rx) and transmit (Tx) modes instead of Applications Specific Integrated Circuits (ASIC). By integrating processor into the design, various powerful applications could be offered to the customers but at the cost of additional power consumptions even if the radio is at idle mode. Ultimately, processors are well known to be more power hungry compared to ASIC. This will post even greater challenge for the radio designers to meet the battery life specification, in which is an essential & critical customer requirement for communications during critical public safety or rescue missions. This paper attempts to investigate the fundamental significant factors that determine the power consumptions of the CMOS based processor. HSPICE current consumption simulations with various combinations of voltage, frequency, load capacitance and temperature values are performed on a modeled CMOS buffer circuit, the simplest logic circuit available in a processor design. Design of Experiments (DOE) method was used to analyze the measured current consumptions at various combinations, determine the significant factors related to current consumptions of CMOS buffer circuit and derive the current consumption transfer function for the buffer circuit. Current consumptions saving of up to 88.30 % was found out to be feasible in CMOS based design by addressing the key significant factors identified in the earlier DOE analysis. Once all the significant factors affecting the current consumption of CMOS based design are known, various related power saving features that are offered by the processors in the market will be discussed for adoption into portable two way radio design.**

Keywords: CMOS, Current consumption, DOE, power.

I. INTRODUCTION

A. Customer Requirement & Literatures Reviews

Longer battery life has become an essential requirement to the customer during critical mission operations. For example, fireman on duty in a critical rescue mission (forest fire) may require substantially more than 8 hours of operation adhering to the 5 % (Transmit) – 5 % (Receiving)- 90 % (Idle) cycles [3], [4], [7]. Carrying additional battery packs may be a quick solution, however it becomes so impractical to carry so many of them along during critical mission. Increasing the capacity of the battery packs might be another alternative to solve this dilemma but with trade-offs in additional product mechanical dimensions, additional weight and increase in the overall product development cost. In tandem with this need, various researches have been conducted by industry players to reduce the current consumption of the design with minimum sacrifices on product performances.

Processor has been commonly used in the portable two-way radio design to control the entire operations of the portable radio in idle, receiving and transmitting modes. Ideally, processors with low power consumptions will be preferred to be integrated into portable device which operates on battery to prolong the battery life of the device. However, in reality most portable radio system designers will pick processor from off-the-shelf solutions without knowing the exact electrical parameters affecting the power consumptions of the CMOS based processor. Without this information at hand, it will be extremely difficult for system level designer to make a wise selection on processor and work on strategies to reduce power consumptions of the processor from system level perspective.

From literature review standpoint, in 2005, Zhichun Zhu & Xiadong Zhang proposed a look-ahead scheme that adjusts the processor issue rate (frequency of speed) triggered by main-memory accesses to effectively reduce processor power consumption in memory-intensive applications [11]. In 2007, Watanabe R. *at el.* proposed a power reduction method for multi-processors chip by using an analytical model to determine the optimal priority and clock frequency setting and uses the information to control the priority of shared resource accesses in cooperation with dynamic voltage frequency

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scaling (DVFS) method [10]. Meanwhile, Gert Goossens proposed a new architectural method in 2007 for multi-processor system-on-chip (SoC) by optimizing the core processor for application by managing an optimal balance of the loads (arithmetic units, task-level, and data-level and instruction-level parallelism to achieve lowest power consumptions [2]. All these above mentioned papers emphasize the optimization method related to scaling of the frequency, voltage and load parameters independently to the processors but do not discuss holistic approach to reduce power consumption at system level design perspective that includes frequency (F), voltage (V), load capacitance (Cload) and temperature (T) parameters.

The motivation of this paper is to investigate the relevancy of all these mentioned parameters based on a case study on a simple 28 nm CMOS digital buffer design and propose holistic approaches to reduce current consumption of the CMOS circuit by taking into consideration of the F-V-C-T parameters. Aside, this paper will reveal to system level designers on what to expect from the 28 nm based CMOS design in the aspect of power consumptions.

This paper is organized with the general overview of the controller architecture and processor (OMAP1710) architecture used in the off-the-shelf MOTOTRBO portable two-way radio in Section I. Key electrical parameters affecting the current consumption of the processor will be investigated based on a simple CMOS buffer design and discussed in Section II. Key current consumption saving features that are offered in the market will be discussed in Section III. Finally, summary and conclusions are drawn in Section IV.

B. *Typical Baseband Controller Architecture in Portable Two-Way Radio*

Typical controller architecture of in the portable two-way radio is investigated. In this case, Motorola MOTOTRBO series portable radio service manual which is available in the public domain is used as a reference and case study as shown in Figure 1.0 [6].

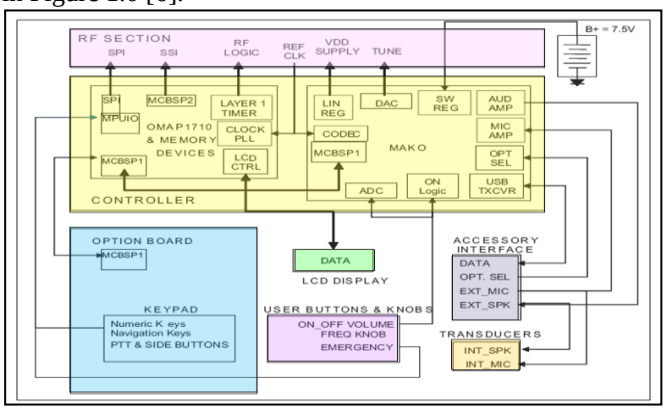

Figure 1.0: Controller Block Diagram with OMAP 1710 Processor [6]

In reference to the service manual [6], the controller section consists of four main integrated circuits (IC). They are:-

1) *OMAP1710 Host/DSP Processor:*
The processor has dual-core architectures which integrates a TMS320C55x DSP core and a high-performance ARM926EJS core. The core of OMAP is powered with 1.4 V and the periphery and I/O interfaces are powered with 1.8 V.
2) *Flash:*
The Flash memory IC is a 64 Mbit CMOS device which is supplied with 1.8 V. The Flash memory has its 23 address lines and 16 data lines connected to the External Interface Module (EIM) of the OMAP IC through the EMIFS_ADDR (23:1) and EMIFS_DATA (15:0) busses. The Flash memory contains host firmware, DSP firmware, code plug data, and tuning values.
3) *SDRAM memories:*
The Synchronous DRAM (SDRAM) is a 128 Mb high-speed CMOS device which is designed to operate at 1.8 V low-power memory system. The SDRAM has 13 address lines and 16 data lines connected to the EIM of OMAP IC through SDRAM_ADDR (12:0) and SDRAM_DATA (15:0) busses.
4) *Audio/Power Management chip (MAKO):*
The MAKO IC provides DC power distribution and audio processing (i.e. audio amplification and analog-to-digital/ digital-to-analog conversions). It consist of Switching and Linear regulators, 1 W audio amplifiers, 16-bit Voice CODEC, 11-channel 10-bit A/D Converter, 10 bit D/A Converter, support 2xUSB "OTG" transceivers, One-Wire Option Detect, and GCAI ports.

C. *OMAP1710 Processor Architecture*

The OMAP processor used in the MOTOTRBO radio is fabricated based on 90 nm technology. It comes with dual-cores architecture which incorporates a TMS320C55x DSP core and a high-performance ARM926EJS core as shown in Figure 1.1. Both cores are powered up by 1.4 V and the processing speed of the cores could be scaled up to the maximum frequency of 220 MHz. The cores utilize an instruction cache to reduce the average access time to instruction memory and eliminate power hungry external accesses. The cores also contain a memory management unit (MMU) which is utilized for virtual-to-physical memory translation task-to-task memory protection [5].

OMAP core contains two external memory interfaces and one internal memory port. The external memory interfaces support direct connection to synchronous DRAMs at up to 100 MHz and to standard asynchronous memories, such as SRAM, FLASH, or burst FLASH devices. The internal

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memory port allows direct connection to on-chip memory, such as SRAM, and can be used for frequently-accessed data, such as critical OS routines or the liquid crystal display (LCD) frame buffer. This reduces the access time and eliminates costly external accesses. All three interfaces are completely independent and allow concurrent access from either processor or direct memory access (DMA) unit [5]. The peripheral and I/O interfaces are powered with 1.8 V independently from the core voltage.

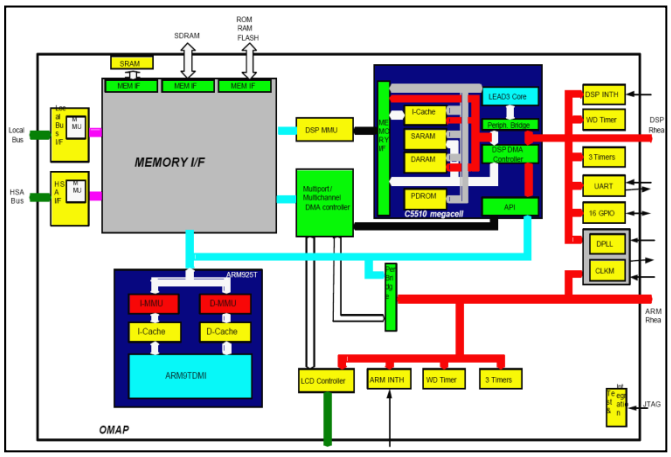

Figure 1.1: OMAP 1710 Processor Architecture [5]

In OMAP 1710 processor architecture, it is obvious that the voltages to the respective cores and peripherals are fixed and there is nothing much can be done by the system level designer to lower the voltage level to the internal circuits of OMAP 1710. Frequency is the only parameter that could be manipulated and controlled by the system level designer to conserve power during standby/ idling mode. Setting the processing speed as high as 220 MHz will force the processor to consume more power from the battery pack to support such operation but if it is set too low, a compromise on delayed information will need to be made. Apparently with this limitation, it forces system level designer to continue to source for processors with more power saving features from the processor makers.

II. INVESTIGATION OF THE KEY ELECTRICAL PARAMETERS THAT DETERMINE THE CURRENT CONSUMPTION OF CMOS BASED PROCESSOR

It is essential for portable radio system level designer to understand the key parameters affecting the current consumptions of the CMOS based processor before demands for power saving features could be fairly tabulated to the processor IC designers or key power saving features could be source from off-the-shelf processor products.

A. Complementary Metal Oxide Semiconductor (CMOS) Buffer Design

In order to gage the current consumption behavior of the CMOS transistor, a case study was conducted on a simple 28 nm CMOS buffer circuit with the following transistor properties:-

1st stage Inverter Transistor widths:
(i) Wp = 1.5 um
(ii) Wn =1 um

2nd stage Inverter Transistor width:
(i) Wp =4.5 um
(ii) Wn =3 um

The schematic for the buffer circuit is drawn with the Cadence Virtuoso Schematic Capture tool as show in Figure 2.0:-

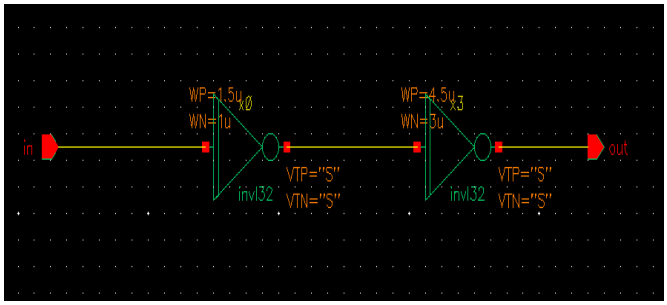

Figure 2.0: Schematic Capture of CMOS Buffer Circuit.

A HSPICE pre-layout simulation script to characterize and measure the current consumption of the CMOS buffer circuit across different voltage, frequency, and load capacitance and temperature values is written.

B. Current Measurements at Various Combinations of Voltage, Frequency, Load Capacitance and Temperature.

The current consumptions of the designed buffer circuit are measured based on 'TT' library various combination of voltage, frequency, and load capacitance and temperature profiles as summarized in Table I and II.

TABLE I. MEASURED CURRENT CONSUMPTIONS OF THE DESIGNED BUFER CIRCUIT AT 0.99 V AT VARIOUS FREQUENCY , LOAD CAPACITANCE AND TEMPERATURES.

Combinations (V-F-C-T)	Dynamic AC Current Measurement (A)
0.99V/100MHz/20fF/-40C	3.296E-06
0.99V/100MHz/20fF/125C	3.376E-06
0.99V/100MHz/150fF/-40C	1.805E-05
0.99V/100MHz/150fF/125C	1.813E-05
0.99V/500MHz/20fF/-40C	1.599E-05
0.99V/500MHz/20fF/125C	1.632E-05
0.99V/500MHz/150fF/-40C	8.644E-05
0.99V/500MHz/150fF/125C	8.676E-05

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TABLE II. MEASURED CURRENT CONSUMPTIONS OF THE DESIGNED BUFER CIRCUIT AT 1.18 V AT VARIOUS FREQUENCY , LOAD CAPACITANCE AND TEMPERATURES.

Combinations (V-F-C-T)	Dynamic AC Current Measurement (A)
1.18V/100MHz/20fF/-40C	3.928E-06
1.18V/100MHz/20fF/125C	4.166E-06
1.18V/100MHz/150fF/-40C	2.153E-05
1.18V/100MHz/150fF/125C	2.176E-05
1.18V/500MHz/20fF/-40C	1.906E-05
1.18V/500MHz/20fF/125C	2.015E-05
1.18V/500MHz/150fF/-40C	1.031E-04
1.18V/500MHz/150fF/125C	1.041E-04

A typical current consumption waveform (green color) of the simulation is shown in Figure 2.1.

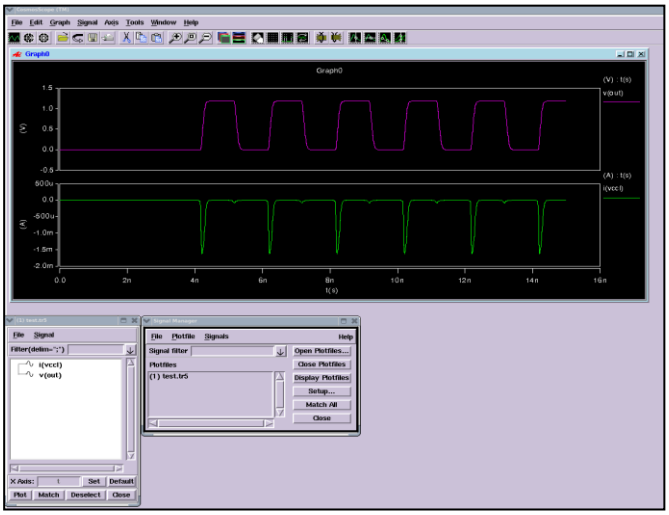

Figure 2.1: Typical Current Consumption Waveform Design of Experiments (DOE) Analysis

The current consumption data captured earlier are migrated to the Design of Experiment (DOE) template for further analysis as shown in Table IV. The template is created based on $\mathbf{2^4}$ (16 outcomes) full factorial design with Minitab 15.0 tool and the indicators to all the possible combinations are summarized in Table III.

TABLE III. INDICATORS OF THE COMBINATIONS IN DOE TEMPLATE

	Low (0)	High (1)
Voltage (v)	0.99	1.18
Frequency (f) in MHz	100	500
Load capacitance (Cload) in fFarad	20	150
Temperature in Celcius	-40	125

TABLE IV. 2^4FULL FACTORIAL DOE DESIGN TEMPLATE

ADRIAN DOE2.MTW ***

↓	C1	C2	C3	C4	C5	C6	C7	C8	C9
	StdOrder	RunOrder	CenterPt	Blocks	Voltage (V)	Frequ	Load C	Temp	Curent Consumption (uA)
1	10	3	1	1	1	-1	-1	1	4.166
2	16	6	1	1	1	1	1	1	104.100
3	15	9	1	1	-1	1	1	1	86.760
4	13	10	1	1	-1	-1	1	1	18.130
5	11	11	1	1	-1	1	-1	1	16.320
6	1	12	1	1	-1	-1	-1	-1	3.296
7	2	16	1	1	1	-1	-1	-1	3.928
8	4	17	1	1	1	1	-1	-1	19.060
9	7	19	1	1	-1	1	1	-1	86.440
10	14	21	1	1	1	-1	1	1	21.760
11	6	24	1	1	1	-1	1	-1	21.530
12	9	26	1	1	-1	-1	-1	1	3.376
13	12	27	1	1	1	1	-1	1	20.150
14	8	30	1	1	1	1	1	-1	103.100
15	5	31	1	1	-1	-1	1	-1	18.050
16	3	32	1	1	-1	1	-1	-1	15.990

The data in Table V are further analyzed in Minitab with the DOE toolbox until all the significant and insignificant terms (one way, two ways, and three ways interactions) are identified as shown in the first run-DOE analysis results in Figure 2.2. Any term that contains P-value of more than 0.05 is considered as insignificant term and must be removed from the analysis. Leveraging from Figure 2.2, the following terms are found out to be insignificant:-

(i) Load capacitance * Temperature
(ii) Voltage *Load capacitance* Temperature
(iii) Frequency *Load capacitance* Temperature

Factorial Fit: Curent Consumpti versus Voltage (V), Frequency (MHz), ...

Estimated Effects and Coefficients for Curent Consumption (uA) (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		34.1347	0.004500	7585.50	0.000
Voltage (V)	6.1790	3.0895	0.004500	686.56	0.001
Frequency (MHz)	44.7105	22.3553	0.004500	4967.83	0.000
Load Capacitance (fF)	46.6980	23.3490	0.004500	5188.67	0.000
Temperature (C)	0.4210	0.2105	0.004500	46.78	0.014
Voltage (V)*Frequency (MHz)	4.0460	2.0230	0.004500	449.56	0.001
Voltage (V)*Load Capacitance (fF)	4.0985	2.0492	0.004500	455.39	0.001
Voltage (V)*Temperature (C)	0.2185	0.1093	0.004500	24.28	0.026
Frequency (MHz)* Load Capacitance (fF)	30.5220	15.2610	0.004500	3391.33	0.000
Frequency (MHz)*Temperature (C)	0.2640	0.1320	0.004500	29.33	0.022
Load Capacitance (fF)* Temperature (C)	-0.0135	-0.0068	0.004500	-1.50	0.374
Voltage (V)*Frequency (MHz)* Load Capacitance (fF)	2.6765	1.3382	0.004500	297.39	0.002
Voltage (V)*Frequency (MHz)* Temperature (C)	0.1415	0.0708	0.004500	15.72	0.040
Voltage (V)*Load Capacitance (fF)* Temperature (C)	-0.0110	-0.0055	0.004500	-1.22	0.437
Frequency (MHz)* Load Capacitance (fF)* Temperature (C)	-0.0115	-0.0057	0.004500	-1.28	0.423

S = 0.018 PRESS = 0.082944
R-Sq = 100.00% R-Sq(pred) = 100.00% R-Sq(adj) = 100.00%

Analysis of Variance for Curent Consumption (uA) (coded units)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	4	16872.4	16872.4	4218.09	13018794.12	0.000
2-Way Interactions	6	3859.5	3859.5	643.25	1985345.52	0.001
3-Way Interactions	4	28.7	28.7	7.18	22172.62	0.005
Residual Error	1	0.0	0.0	0.00		
Total	15	20760.6				

Figure 2.2: First Run -DOE analysis results

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Subsequently, DOE analysis was rerun for the second time after the removal of the above mentioned insignificant terms and the final model transfer function of the response (current consumption) is obtained. The results of the final DOE analysis are illustrated in Figure 2.3. The normal plot of the standardized effects and Pareto chart of the effects are also shown in Figure 2.4 and Figure 2.5 respectively.

Factorial Fit: Curent Consumpti versus Voltage (V), Frequency (MHz), ...

Estimated Effects and Coefficients for Curent Consumption (uA) (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		34.1347	0.005682	6007.88	0.000
Voltage (V)	6.1790	3.0895	0.005682	543.77	0.000
Frequency (MHz)	44.7105	22.3553	0.005682	3934.63	0.000
Load Capacitance (fF)	46.6980	23.3490	0.005682	4109.54	0.000
Temperature (C)	0.4210	0.2105	0.005682	37.05	0.000
Voltage (V)*Frequency (MHz)	4.0460	2.0230	0.005682	356.06	0.000
Voltage (V)*Load Capacitance (fF)	4.0985	2.0492	0.005682	360.68	0.000
Voltage (V)*Temperature (C)	0.2185	0.1093	0.005682	19.23	0.000
Frequency (MHz)* Load Capacitance (fF)	30.5220	15.2610	0.005682	2686.01	0.000
Frequency (MHz)*Temperature (C)	0.2640	0.1320	0.005682	23.23	0.000
Voltage (V)*Frequency (MHz)* Load Capacitance (fF)	2.6765	1.3382	0.005682	235.54	0.000
Voltage (V)*Frequency (MHz)* Temperature (C)	0.1415	0.0708	0.005682	12.45	0.000

S = 0.0227266 PRESS = 0.033056
R-Sq = 100.00% R-Sq(pred) = 100.00% R-Sq(adj) = 100.00%

Analysis of Variance for Curent Consumption (uA) (coded units)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Main Effects	4	16872.4	16872.4	4218.09	8166678.21	0.000
2-Way Interactions	5	3859.5	3859.5	771.90	1494486.34	0.000
3-Way Interactions	2	28.7	28.7	14.37	27816.75	0.000
Residual Error	4	0.0	0.0	0.00		
Total	15	20760.6				

Figure 2.3: Second Run -DOE analysis results (Final)

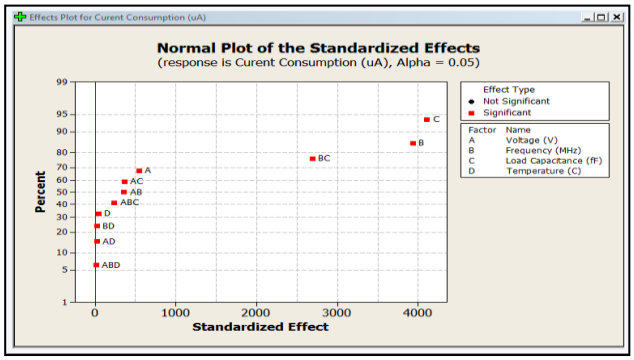

Figure 2.4: Normal plot of the standardized effects

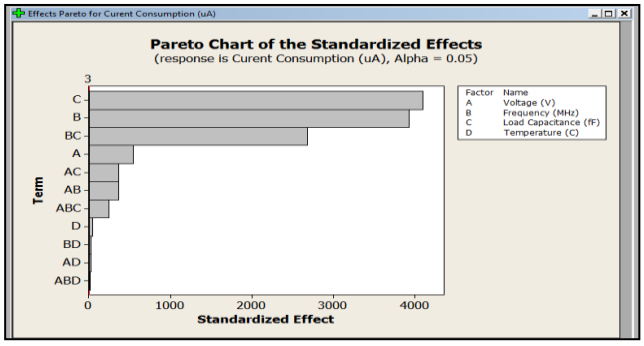

Figure 2.5: Pareto chart of the effects

Based on the results of the final DOE analysis in figure 2.3, 2.4 and 2.5 the current consumption equation for the above designed buffer circuit could be represented by the following transfer function as shown in Equation 1.0:-

$$Current\_Consumption(buffer\_circuit) = [3.0895v + 22.3553f + 23.3490Cload + 0.2105T + 2.0230(vf) + 2.0492(v.Cload) + 0.1093(vT) + 15.2610(f.Cload) + 0.1320(f.T) + 1.3382(v.f.Cload) + 0.0708(v.f.T) \quad (1.0)$$

(R-Sq is computed to be 100 %, meaning predictability can be represented by model and its transfer function).

By referring to Figure 2.5, the main electrical parameter contributing to the current consumption of the designed CMOS buffer circuit is the load capacitance parameter; followed by frequency, voltage and temperature parameters in chronological order. It shows that the current consumptions of the CMOS based system (e.g. processor) are heavily related to all these four parameters as well.

C. Analysis of Current Consumption Saving

Based on the transfer function given in Equation 1.0, further analysis was conducted on the percentage of current saving that will be salvaged if the load capacitance is reduced from 100 fF to 20 fF as shown in Table V.

TABLE V. PERCENTAGE OF CURRENT SAVING IF LOAD CAPACITANCE IS REDUCE INCREMENTALLY

Actual Voltage (V)	Voltage Factor	Actual Frequency(MHz)	Frequency Factor	Actual Cload (fF)	Cload Factor	Actual Temperature (Celcius)	Temperature Factor	Current Consumption (uA)	% Current saving
1.18	1	500	1	150	1	125	1	104.1225	0.00
1.18	1	500	1	137	0.8	125	1	95.72302	8.07
1.18	1	500	1	124	0.6	125	1	87.32354	16.13
1.18	1	500	1	111	0.4	125	1	78.92406	24.20
1.18	1	500	1	98	0.2	125	1	70.52458	32.27
1.18	1	500	1	85	0	125	1	62.1251	40.33
1.18	1	500	1	72	-0.2	125	1	53.72562	48.40
1.18	1	500	1	59	-0.4	125	1	45.32614	56.47
1.18	1	500	1	46	-0.6	125	1	36.92666	64.54
1.18	1	500	1	33	-0.8	125	1	28.52718	72.60
1.18	1	500	1	20	-1	125	1	20.1277	80.67

Up to 80.67 % of current consumption reduction could be achieved by just reducing the load capacitance from 150 fF to 20 fF. If the same equation is used and the frequency parameter is reduced from 500 MHz to 100 MHz, up to 79.10 % of current saving could be salvaged as shown in Table VI.

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TABLE VI. PERCENTAGE OF CURRENT SAVING IF FREQUENCY IS REDUCE INCREMENTALLY

Actual Voltage (V)	Voltage Factor	Actual Frequency(MHz)	Frequency Factor	Actual Cload (fF)	Cload Factor	Actual Temperature (Celcius)	Temperature Factor	Current Consumption (uA)	% Current saving
1.18	1	500	1	150	1	125	1	104.1225	0.00
1.18	1	460	0.8	150	1	125	1	95.88644	7.91
1.18	1	420	0.6	150	1	125	1	87.65038	15.82
1.18	1	380	0.4	150	1	125	1	79.41432	23.73
1.18	1	340	0.2	150	1	125	1	71.17826	31.64
1.18	1	300	0	150	1	125	1	62.9422	39.55
1.18	1	260	-0.2	150	1	125	1	54.70614	47.46
1.18	1	220	-0.4	150	1	125	1	46.47008	55.37
1.18	1	180	-0.6	150	1	125	1	38.23402	63.28
1.18	1	140	-0.8	150	1	125	1	29.99796	71.19
1.18	1	100	-1	150	1	125	1	21.7619	79.10

Meanwhile if the input voltage is reduced from 1.18 V to 0.99 V incrementally, up to 16.67 % of current saving could be easily obtained as shown in Table VII.

TABLE VII. PERCENTAGE OF CURRENT SAVING IF VOLTAGE IS REDUCE INCREMENTALLY

Actual Voltage (V)	Voltage Factor	Actual Frequency(MHz)	Frequency Factor	Actual Cload (fF)	Cload Factor	Actual Temperature (Celcius)	Temperature Factor	Current Consumption (uA)	% Current saving
1.18	1	500	1	150	1	125	1	104.1225	0.00
1.161	0.8	500	1	150	1	125	1	102.3865	1.67
1.142	0.6	500	1	150	1	125	1	100.6505	3.33
1.123	0.4	500	1	150	1	125	1	98.9145	5.00
1.104	0.2	500	1	150	1	125	1	97.1785	6.67
1.085	0	500	1	150	1	125	1	95.4425	8.34
1.066	-0.2	500	1	150	1	125	1	93.7065	10.00
1.047	-0.4	500	1	150	1	125	1	91.9705	11.67
1.028	-0.6	500	1	150	1	125	1	90.2345	13.34
1.009	-0.8	500	1	150	1	125	1	88.4985	15.01
0.99	-1	500	1	150	1	125	1	86.7625	16.67

And about 0.60 % of current saving could be achieved if the buffer temperature parameter is controlled and reduced from 125 ^{o}C to 26 ^{o}C as illustrated in Table VIII.

TABLE VIII. PERCENTAGE OF CURRENT SAVING IF TEMPERATURE IS CONTROLLED

Actual Voltage (V)	Voltage Factor	Actual Frequency(MHz)	Frequency Factor	Actual Cload (fF)	Cload Factor	Actual Temperature (Celcius)	Temperature Factor	Current Consumption (uA)	% Current saving
1.18	1	500	1	150	1	125	1	104.1225	0.00
1.18	1	500	1	150	1	108.5	0.8	104.01798	0.10
1.18	1	500	1	150	1	92	0.6	103.91346	0.20
1.18	1	500	1	150	1	75.5	0.4	103.80894	0.30
1.18	1	500	1	150	1	59	0.2	103.70442	0.40
1.18	1	500	1	150	1	42.5	0	103.5999	0.50
1.18	1	500	1	150	1	26	-0.2	103.49538	0.60
1.18	1	500	1	150	1	9.5	-0.4	103.39086	0.70
1.18	1	500	1	150	1	-7	-0.6	103.28634	0.80
1.18	1	500	1	150	1	-23.5	-0.8	103.18182	0.90
1.18	1	500	1	150	1	-40	-1	103.0773	1.00

However if we compare the worst case profile vs. the feasible profile as defined and shown in Table IX, roughly about 88.30 % current saving could be feasibly achieved; provided that the voltage is skewed to 0.99 V, buffer running at 100 MHz speed with reasonable loading of 98 fF and temperature of the buffer maintained at 26 degrees Celsius.

TABLE IX. PERCENTAGE OF CURRENT & POWER SAVING COMPARISON IN BETWEEN WORST CASE PROFILE VS. FEASIBLE PROFILE

PROFILE	Actual Voltage (V)	Actual Frequency(MHz)	Actual Cload (fF)	Actual Temperature (Celcius)	Current Consumption (uA)	Power Consumption (uW)	% Current Saving	% Power Saving
WORST CASE PROFILE	1.18	500	150	125	104.12	122.86	0.00	0.00
FEASIBLE PROFILE	0.99	100	98	26	12.18	12.06	88.30	90.19

These comparisons testified that if current saving of up to 88.30 % could be easily achieved in a simple CMOS buffer design; theoretically it is also feasible in the CMOS based processor design.

III. KEY PROCESSOR FEATURES FOR POWER SAVING

In the quest to reduce the current consumption of the processor in the portable two-way radio, radio designers will need to start to consider processor with the following features:-

1) Mechanism to disable or turn off selective circuits (load) that are unused during standby mode.
2) Mechanism to scale down the speed of the processor (frequency) to lower speed during standby mode.
3) Mechanism to scale down the voltage to lower operating voltage during system standby mode.
4) Mechanism to measure the temperature of the processor and control the temperature of processor.

A. Load Reduction Scheme

Load reduction scheme is a scheme that could be used to intelligently disable the unused internal circuits or modules in the processor during radio idle or standby mode to reduce current consumption which will lead to lower power consumptions.

For example, such feature is available in OMAP-L138 processor in which unused modules can be disabled by using the power sleep controllers (PSC) to turn off the clock to the unused peripherals or modules [9]. There are two PSCs in the OMAP-L138 processor which are utilized to manage the system power on/off, clock on/off and reset schemes. The first power sleep controller, PSC0 controls the power on/off, clock on/off and reset schemes of the core modules while the second power sleep controller, PSC1 controls the power on/off, clock on/off and reset schemes of the peripherals modules as shown in Table X and Table XI respectively.

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TABLE X. MODULES CONTROLLED BY PSC0 AND ITS DEFAULT STATES[9].

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/ Wake Only
0	EDMA3_0 Channel Controller 0	AlwaysON (PD0)	SwRstDisable	—
1	EDMA3_0 Transfer Controller 0	AlwaysON (PD0)	SwRstDisable	—
2	EDMA3_0 Transfer Controller 1	AlwaysON (PD0)	SwRstDisable	—
3	EMIFA (BR7)	AlwaysON (PD0)	SwRstDisable	—
4	SPI0	AlwaysON (PD0)	SwRstDisable	—
5	MMC/SD0	AlwaysON (PD0)	SwRstDisable	—
6	ARM Interrupt Controller	AlwaysON (PD0)	Enable	—
7	ARM RAM/ROM	AlwaysON (PD0)	Enable	Yes
8	Not Used	—	—	—
9	UART0	AlwaysON (PD0)	SwRstDisable	—
10	SCR0 (BR0, BR1, BR2, BR8)	AlwaysON (PD0)	Enable	Yes
11	SCR1 (BR4)	AlwaysON (PD0)	Enable	Yes
12	SCR2 (BR3, BR5, BR6)	AlwaysON (PD0)	Enable	Yes
13	PRU	AlwaysON (PD0)	SwRstDisable	—
14	ARM	AlwaysON (PD0)	SwRstDisable	—
15	DSP	PD_DSP (PD1)	Enable	—

TABLE XI. MODULES CONTROLLED BY PSC1 AND ITS DEFAULT STATES[9].

LPSC Number	Module Name	Power Domain	Default Module State	Auto Sleep/ Wake Only
0	EDMA3_1 Channel Controller 0	AlwaysON (PD0)	SwRstDisable	—
1	USB0 (USB2.0)	AlwaysON (PD0)	SwRstDisable	—
2	USB1 (USB1.1)	AlwaysON (PD0)	SwRstDisable	—
3	GPIO	AlwaysON (PD0)	SwRstDisable	—
4	HPI	AlwaysON (PD0)	SwRstDisable	—
5	EMAC	AlwaysON (PD0)	SwRstDisable	—
6	DDR2/mDDR	AlwaysON (PD0)	SwRstDisable	—
7	McASP0 (+ McASP0 FIFO)	AlwaysON (PD0)	SwRstDisable	—
8	SATA[1]	AlwaysON (PD0)	SwRstDisable	—
9	VPIF	AlwaysON (PD0)	SwRstDisable	—
10	SPI1	AlwaysON (PD0)	SwRstDisable	—
11	I2C1	AlwaysON (PD0)	SwRstDisable	—
12	UART1	AlwaysON (PD0)	SwRstDisable	—
13	UART2	AlwaysON (PD0)	SwRstDisable	—
14	McBSP0 (+ McBSP0 FIFO)	AlwaysON (PD0)	SwRstDisable	—
15	McBSP1 (+ McBSP1 FIFO)	AlwaysON (PD0)	SwRstDisable	—
16	LCDC	AlwaysON (PD0)	SwRstDisable	—
17	eHRPWM0/1	AlwaysON (PD0)	SwRstDisable	—
18	MMC/SD1	AlwaysON (PD0)	SwRstDisable	—
19	uPP	AlwaysON (PD0)	SwRstDisable	—
20	eCAP0/1/2	AlwaysON (PD0)	SwRstDisable	—
21	EDMA3_1 Transfer Controller 0	AlwaysON (PD0)	SwRstDisable	—
22-23	Not Used	—	—	—

When the module is in enable state, the clock signal is enabled and the module works as in normal operation. However when the module is in disable state the clock signal is disabled indefinitely to conserve power. This scheme is also known as clock gating scheme by some designers, where the input to the devices are gated with a static LOW state (logic zero state) to prevent it from running.

B. Dynamic Voltage & Frequency Scaling (DVFS) Scheme

Dynamic voltage and frequency scaling scheme is the scheme that could be utilized to scale down the main processing unit and core voltages in the processor to lower value in relation to the processing speed of the processor when portable radio is in idling mode; a mode which does not require the processor to run at exceptionally high speed condition. For example in OMAP3503, the main processing unit (MPU) is powered by VDD_MPU while the interconnect and peripherals are powered by VDD_CORE. Both the VDD_MPU and VDD_CORE voltages will be adjusted based on maximum accompanying clock frequency allowed on the internal MPU, interconnects and peripherals as shown in Table XII and Table XIII.

TABLE XII. VDD_MPU OPERATING POINTS [8].

PROCESSOR OPP	VDD_MPU	ARM Max MHz
5	1.35	600
4	1.27	550
3	1.20	500
2	1	250
1	0.95	125

TABLE XIII. VDD_CORE OPERATING POINTS [8].

INTERCONNECT/ PERIPHERALS OPP	VDD_CORE	L3 Max MHz
3	1.15	166
2	1	100
1	0.95	41.5
See the latest OMAP™3 Operating Condition Addendum for the most current voltage values.		

In order to utilize the above schemes, two external programmable regulators (TPS62352) must be used as independent supplies for both VDD_MPU and VDD_CORE supplies. The output voltage of the regulators will be programmed via I2C data coming from the OMAP 3503 processor as illustrated in Figure 3.0.

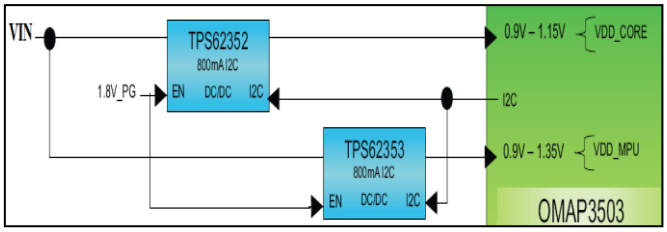

Figure 3.0: Two External Programmable Regulators for OMAP 3503 DVFS Scheme [8].

C. Temperature Sensing & Clock Frequency Adjustment Scheme

Temperature sensing and clock adjustment scheme is a scheme that measures the temperature of the processor with the internal temperature sensing diode in real time and scale down the frequency of the internal module operation adaptively so that the temperature of the processor could be contained in room temperature and thus current consumption of the processor could be minimized indefinitely. Such scheme is still not available in the market. However a brief architecture of the temperature sensing and clock frequency adjustment scheme is illustrated in Figure 3.1.

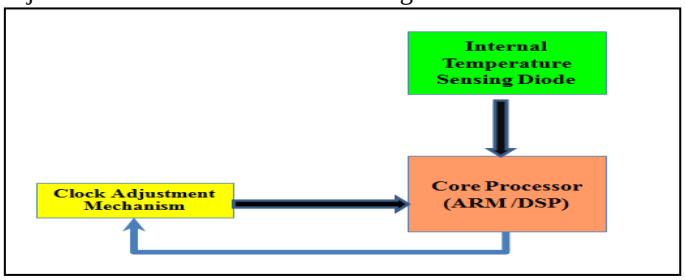

Figure 3.1: Temperature Sensing & Clock Frequency Adjustment Scheme

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IV. SUMMARY & CONCLUSION

Design of experiments on a simple 28nm CMOS buffer circuit proves that current consumption of the CMOS based devices (e.g. processor) could be lowered down by reducing the values of the load capacitance, voltage, frequency and temperature. From quick analysis, current saving of up to 88.30 % could be easily achieved in a simple CMOS buffer design as discussed in Section II. Theoretically, it proves that such current consumption savings are also feasible in CMOS based processor design. This could be simply achieved by utilizing processor that offers load reduction scheme, dynamic voltage and frequency scaling feature, temperature sensing and clock frequency adjustment scheme. With all these current saving features in place, radio designers will be able to reduce the overall current consumption of the processor at idle mode and offer better battery life specification to the customers without the need to increase the size of the battery capacity while keeping the development cost at bay.

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