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Analysis of Phase Locked Loop Using 180nm Technology for Bluetooth Applications

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Abstract: Bluetooth is a wireless technology standard for short-wave length radio transmission of data for both fixed and mobile devices, thereby creating personal area network. This provides a secure communication between devices such as faxes, mobile phones, laptops, PCs, global positioning system receivers. An on-chip phase locked loop (PLL) for Bluetooth application is specified in this paper. The closed loop of the proposed PLL is stable. This phase locked loop was designed with a digitally controlled oscillator, a phase detector, loop filter and a divide by N counter. The phase locked loop is simulated to have a lock in range of 2430MHz to 2470MHz. In the proposed Phase locked loop, area is 12156(um^2), power is 305825(nW), delay is 7620(ps) and memory is 65307(K). Cadence encounter tool is used to analyse and compare the conventional phase locked loop and proposed phase locked loop.

Keywords: Phase locked loop (PLL), phase detector, lock range, Bluetooth application

I. INTRODUCTION

Bluetooth is one of the emerging communication protocols which provide low-cost, short range radio links between mobile phones, mobile PCs and other portable electronic devices [1-3]. An on chip phase locked loop for Bluetooth application is proposed in this work. Phase locked loop finds applications in space communication for demodulation extension, bit synchronization, symbol synchronization and demodulation of frequency demodulated signal [4-5].

Phase locked loops are widely used to provide the local oscillator for transmission and reception purposes in digital wireless communication systems such as GSM and CDMA. To reduce the cost and size of the most cellular handsets, phase locked loop has been integrated into a single integrated circuit [6-8]. In GSM applications these local oscillator modules are composed of a frequency synthesizer integrated circuit and voltage control oscillators.

A frequency synthesizer generates any range of frequencies from a single oscillator, which finds application in many modern devices including radio receivers, mobile telephones, radio phones, CB radios, walkie-talkies, satellite receivers, GPS systems etc. The desired output signal can be generated by the frequency synthesizer by performing various operations such as frequency multiplication, frequency division and frequency mixing [9-12].

Phase detector of phase locked loop performs the comparison between the reference input and feedback from digitally controlled oscillator. In applications using conventional phase locked loop, the dead-zone problem is eliminated by using tri-state phase detector which introduces a delay in the reset path. In the proposed phase detector this delay component can be avoided as there is no dead-zone problem.

In this proposed work an analysis of Phase locked loop operation and the comparison of conventional and proposed phase locked loop using cadence encounter tool has been presented. The proposed phase locked loop architecture for Bluetooth application achieves low power consumption, less area and less propagation delay as compared to the conventional phase locked loop architectures which are used for the same application.

The organisation of the rest of this paper is described as follows. In section II, the conventional PLL architecture is specified. The proposed PLL architecture is presented in section III. In section IV the experimental results and comparison of the performance parameters of the conventional phase locked loop and proposed phase locked loop is mentioned. The conclusion of this proposed work is given in section V.

II. CONVENTIONAL PHASE LOCKED LOOP SYSTEMS

A conventional phase locked loop consists of phase detector, low pass filter and digitally controlled oscillator. In conventional phase locked loop, tri-state phase detectors are used.

A. Conventional PLL architecture

The block diagram of the conventional phase locked loop is shown in figure 1. In conventional Phase locked loop the tri-state phase detector compares the input signal and feedback signal from the digitally controlled oscillator and generates an output error signal. The output of the phase detector is then fed to the low pass filter which filters out the high frequency components. According to the control signal generated by low pass loop filter, digitally controlled oscillator produces oscillations and it is fed back to the phase detector as one of its input.

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The tri-state phase detector used in conventional phase locked loop provides nonzero gain for both positive and negative phase error signals. The main disadvantage of tri-state phase detector is that it introduces a delay in the reset path in order to avoid the dead zone problem.

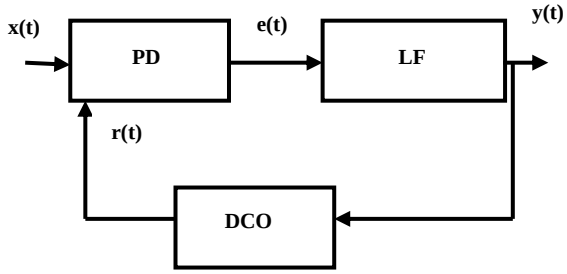

Fig. 1. Block diagram of conventional phase locked loop

III. PROPOSED PHASE LOCKED LOOP ARCHITECTURE

An on chip phase locked loop for Bluetooth applications is proposed here. The proposed phase locked loop architecture and the block diagram of key components such as two-state phase detector, loop filter, digitally controlled oscillator (DCO) and divide by N counter are mentioned here.

A. Proposed architecture

The block diagram of proposed phase locked loop architecture is shown in figure 2. It consists of JK phase detector, K counter loop filter, digitally controlled oscillator (DCO) and divide by N counter.

The phase detector compares the reference input signal and digitally controlled oscillator feedback input and generates a differential output, which is proportional to the phase difference between the two input signals. The loop filter suppresses the high frequency component in the phase detector output and produces a dc output which act as the control signal for the digitally controlled oscillator. Then digitally controlled oscillator oscillates according to a control signal generated by the loop filter. The DCO output signal is divided by divide by N counter and is fed back to the phase detector which acts as the one of its input signal.

B. Phase locked loop building blocks

The basic phase locked loop building blocks consists of phase detector, loop filter, digitally controlled oscillator and divide by N counter. Phase detector compares the phase difference between two input signals and produces a phase error signal. The block diagram of JK phase detector is shown in figure 2. The two input signals of phase detector are binary values. The counter is reset on the rising edge of a1 and is gated when output signal become logic 1. Then the output generated is proportional to the phase error signal and act as control signal to the DCO.

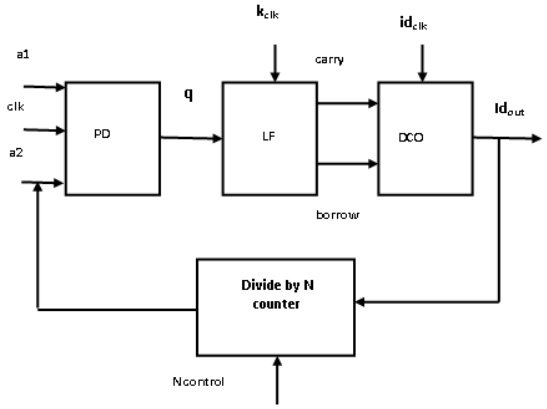

Fig. 2. Block diagram of proposed phase locked loop

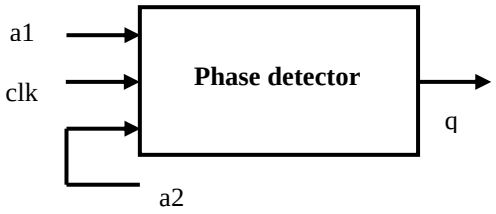

Fig. 3. Proposed JK phase detector

The phase detector output signal is then passed through a low pass loop filter, which removes the high frequency components in the signal. The block diagram of K counter loop filter is shown in the figure 4. This loop filter consists of an up counter and down counter which are used for counting upwards. The up and down bit determines which counter is performing the operation at any moment. The K clock signal
is found to be M*a1, where M is a large integer of the reference input signal a1. The generated carry and borrow outputs are the most significant bits of the counters and becomes high only when the particular counter values are greater than K/2. These output values are fed to DCO which controls the DCO operation.

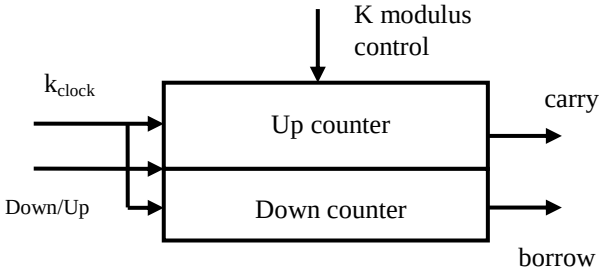

Fig. 4. Proposed K counter loop filter

A digitally controlled oscillator is similar to that of a voltage controlled oscillator which is synchronized to an external frequency reference pulses which are produced by a digital counter. This counter acts as a frequency divider which counts pulse from a master clock operating at high frequency and toggles its output state when the

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counter attains some predetermined value. The counter output frequency can be defined by the number of pulses it counts, which generates a square wave of required frequency. The block diagram of digitally controlled oscillator is shown in the figure 5.

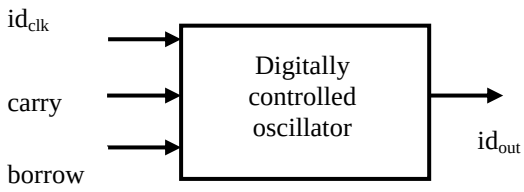

Fig.5. Proposed digitally controlled oscillator

The divide by N counter divides the DCO output signal and fed back to phase detector as one of its input signal. This counter resets at the n^{th} clock pulse and act as phase dividers which divides the frequency by a factor of 1/N. The block diagram of the proposed divide by N counter is shown in the figure 6.

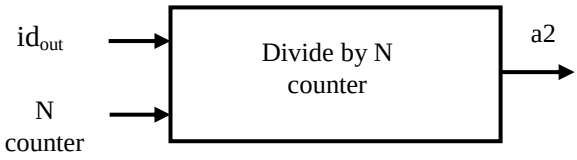

Fig.6. Proposed divides by N counter

IV. EXPERIMENTAL RESULTS

An on chip PLL for Bluetooth application is designed and its various performance parameters have been analysed using cadence encounter tool. The proposed PLL is simulated to have a lock in range of 2430MHz to 2470MHz.

A. Pre-layout analysis of performance parameters

The pre-layout analysis of performance parameters were carried out individually for both the conventional and proposed PLL and the results are compared here. The use of tri-state phase detector in conventional phase locked loop increases the area usage up to 13698μm^2. The major drawback of conventional phase locked loop is the large power consumption of about 423897nW. It has a memory usage of 67880K and provides a delay of 8540ps.

The inclusion of tri-state phase detector in conventional phase locked loop to avoid the dead zone problem, introduces a delay in the reset path. This problem is overcome by using two state phase detector in this proposed phase locked loop.

This reduces the area usage up to 12156μm^2. In proposed phase locked loop, large power consumption of conventional phase locked loop due to the inclusion of tri-state phase detectors is substantially reduced up to a value of 305825nW.

TABLE I
COMPARISON OF PERFORMANCE PARAMETERS IN PRE-LAYOUT ANALYSIS

Parameter	Conventional	Proposed
Area(μm^2)	13698	12156
Power(nW)	423897	305824
Memory(K)	67880	65307
Delay(ps)	8540	7620
Instances	545	536

As there is no delay component in proposed phase locked loop, the delay is sufficiently reduced by a value of 7620ps. The memory usage is also less as compared to conventional phase locked loop. It reduces up to a value of 7620ps. Thus, the proposed phase locked loop has reduced power consumption, less delay, less area usage and less memory usage as compared to conventional phase locked loop. Therefore, it provides better performance and high efficiency as compared to the conventional one.

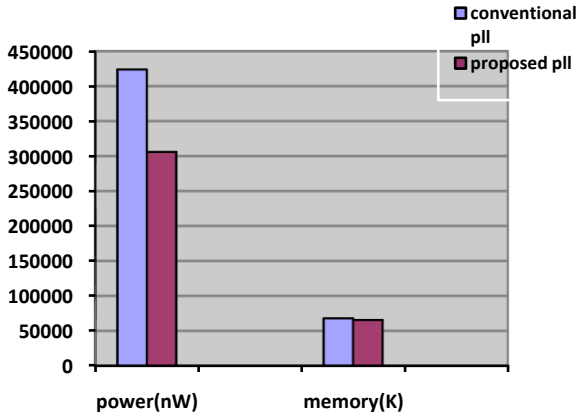

Fig.7. Power and Memory analysis

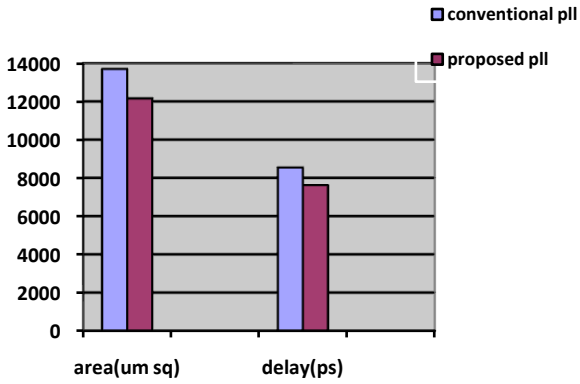

Fig.8. Area and Delay analysis

B. Post-layout analysis of performance parameters

The post-layout analysis of performance parameters were carried out individually for both the conventional and proposed PLL and the results are compared here.

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TABLE II
COMPARISON OF PERFORMANCE PARAMETERS IN POST-LAYOUT ANALYSIS

Parameter	Conventional	Proposed
Power(mW)	0.2309	0.1051
Memory(megabytes)	362	358.843
Instances	545	536

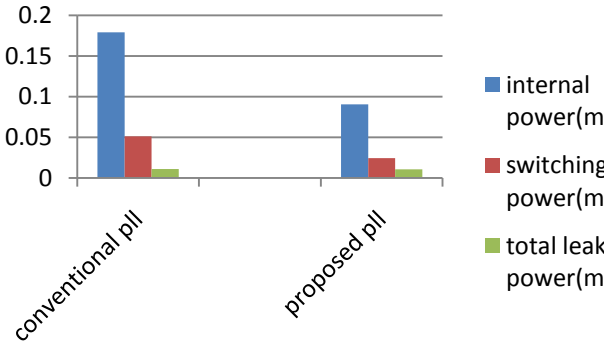

Fig.9. Power analysis of conventional and proposed pll

V. CONCLUSIONS

Analysis of on chip phase locked loop for Bluetooth applications has been done and various performance parameters of conventional phase locked loop and proposed phase locked loop has been compared in this work using cadence encounter tool. The phase locked loop is simulated to have a lock range of 2430MHz to 2470MHz. In the conventional phase locked loop area is 13698(μm^2), power is 423897nW, delay is 8540(ps) and memory is 67880(K). In the proposed phase locked loop area is 12156(μm^2), power is 305825(nW), delay is 7620(ps) and memory is 65307(K).

In future works, the proposed Phase locked loop can be implemented using mixed logic by introducing charge pump at the output of phase detector. Analog implementation has various advantages like high performance, better accuracy and high precision. Digital implementation also has many advantages such as power optimization, speed and area optimization. Then the implementation of phase locked loop in mixed logic has the combined advantages of both analog and digital logic implementation.

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BIOGRAPHY

Merin Annie Joy received her B.Tech degree in Electronics and Communication Engineering from Mount Zion College of Engineering Kadammanitta in 2010. Currently she is pursuing M.Tech VLSI Design from Karunya University, Coimbatore.